User's Guide

TPS61376 Evaluation Module

ABSTRACT

This user's guide describes the setup, schematic, and layout of the evaluation module (EVM) for the TPS61376. The EVM helps to evaluate the behavior and performance of the device at different input voltage, output voltage, and load conditions. This EVM is optimized for 5-V input voltage and 12-V output voltage applications. The feedback divider and compensation network can be modified for other application conditions, according to the data sheet.

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1 Introduction

The TPS61376 is a high voltage non-synchronous boost converter with load-disconnect and input current limit functions. The device has output overvoltage protection and hiccup mode for overcurrent protection to prevent the device from over heat. This EVM is optimized for 5-V input voltage and 12-V output voltage applications. The operating conditions of the EVM can be easily changed by modifying the external components.

1.1 Performance Specification

Table 1-1 provides the summary of the TPS61376EVM performance specifications. All the specifications are given for an ambient temperature of 25°C.

Table 1-1. Performance Specification

Parameter	Test Condition	Value	Unit
Input voltage		3-8	V
Output voltage		12	V
Maximum input current	ISEL = H	3	A
	ISEL = L	0.75	A
Default switching frequency		1200	kHz

1.2 Modification

The external components of the TPS61376 device can be modified to adjust the output voltage, input current limit, and response speed of real applications.

1.3 Input Capacitor C8

The 47-µF, 35-V aluminum capacitor C8 is added as the input capacitor in the EVM. The capacitor is not necessary and can be removed in a real application.

2 Test Setup

This section describes how to properly connect, set up, and use the TPS61376 EVM.

2.1 Input/Output Connector Descriptions

Jumper	Description
J1	Input voltage positive connection
J2	Output voltage positive connection
J3	Input voltage return connection
J4	Output voltage return connection
JP1	EN pin input jumper. Place a jumper across EN and H to turn on the IC. Place a jumper across EN and L to turn off the IC.
JP2	ISEL pin input jumper. Place a jumper across ISEL and H to set the device input current limit in high range. Put the jumper across ISEL and L to set the device input current limit in low range.
TP1	Input voltage positive sensing node for measuring efficiency
TP2	Output voltage positive sensing node for measuring efficiency
TP3	Input voltage negative sensing node for measuring efficiency
TP4	Output voltage negative sensing node for measuring efficiency
TP5	Test point to measure bode plot
TP6	Test point to measure SW pin waveform

3 Schematic and Bill of Materials

This section provides the TPS61376 EVM schematic and bill of materials (BOM).

3.1 Schematic

Figure 3-1 shows the TPS61376 EVM schematic.

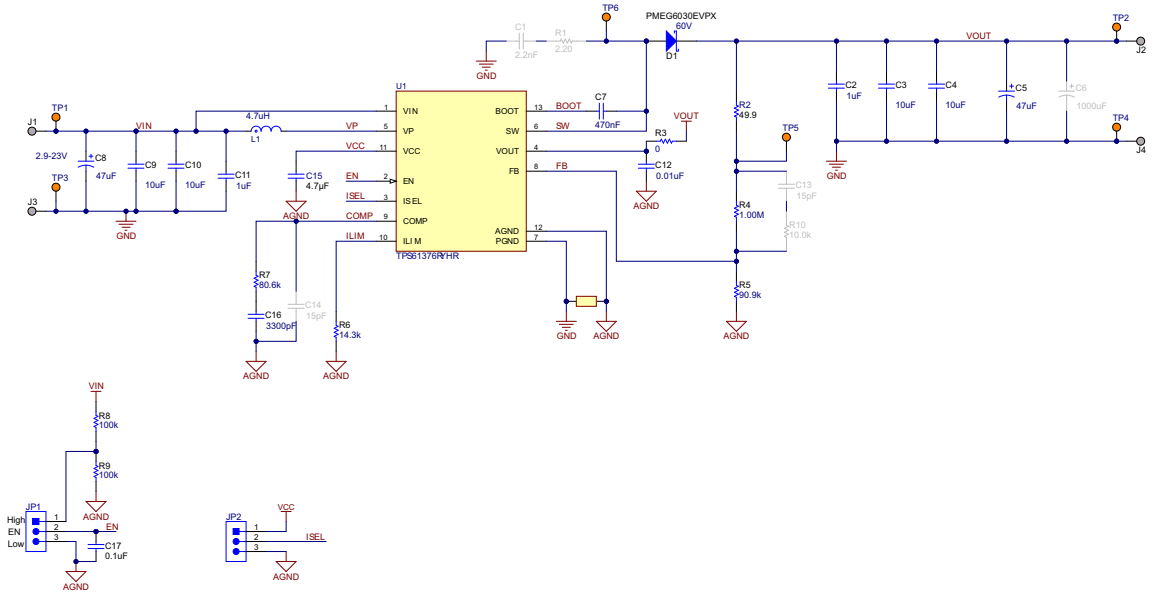

Figure 3-1. Schematic

3.2 Bill of Materials

Table 3-1 lists the BOM of the TPS61376 EVM.

Table 3-1. TPS61376EVM Bill of Materials

Designator	Qty	Value	Description	PackageReference	PartNumber	Manufacturer
C2, C11	2	1 µF	CAP, CERM, 1 µF, 35 V, ±10%, X5R, 0402	0402	GRM155R6YA105KE11D	MuRata
C3, C4, C9, C10	4	10 µF	CAP, CERM, 10 µF, 50 V, ±10%, X5R, AEC-Q200 Grade 1, 1206	1206	GRT31CR61H106KE01L	MuRata
C5, C8	2	47 µF	CAP, AL, 47 µF, 35 V, ±20%, 0.06 Ω, SMD	SMT Radial D	EEHZC1V470P	Panasonic
C7	1	0.47uF	CAP, CERM, 0.47 uF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E474KA12D	MuRata
C12	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H103KA88D	MuRata
C15	1	4.7 µF	CAP, CERM, 4.7 µF, 16 V, ±10%, X5R, AEC-Q200 Grade 3, 0603	0603	GRT188R61C475KE13D	MuRata
C16	1	3300 pF	CAP, CERM, 3300 pF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B2X7R1H332K050BA	TDK
C17	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
D1	1	60 V	Diode, Schottky, 60 V, 3 A, SOD-128	SOD-128	PMEG6030EVPX	Nexperia
J1, J2, J3, J4	4		Terminal, Turret, TH, Double	Keystone1502-2	1502-2	Keystone
JP1, JP2	2		Header, 100 mil, 3 × 1, Tin, TH	Header, 3 PIN, 100 mil, Tin	PEC03SAAN	Sullins Connector Solutions
L1	1	4.7 µH	Shielded Power Inductor, 4.7 µH, 19.6 mΩ, 7.4 A	SMT2_5MM28_5MM48	XEL5050-472MEC	Coilcraft
R2	1	49.9	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040249R9FKED	Vishay-Dale
R3	1	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0EDHP	Vishay-Dale
R4	1	1.00 Meg	RES, 1.00 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M00FKED	Vishay-Dale
R5	1	90.9 k	RES, 90.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040290K9FKED	Vishay-Dale
R6	1	14.3 k	RES, 14.3 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040214K3FKED	Vishay-Dale
R7	1	80.6 k	RES, 80.6 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040280K6FKED	Vishay-Dale
R8, R9	2	100 k	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100KFKED	Vishay-Dale
SH-JP1, SH-JP2	2		Shunt, 100 mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
TP1, TP2, TP3, TP4, TP5, TP6	6		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
U1	1		23-VIN, 25-VOUT, 4.5-A, Boost Converter with Input Average Current Limit and Load Disconnect	VQFN-HR-13	TPS61376RYHR	Texas Instruments
C1	0	2200 pF	CAP, CERM, 2200 pF, 250 V, ±10%, X7R, 0805	0805	GRM21AR72E222KW01D	MuRata

Table 3-1. TPS61376EVM Bill of Materials (continued)

Designator	Qty	Value	Description	PackageReference	PartNumber	Manufacturer
C6	0	1000 µF	CAP, AL, 1000 µF, 35 V, ±20%, 0.018 Ω, TH	D12.5xL20mm	EEU-FR1V102B	Panasonic
C13, C14	0	15 pF	CAP, CERM, 15 pF, 50 V, ±5%, C0G/NP0, 0402	0402	GRM1555C1H150JA01D	MuRata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R1	0	2.2	RES, 2.20, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8RQF2R2V	Panasonic
R10	0	10k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0FKED	Vishay-Dale

4 Board Layout

The TPS61376 EVM board is a 4-layer, 1-oz copper thick PCB. All the components are placed on the top layer. Figure 4-1 and Figure 4-2 show the top view and bottom view, respectively. Figure 4-3 and Figure 4-4 show the inner layer 1 and inner layer 2, respectively.

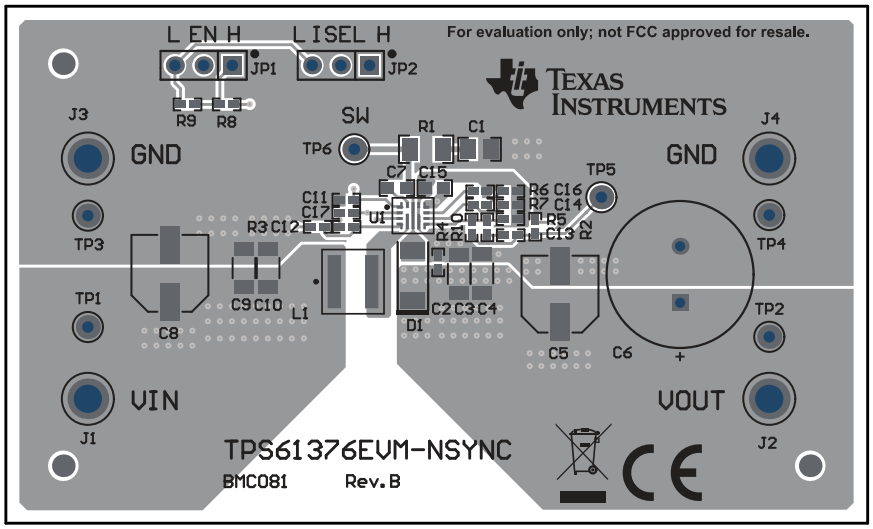

Figure 4-1. Top-Side Layout

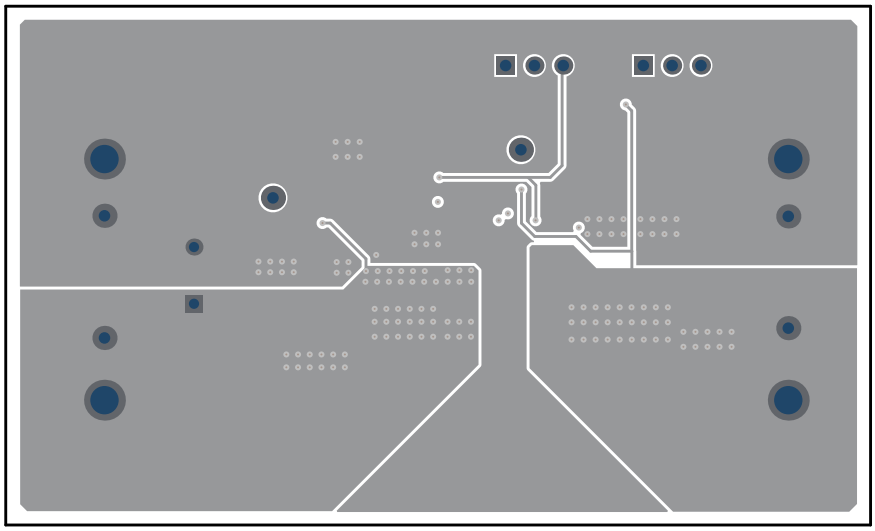

Figure 4-2. Bottom-Side Layout

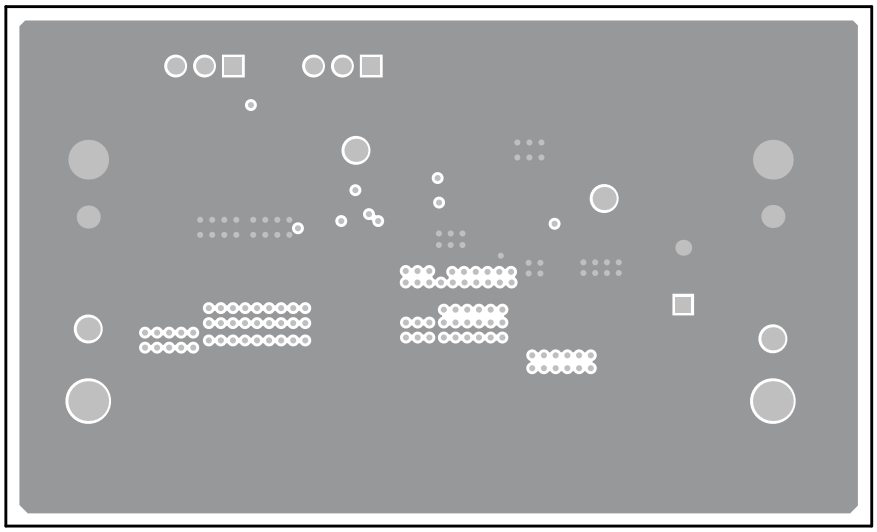

Figure 4-3. Inner Layer 1 Layout

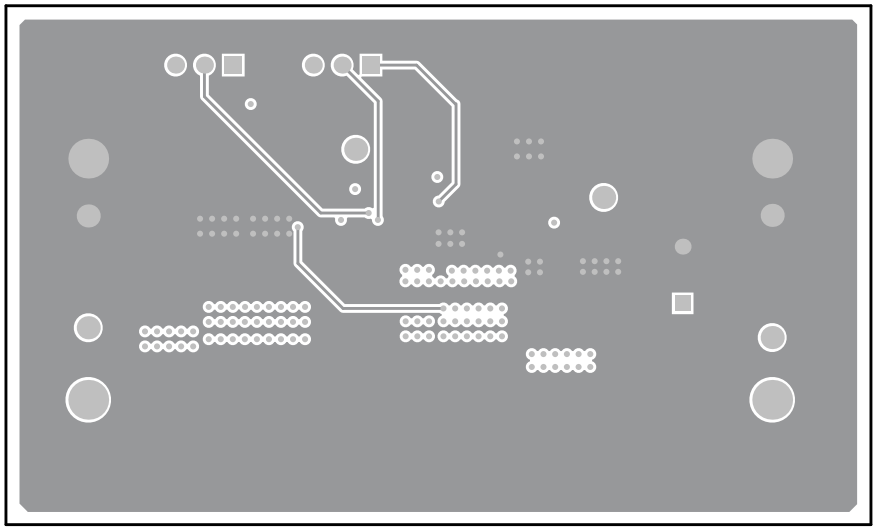

Figure 4-4. Inner Layer 2 Layout

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2022) to Revision B (March 2023)	Page
• Changed device MODE pin name to ISEL	2
• Changed device MODE pin name to ISEL	2

Changes from Revision * (January 2022) to Revision A (August 2022)	Page
• Updated schematic and bill of materials	3
• Updated board layout images	6

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