## Character Display Module

### Part Number

C81BLGFGN06CT30XAG

### Overview

Character: 8x1(55x27.6), FSTN, Gray background, No Backlight, Bottom view, -20C to +85C operating, -30C to +90C storage, Transflective (positive), 3.3V, Controller=ST7036, RoHS Compliant
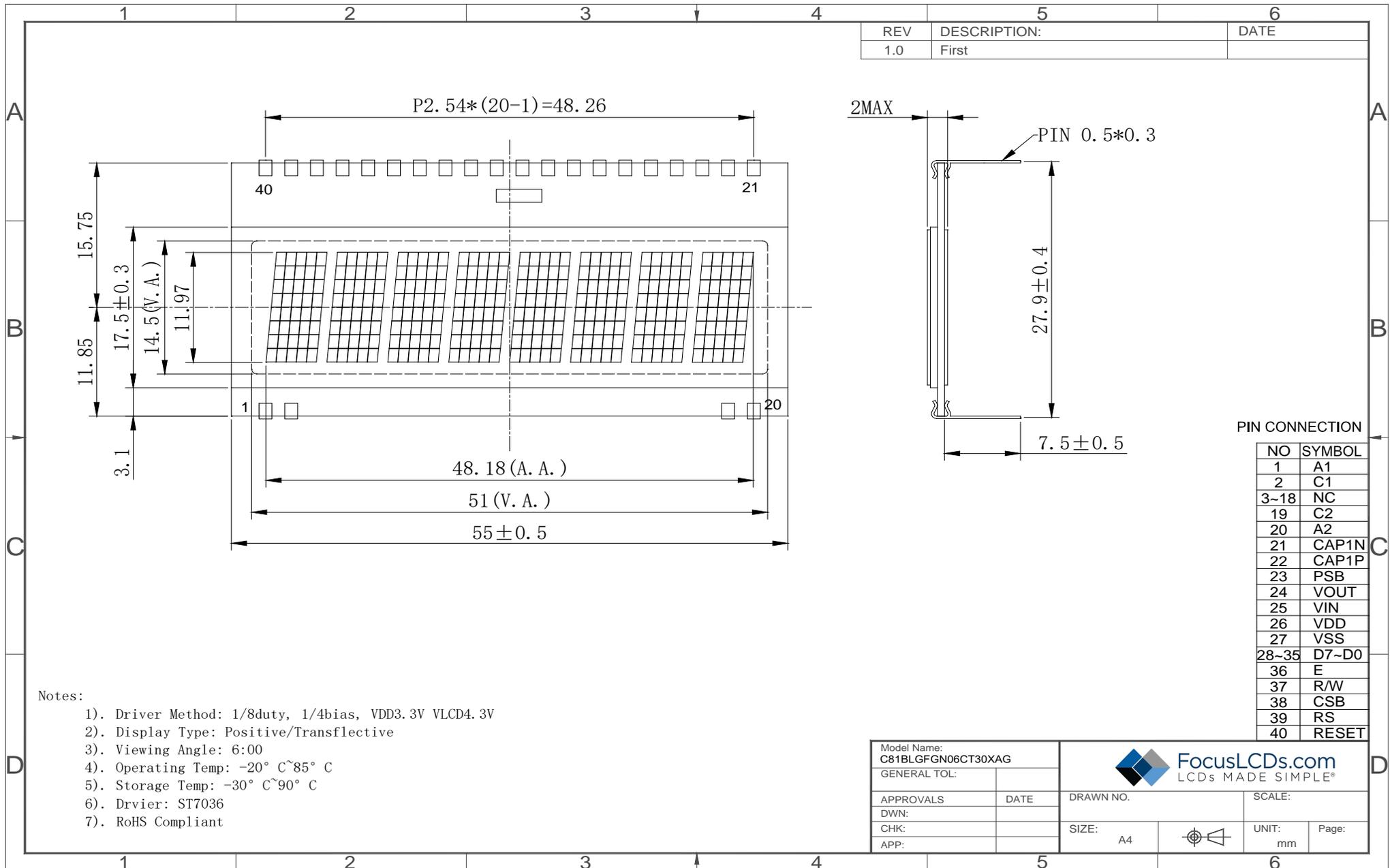
## 1.Features

1. 5x8 dots with cursor
2. Built-in controller ST7036
3. +3.3V power supply
4. 1/8 duty cycle;1/4bias
5. 8characters *1lines display

| LCD type | ☐TN | | | |
|---|---|---|---|---|
| | ☑FSTN | ☐FSTN Negative | | |
| | ☐STN Yellow Green | ☐STN Gray | | ☐STN Blue Negative |
| **View direction** | ☑6 O'clock | ☐12 O'clock | | |
| **Rear Polarizer** | ☐Reflective | ☑Transflective | | ☐Transmissive |
| **Temperature Range** | ☐Normal | ☑Wide | | ☐Super Wide |
| **DC to DC circuit** | ☐Build-in | ☑Not Build-in | | |
| **Touch screen** | ☐With | ☑Without | | |
| **Font type** | ☑English-Japanese | ☐English-Europen | ☐English-Russian | ☐Other |

## 2. MECHANICAL SPECIFICATIONS

| | |
|---|---|
| Module size | 55.0mm(L)*27.6mm(W)*9.2mm(H) |
| Viewing area | 51.0mm(L)*14.5mm(W) |
| Weight | Approx. |

# 3.Outline dimension

| REV | DESCRIPTION: | DATE |
|---|---|---|
| 1.0 | First | |

P2.54*(20-1)=48.26

2MAX

PIN 0.5*0.3

40

21

15.75

27.9±0.4

17.5±0.3

14.5(V.A.)

11.97

11.85

1

20

3.1

7.5±0.5

48.18(A.A.)

51(V.A.)

55±0.5

**PIN CONNECTION**

| NO | SYMBOL |
|---|---|
| 1 | A1 |
| 2 | C1 |
| 3~18 | NC |
| 19 | C2 |
| 20 | A2 |
| 21 | CAP1N |
| 22 | CAP1P |
| 23 | PSB |
| 24 | VOUT |
| 25 | VIN |
| 26 | VDD |
| 27 | VSS |
| 28~35 | D7~D0 |
| 36 | E |
| 37 | R/W |
| 38 | CSB |
| 39 | RS |
| 40 | RESET |

Notes:
1). Driver Method: 1/8duty, 1/4bias, VDD3.3V VLCD4.3V
2). Display Type: Positive/Transflective
3). Viewing Angle: 6:00
4). Operating Temp: -20° C~85° C
5). Storage Temp: -30° C~90° C
6). Drvier: ST7036
7). RoHS Compliant

Model Name:
C81BLGFGN06CT30XAG

GENERAL TOL:

APPROVALS | DATE
DWN:
CHK:
APP:

DRAWN NO.

SCALE:

SIZE: A4

UNIT: mm

Page:

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# 4.Absolute maximum ratings

| Item | Symbol | Standard | | | Unit |
|---|---|---|---|---|---|
| Power voltage | $V_{DD}$-$V_{SS}$ | 0 | - | 7.0 | V |
| Input voltage | $V_{IN}$ | VSS | - | VDD | |
| Operating temperature range | $V_{OP}$ | -10 | - | +50 | ℃ |
| Storage temperature range | $V_{ST}$ | -20 | - | +70 | |

# 5.Block diagram
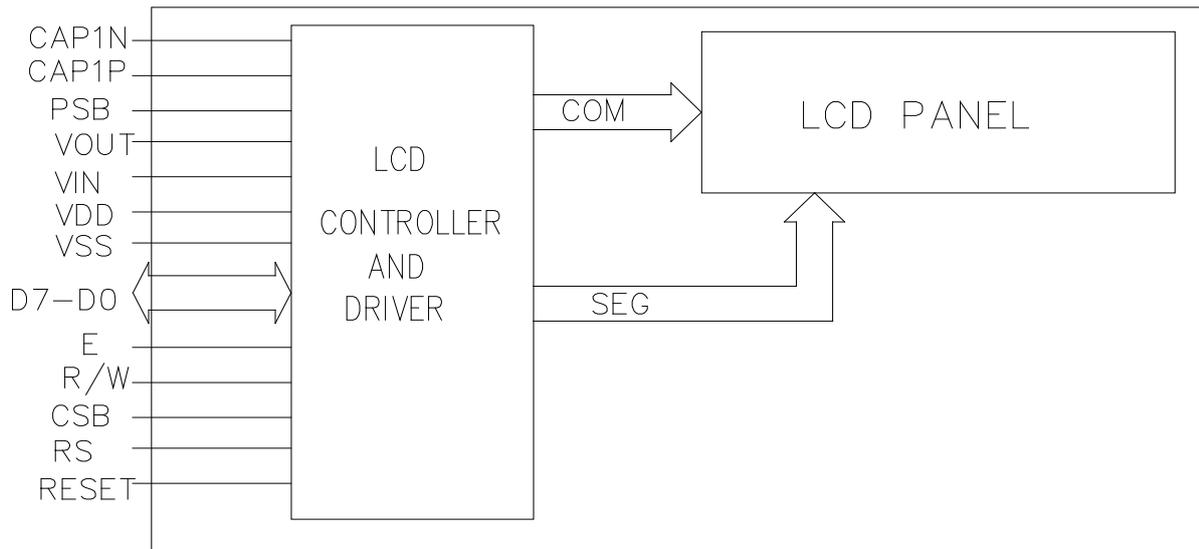


# 6.Interface pin description

| Pin no. | Symbol | External connection | Function |
|---|---|---|---|
| 1 | A1 | Power supply | Power supply    (+3.0V) for BKL |
| 2 | C1 | Power supply | Ground for BKL (GND) |
| 3~18 | NC | | |
| 19 | C2 | Power supply | Ground for BKL (GND) |
| 20 | A2 | Power supply | Power supply    (+3.0V) for BKL |
| 21 | CAP1N | Power supply | For voltage booster circuit |
| 22 | CAP1P | Power supply | For voltage booster circuit |
| 23 | PSB | MPU | Interface selection |
| 24 | VOUT | Power supply | DC/DC voltage converter |
| 25 | VIN | Power supply | Input the voltage to booster |
| 26 | VDD | Power supply | Power supply    (+3.3V) for LCM |
| 27 | VSS | Power supply | Signal ground for LCM (GND) |
| 28~35 | D7-D0 | MPU | This is an 8-bit-directional data bus. |
| 36 | E | MPU | Operation (data read/write) enable signal |
| 37 | R/W | MPU | Read/write select signal |
| 38 | CSB | MPU | Chip select in parallel mode and serial interface |
| 39 | RS | MPU | Register select signal |
| 40 | RESET | MPU | External reset PIN |

# 7.Optical characteristics

STN type display module (Ta=25℃, VDD=3.3V)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Viewing angle (6 0'clock) | Left--Right | $\theta$ | Ta=25℃ | - | 60 | - | deg |
| | Top--Bottom | $\theta$ | | - | 70 | - | |
| Contrast ratio | | CR | | 3 | 5 | - | - |
| Response time | Rise | $t_r$ | Ta=25℃ | - | 150 | 250 | ms |
| | Tall | $t_f$ | | - | 200 | 300 | |

# 8.Electrical characteristics

DC characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage for LCD | $V_{DD}-V_0$ | Ta =25℃ | - | 4.3 | - | V |
| Input voltage | $V_{DD}$ | | - | 3.3 | - | |
| Supply current | $I_{DD}$ | Ta=25℃, $V_{DD}$=3.3V | - | 1.0 | 1.5 | mA |
| Input leakage current | $I_{LKG}$ | | - | - | 1.0 | uA |
| "H" level input voltage | $V_{IH}$ | | 2.2 | - | $V_{DD}$ | V |
| "L" level input voltage | $V_{IL}$ | Twice initial value or less | 0 | - | 0.6 | |
| "H" level output voltage | $V_{OH}$ | LOH=-0.25mA | 2.4 | - | - | |
| "L" level output voltage | $V_{OL}$ | LOH=1.6mA | - | - | 0.4 | |

# 9.Contrast adjust

> ➤ **V0 voltage follower value calculation**
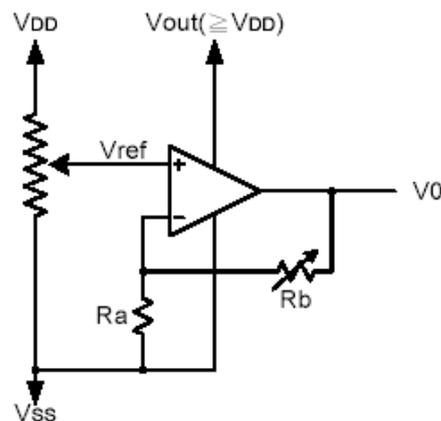


$$V0 = (1 + \frac{Rb}{Ra}) \times Vref$$

$$\text{While } Vref = V_{DD} \times (\frac{\alpha + 36}{100})$$

| C5 | C4 | C3 | C2 | C1 | C0 | α |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| ⋮ | | | | | | ⋮ |
| 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

| Rab2 | Rab1 | Rab0 | 1+Rb/Ra |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1.25 |
| 0 | 1 | 0 | 1.5 |
| 0 | 1 | 1 | 1.8 |
| 1 | 0 | 0 | 2 |
| 1 | 0 | 1 | 2.5 |
| 1 | 1 | 0 | 3 |
| 1 | 1 | 1 | 3.75 |

# 10. Timing Characteristics

( Ta = 25°C )

| Item | Signal | Symbol | Condition | VDD=2.7 to 4.5V Rating | | VDD=4.5 to 5.5V Rating | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| SCL clock frequency | SCL | $f_{SCLK}$ | | DC | 300K | DC | 400 | kHz |
| SCL clock low period | | $t_{LOW}$ | — | 2.5 | — | 1.3 | — | μs |
| SCL clock high period | | $t_{HIGH}$ | | 0.6 | — | 0.6 | — | |
| Data set-up time | SDA | $t_{SU;DAT}$ | — | 1800 | — | 700 | — | ns |
| Data hold time | | $t_{HD;DAT}$ | | 0 | 0.5 | 0 | 0.5 | μs |
| SCL,SDA rise time | SCL, SDA | $t_r$ | — | $20+0.1C_b$ | 300 | $20+0.1C_b$ | 300 | ns |
| SCL,SDA fall time | | $t_f$ | | $20+0.1C_b$ | 300 | $20+0.1C_b$ | 300 | |
| Capacitive load represent by each bus line | | $C_b$ | — | — | 400 | — | 400 | pf |
| Setup time for a repeated START condition | SDA | $t_{SU;STA}$ | — | 0.6 | — | 0.6 | — | μs |
| Start condition hold time | | $t_{HD;STA}$ | — | 1.8 | — | 1.0 | — | μs |
| Setup time for STOP condition | | $t_{SU;STO}$ | — | 0.6 | — | 0.6 | — | μs |
| Bus free time between a Stop and START condition | SCL | $t_{BUF}$ | — | 1.3 | — | 1.3 | — | μs |

**I2C interface**
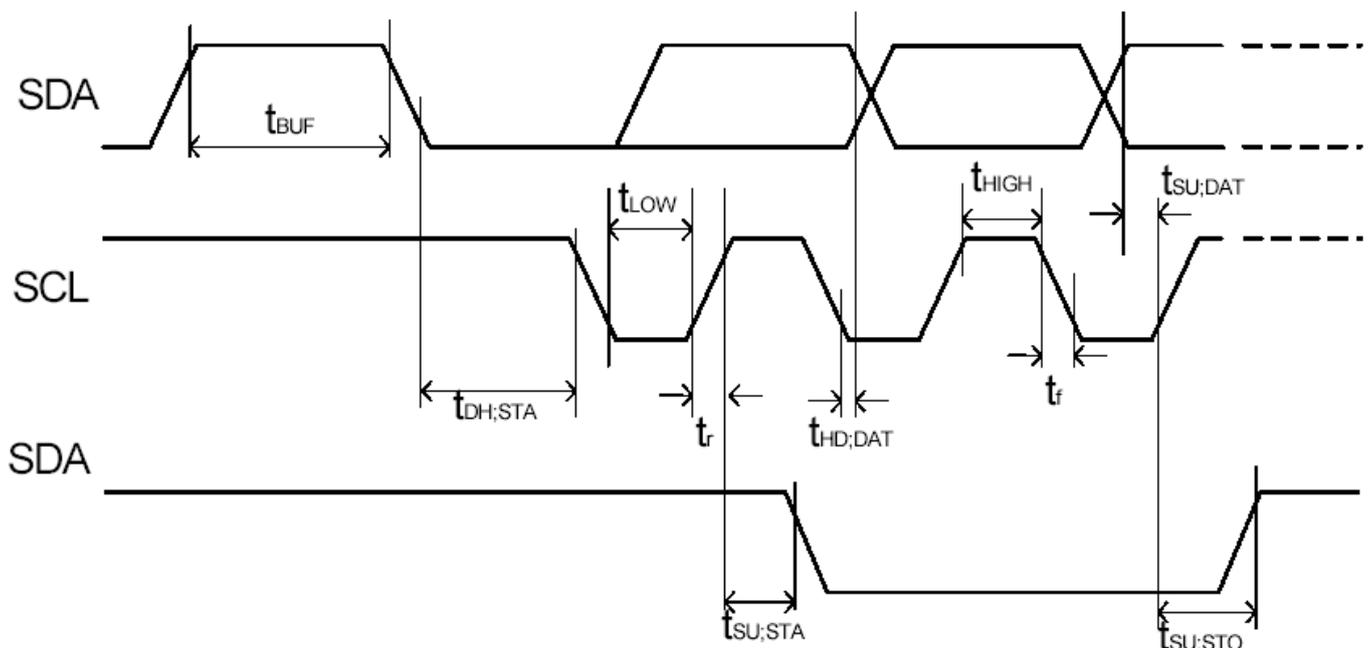
## Internal Power Supply Reset
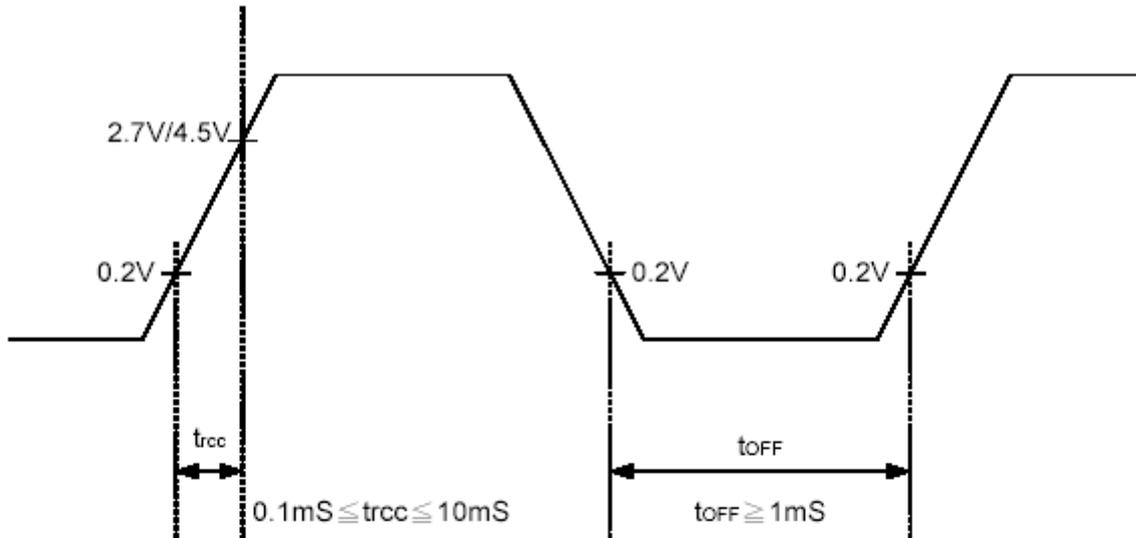


Notes:
- $t_{OFF}$ compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation, and at 2.7V for 3V operation.
- For if 2.7V/4.5V is not reached during 3V/5V operation, internal reset circuit will not operate normally.

## Hardware reset(XRESET)
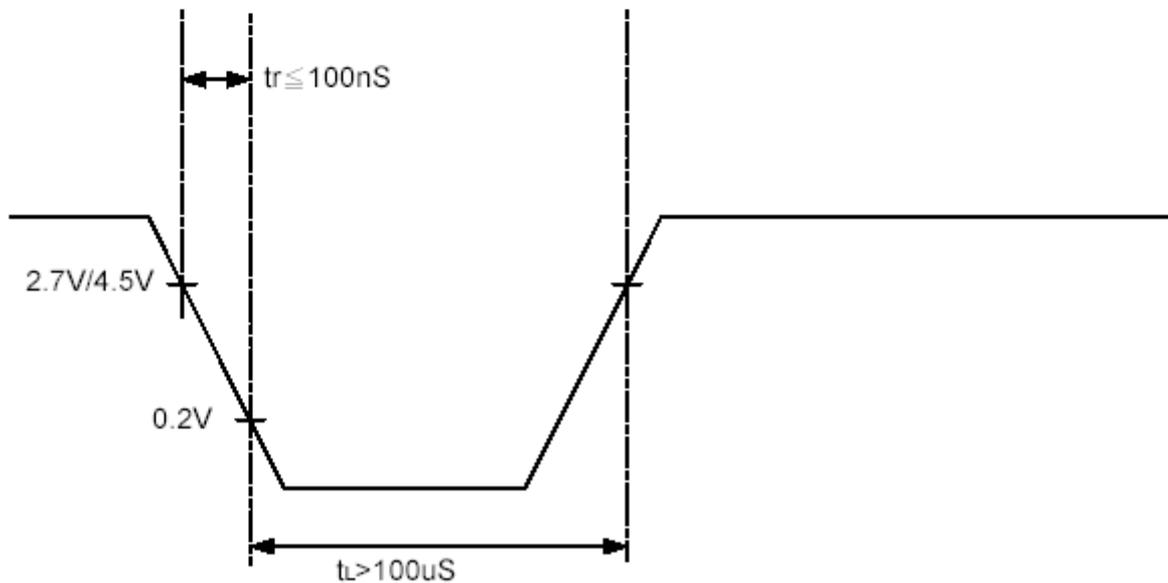
- **System Interface**

This chip has all four kinds of interface type with MPU: 4-bit bus, 8-bit bus, serial and fast I$^2$C interface. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/ICON RAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

| RS | R/W | Operation |
|----|-----|-----------|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy Flag(DB7) and address counter (DB0 ~ DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

**Table 1. Various kinds of operations according to RS and R/W bits.**

## I$^2$C interface

**It just only could write Data or Instruction to ST7036 by the IIC Interface.**
**It could not read Data or Instruction from ST7036 (except Acknowledge signal).**

SCL: serial clock input
SDA_IN: serial data input
SDA_OUT: acknowledge response output
**Slaver address could set from "0111100" to "0111111".**

The I$^2$C interface send RAM data and executes the commands sent via the I$^2$C Interface. It could send data in to the RAM. The I$^2$C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

### BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.

### START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.

### SYSTEM CONFIGURATION
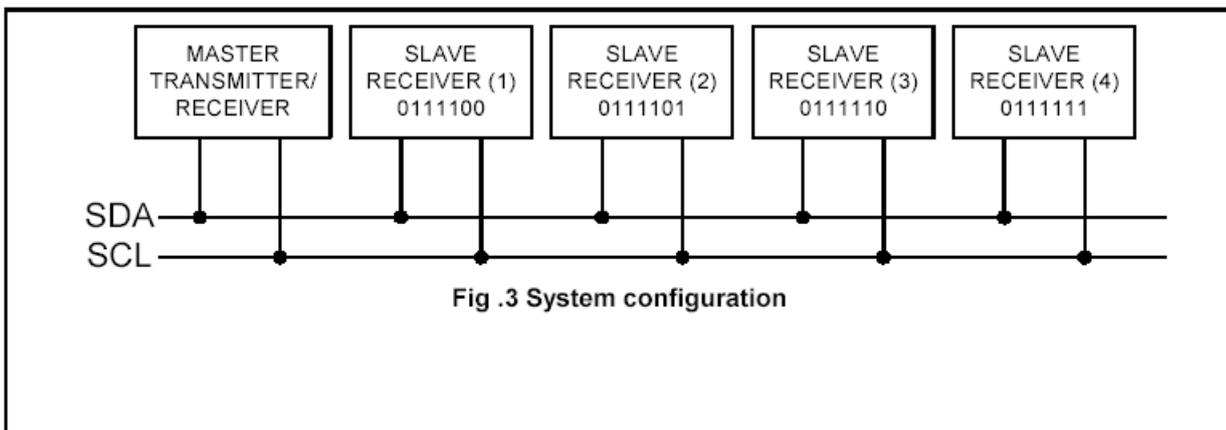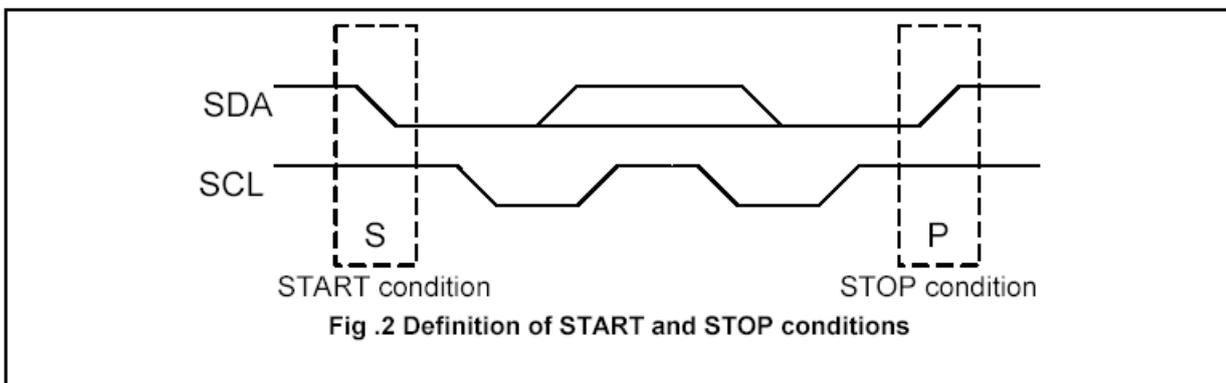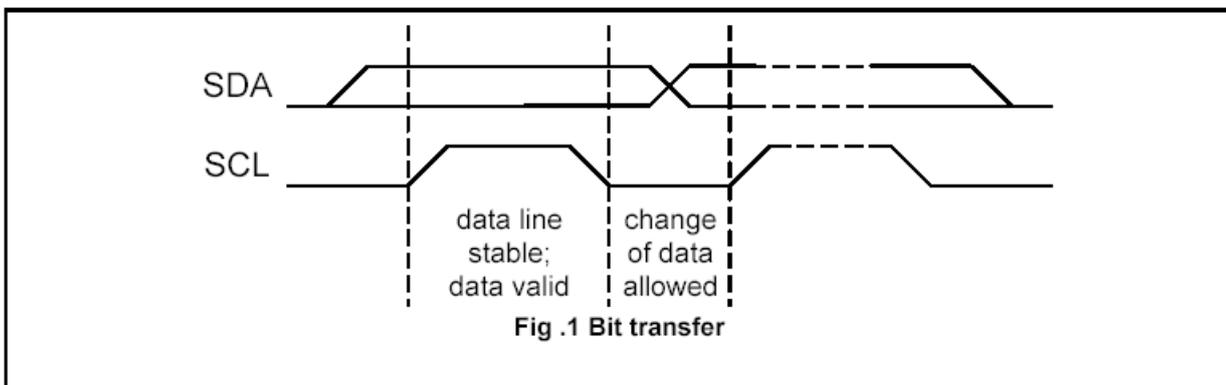
The system configuration is illustrated in Fig.3.
· Transmitter: the device, which sends the data to the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
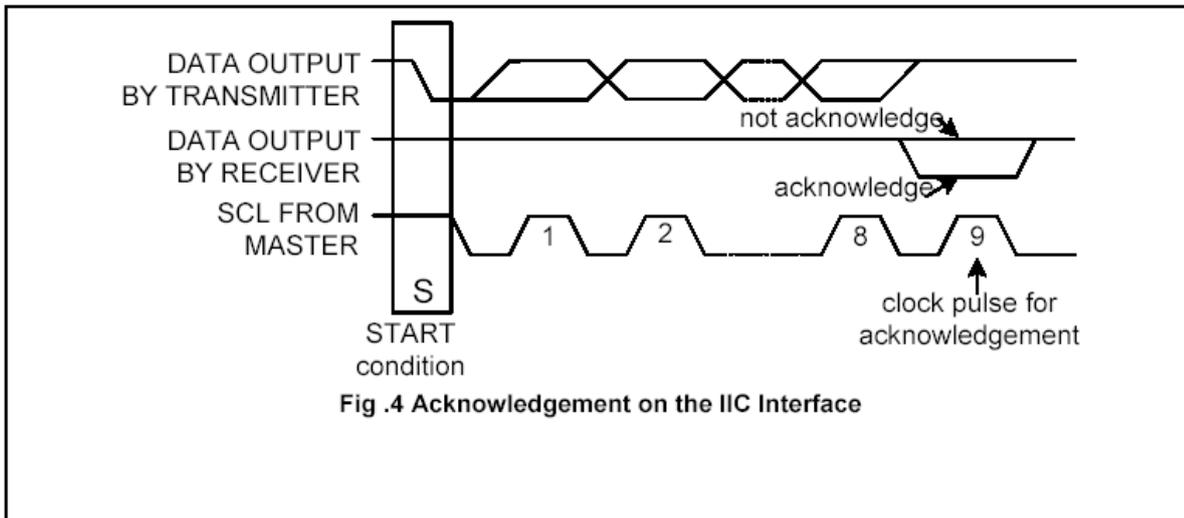· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

### ACKNOWLEDGE

**Acknowledge signal (ACK) is not BF signal in parallel interface.**

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW durir the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A maste receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STO condition. Acknowledgement on the I$^2$C Interface is illustrated in Fig.4.

**Fig .1 Bit transfer**

**Fig .2 Definition of START and STOP conditions**

**Fig .3 System configuration**

Fig .4 Acknowledgement on the IIC Interface

## I²C Interface protocol

The ST7036 supports command, data write addressed slaves on the bus.
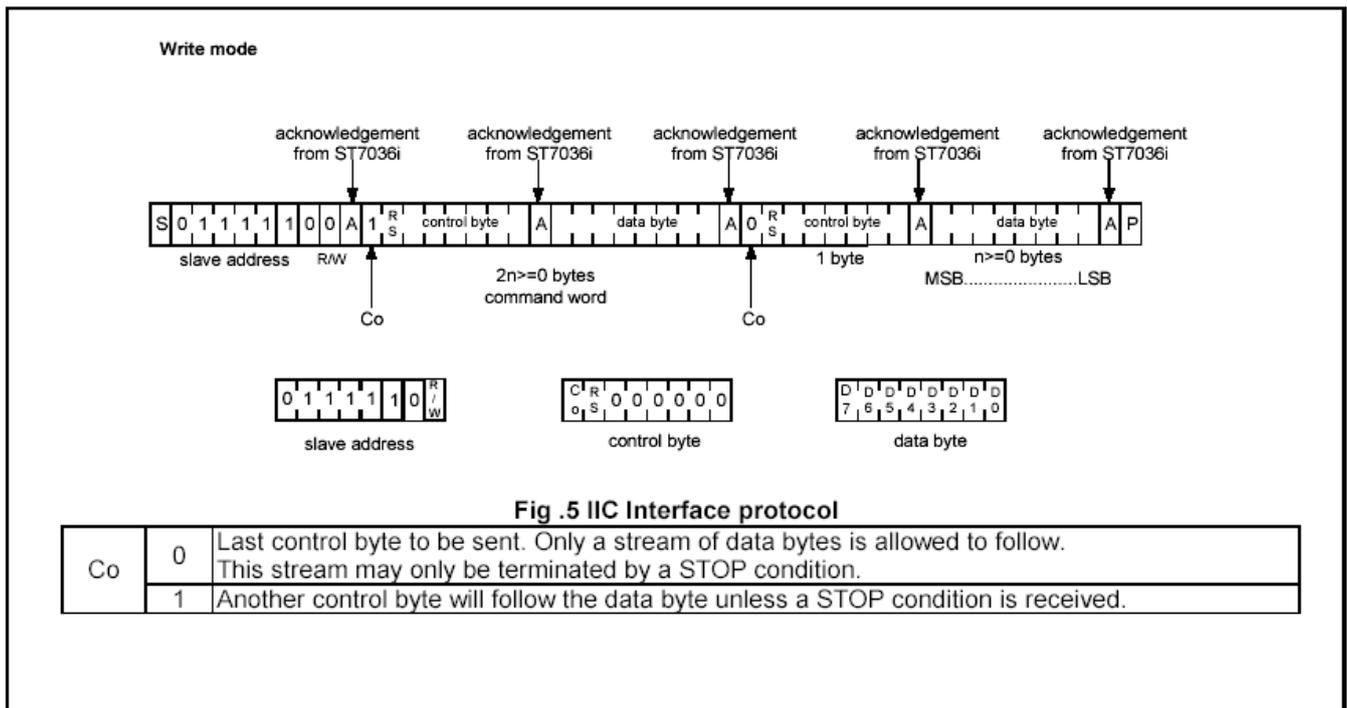
Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**100** to 0111**111**) are reserved for the ST7036. The R/W is assigned to 0 for Write only.

The I²C Interface protocol is illustrated in Fig.5.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and RS, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7036i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I²C INTERFACE-bus master issues a STOP condition (P).

Fig .5 IIC Interface protocol

| Co | 0 | Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition. |
| | 1 | Another control byte will follow the data byte unless a STOP condition is received. |

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS bit input in IIC interface.

| RS | R/W | Operation |
|----|-----|-----------|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| H | L | Data Write operation (MPU writes data into DR) |

Table 2. Various kinds of operations according to RS and R/W bits.

● **Busy Flag (BF)**
When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

● **Address Counter (AC)**
Address Counter(AC) stores DDRAM/CGRAM/ICON RAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM/ICON RAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

● **Display Data RAM (DDRAM)**

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 6 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address ($A_{DD}$) is set in the address counter (AC) as hexadecimal.

➤ **2-line display (N3=0,N = 1) (Figure 9)**

Case 1: When the number of display characters is less than 40 x 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7036 is used, 20 characters x 2 lines are displayed. See Figure 9.
When display shift operation is performed, the DDRAM address shifts. See Figure 10.

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | | 38 | 39 | 40 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | ........ | 25 | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | 45 | ........ | 65 | 66 | 67 |

**Fig. 9  2-Line Display**

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | .............. | 10 | 11 | 12 | 13 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | .............. | 50 | 51 | 52 | 53 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | .............. | 11 | 12 | 13 | 14 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | .............. | 51 | 52 | 53 | 54 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | .............. | 0F | 10 | 11 | 12 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | .............. | 4F | 50 | 51 | 52 |

**Fig. 10  2-Line by 20-Character Display Example**

## ● Character Generator ROM (CGROM)

The character generator ROM generates 5 x 8 dot character patterns from 8-bit character codes. It can generate 240/250/248/256 5 x 8 dot character patterns(select by OPR1/2 ITO pin). User-defined character patterns are also available by mask-programmed ROM.

## ● Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 5 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

| Character Code (DDRAM Data) | | | | | | | | CGRAM Address | | | | | | Character Patterns (CGRAM Data) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b5 | b4 | b3 | b2 | b1 | b0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 1 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 0 | 0 | 1 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 0 | 1 | 0 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 0 | 1 | 1 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 1 | 0 | 0 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 1 | 0 | 1 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 1 | 1 | 0 |  |  |  | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 0 |  |  |  | 1 | 1 | 1 |  |  |  | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 0 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 0 | 0 | 1 |  |  |  | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 0 | 1 | 0 |  |  |  | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 0 | 1 | 1 |  |  |  | 1 | 1 | 1 | 1 | 0 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 1 | 0 | 0 |  |  |  | 1 | 0 | 1 | 0 | 0 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 1 | 0 | 1 |  |  |  | 1 | 0 | 0 | 1 | 0 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 1 | 1 | 0 |  |  |  | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  | 0 | 0 | 1 |  |  |  | 1 | 1 | 1 |  |  |  | 0 | 0 | 0 | 0 | 0 |

**Table 5  Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)**

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. "1" for CGRAM data corresponds to display selection and "0" to non-selection,"-" Indicates no effect.
6. Different OPR1/2 ITO option can select different CGRAM size.

# 11.Instruction description

There are four categories of instructions that:

- Designate ST7036 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

> instruction table at "Normal mode"

(when "EXT" option pin connect to V$_{DD}$, the instruction set follow below table)

| Instruction | Instruction Code | | | | | | | | | | Description | Instruction Execution Time | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | OSC= 380kHz | OSC= 540kHz | OSC= 700kHz |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.08 ms | 0.76 ms | 0.59 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H"  from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.08 ms | 0.76 ms | 0.59 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 26.3 µs | 18.5 µs | 14.3 µs |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on C=1:cursor on B=1:cursor position on | 26.3 µs | 18.5 µs | 14.3 µs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 26.3 µs | 18.5 µs | 14.3 µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | X | X | X | DL: interface data is 8/4 bits N: number of line is 2/1 | 26.3 µs | 18.5 µs | 14.3 µs |
| Set CGRAM | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 | 0 | 0 |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM) | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM) | 26.3 µs | 18.5 µs | 14.3 µs |

Note:
Be sure the ST7036 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7036. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

➢ **instruction table at "Extension mode"**

(when "EXT" option pin connect to Vss, the instruction set follow below table)

| Instruction | Instruction Code | | | | | | | | | | | Description | Instruction Execution Time | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | OSC= 380kHz | OSC= 540kHz | OSC= 700kHz |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.08 ms | 0.76 ms | 0.59 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.08 ms | 0.76 ms | 0.59 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 26.3 µs | 18.5 µs | 14.3 µs |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | | D=1:entire display on C=1:cursor on B=1:cursor position on | 26.3 µs | 18.5 µs | 14.3 µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | DH | IS2 | IS1 | | DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS[2:1]: instruction table select | 26.3 µs | 18.5 µs | 14.3 µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set DDRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 | 0 | 0 |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Write data into internal RAM (DDRAM/CGRAM/ICONRAM) | 26.3 µs | 18.5 µs | 14.3 µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Read data from internal RAM (DDRAM/CGRAM/ICONRAM) | 26.3 µs | 18.5 µs | 14.3 µs |

## Instruction table 0(IS[2:1]=[0,0])

| | | | | | | | | | | | Description | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | S/C and R/L:<br>Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 26.3 µs | 18.5 µs | 14.3 µs |
| Set CGRAM | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 26.3 µs | 18.5 µs | 14.3 µs |

## Instruction table 1(IS[2:1]=[0,1])

| | | | | | | | | | | | Description | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bias Set | 0 | 0 | 0 | 0 | 0 | 1 | BS | 1 | 0 | FX | BS=1:1/4 bias<br>BS=0:1/5 bias<br>FX: fixed on high in 3-line application and fixed on low in other applications. | 26.3 µs | 18.5 µs | 14.3 µs |
| Set ICON Address | 0 | 0 | 0 | 1 | 0 | 0 | AC3 | AC2 | AC1 | AC0 | Set ICON address in address counter. | 26.3 µs | 18.5 µs | 14.3 µs |
| Power/ICON Control/ Contrast Set | 0 | 0 | 0 | 1 | 0 | 1 | Ion | Bon | C5 | C4 | Ion: ICON display on/off<br>Bon: set booster circuit on/off<br>C5,C4: Contrast set for internal follower mode. | 26.3 µs | 18.5 µs | 14.3 µs |
| Follower Control | 0 | 0 | 0 | 1 | 1 | 0 | Fon | Rab 2 | Rab 1 | Rab 0 | Fon: set follower circuit on/off<br>Rab2~0:<br>select follower amplified ratio. | 26.3 µs | 18.5 µs | 14.3 µs |
| Contrast Set | 0 | 0 | 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 | Contrast set for internal follower mode. | 26.3 µs | 18.5 µs | 14.3 µs |

## Instruction table 2(IS[2:1]=[1,0])

| | | | | | | | | | | | Description | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Double Height Position Select | 0 | 0 | 0 | 0 | 0 | 1 | UD | X | x | x | UD: Double height position select | 26.3 µs | 18.5 µs | 14.3 µs |
| Reserved | 0 | 0 | 0 | 1 | X | X | X | X | X | X | Do not use (reserved for test) | 26.3 µs | 18.5 µs | 14.3 µs |

*Instruction table 3(IS[2:1]=[1,1]):Do not use (reserved for test)*

## 12. Standard character pattern



The table shows the standard character pattern (character generator ROM) with columns labeled b7-b4 (0000 through 1111) and rows labeled b3-b0 (0000 through 1111), each cell containing a dot-matrix character image.

CGRAM/CGROM arrangement with(OPR1=0;OPR2=0)

# 13.QUALITY SPECIFICATIONS

## 13.1 Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.
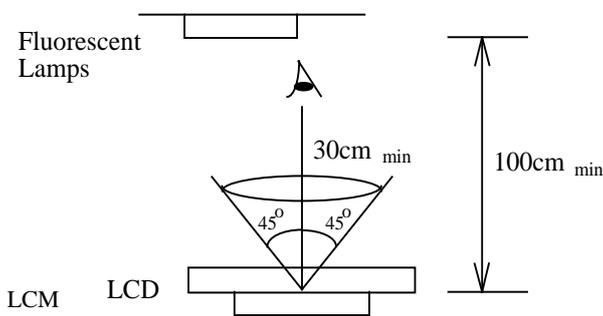


Definition of zone:
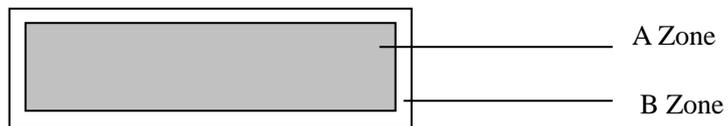


A Zone:    Active display area (minimum viewing area).
B Zone:    Non-active display area (outside viewing area).

## 13.2 Specification of quality assurance

AQL inspection standard

Sampling method: MIL-STD-105E, Level II, single sampling

Defect classification   **(Note: * is not including)**

| Classify | | Item | Note | AQL |
|---|---|---|---|---|
| Major | Display state | Short or open circuit | 1 | 0.65 |
| | | LC leakage | | |
| | | Flickering | | |
| | | No display | | |
| | | Wrong viewing direction | | |
| | | Contrast defect (dim, ghost) | 2 | |
| | | Back-light | 1,8 | |
| | Non-display | Flat cable or pin reverse | 10 | |
| | | Wrong or missing component | 11 | |
| Minor | Display state | Background color deviation | 2 | 1.0 |
| | | Black spot and dust | 3 | |
| | | Line defect, Scratch | 4 | |
| | | Rainbow | 5 | |
| | | Chip | 6 | |
| | | Pin hole | 7 | |
| | | Protruded | 12 | |
| | Polarizer | Bubble and foreign material | 3 | |
| | Soldering | Poor connection | 9 | |
| | Wire | Poor connection | 10 | |
| | TAB | Position, Bonding strength | 13 | |

**Note on defect classification**

| No. | Item | Criterion |
|---|---|---|
| 1 | Short or open circuit | Not allow |
| | LC leakage | |
| | Flickering | |
| | No display | |
| | Wrong viewing direction | |
| | Wrong Back-light | |
| 2 | Contrast defect | Refer to approval sample |
| | Background color deviation | |
| 3 | Point defect, Black spot, dust (including Polarizer) $\phi = (X+Y)/2$ |  |
| 4 | Line defect, Scratch |  |
| 5 | Rainbow | Not more than two color changes across the viewing area. |

Table for No. 3:
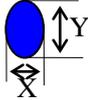
| Point Size | Acceptable Qty. |
|---|---|
| $\phi \leq 0.10$ | Disregard |
| $0.10 < \phi \leq 0.20$ | 3 |
| $0.20 < \phi \leq 0.25$ | 2 |
| $0.25 < \phi \leq 0.30$ | 1 |
| $\phi > 0.30$ | 0 |

Unit: mm

Table for No. 4:

| Line | | Acceptable Qty. |
|---|---|---|
| L | W | |
| --- | $0.015 \geq W$ | Disregard |
| $3.0 \geq L$ | $0.03 \geq W$ | 2 |
| $2.0 \geq L$ | $0.05 \geq W$ | |
| $1.0 \geq L$ | $0.1 > W$ | 1 |
| --- | $0.05 < W$ | Applied as point defect |

Unit: mm

| No | Item | Criterion |
|---|---|---|

**6** — Chip

Remark:
- X: Length direction
- Y: Short direction
- Z: Thickness direction
- t: Glass thickness
- W: Terminal Width
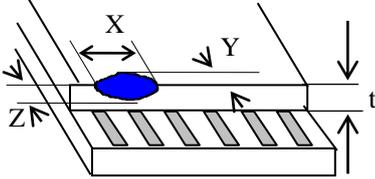
Acceptable criterion

| X | Y | Z |
|---|---|---|
| $\leqslant 2$ | 0.5mm | $\leqslant t/2$ |
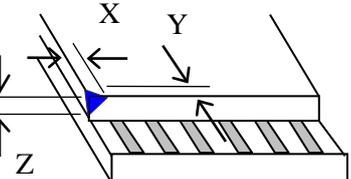
Acceptable criterion

| X | Y | Z |
|---|---|---|
| $\leqslant 2$ | 0.5mm | $\leqslant t$ |
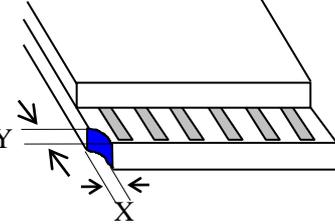
Acceptable criterion

| X | Y | Z |
|---|---|---|
| $\leqslant 3$ | $\leqslant 2$ | $\leqslant t$ |
| shall not reach to ITO | | |
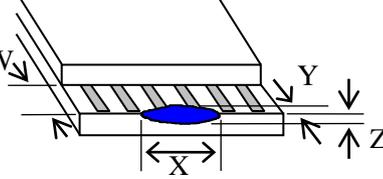
Acceptable criterion

| X | Y | Z |
|---|---|---|
| Disregard | $\leqslant 0.2$ | $\leqslant t$ |

Acceptable criterion

| X | Y | Z |
|---|---|---|
| $\leqslant 5$ | $\leqslant 2$ | $\leqslant t/3$ |

| No. | Item | Criterion |
|---|---|---|
| 7 | Segment pattern<br>W = Segment width<br>$\phi = (X+Y)/2$ | (1) Pin hole<br><br>$\phi < 0.10\text{mm}$ is acceptable.<br><br><br><br>| Point Size | Acceptable Qty |<br>\|---\|---\|<br>\| $\phi \leq 1/4W$ \| Disregard \|<br>\| $1/4W < \phi \leq 1/2W$ \| 1 \|<br>\| $\phi > 1/2W$ \| 0 \|<br><br>Unit: mm |
| 8 | Back-light | (1) The color of backlight should correspond its specification.<br>(2) Not allow flickering |
| 9 | Soldering | (1) Not allow heavy dirty and solder ball on PCB.<br>(The size of dirty refer to point and dust defect)<br>(2) Over 50% of lead should be soldered on Land.<br><br> |
| 10 | Wire | (1) Copper wire should not be rusted<br>(2) Not allow crack on copper wire connection.<br>(3) Not allow reversing the position of the flat cable.<br>(4) Not allow exposed copper wire inside the flat cable. |
| 11* | PCB | (1) Not allow screw rust or damage.<br>(2) Not allow missing or wrong putting of component. |

| No | Item | Criterion |
|---|---|---|
| 12 | Protruded<br><br>W: Terminal Width | <br>Acceptable criteria:<br>$Y \leq 0.4$ |
| 13 | TAB | 1. Position<br><br><br>$W1 \leq 1/3W$<br>$H1 \leq 1/3H$<br><br>2  TAB bonding strength test<br><br><br><br>P (=F/TAB bonding width) $\geq 650$gf/cm ,(speed rate: 1mm/min)<br>5pcs per SOA (shipment) |
| 14 | Total no. of acceptable Defect | A. Zone<br><br>Maximum 2 minor non-conformities per one unit.<br><br>Defect distance: each point to be separated over 10mm<br><br>B. Zone<br><br>It is acceptable when it is no trouble for quality and assembly<br><br>in customer's end product. |
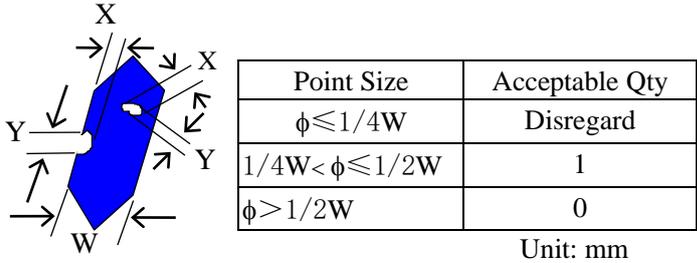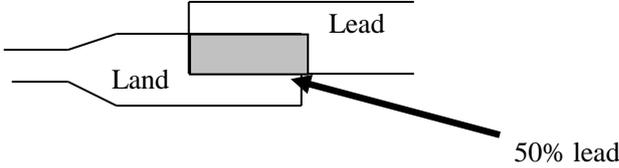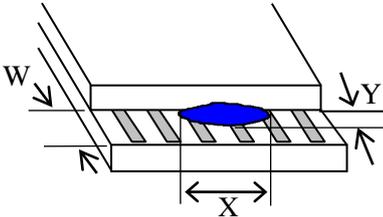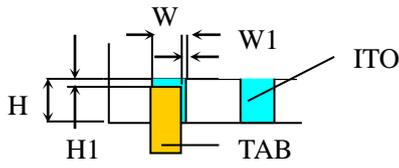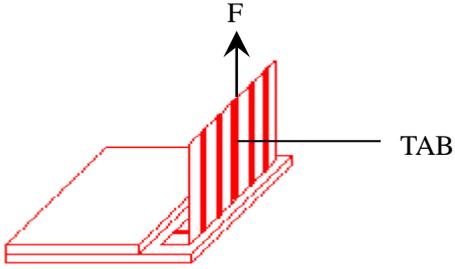
## 13.3 Reliability of LCM
Reliability test condition:

| Item | Condition | Time (hrs) | Assessment |
|---|---|---|---|
| High temp. Storage | 80°C | 48 | |
| High temp. Operating | 70°C | 48 | |
| Low temp. Storage | -30°C | 48 | No abnormalities |
| Low temp. Operating | -20°C | 48 | in functions |
| Humidity | 40°C/ 90%RH | 48 | and appearance |
| Temp. Cycle | 0°C ← 25°C →50°C<br>(30 min ← 5 min → 30min) | 10cycles | |

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20$\pm$8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

## 13.4 Precaution for using LCD/LCM
LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

**General Precautions:**
1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting Focus Display Solutions, inc.
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

**Static Electricity Precautions:**
1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or

defective insulation of terminals.
4.  The modules should be kept in anti-static bags or other containers resistant to static for storage.
5.  Only properly grounded soldering irons should be used.
6.  If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7.  The normal static prevention measures should be observed for work clothes and working benches.
8.  Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

## Soldering Precautions:

1.  Soldering should be performed only on the I/O terminals.
2.  Use soldering irons with proper grounding and no leakage.
3.  Soldering temperature: 280°C$\pm$10°C
4.  Soldering time: 3 to 4 second.
5.  Use eutectic solder with resin flux filling.
6.  If flux is used, the LCD surface should be protected to avoid spattering flux.
7.  Flux residue should be removed.

## Operation Precautions:

1.  The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2.  Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3.  Driving voltage should be kept within specified range; excess voltage will shorten display life.
4.  Response time increases with decrease in temperature.
5.  Display color may be affected at temperatures above its operational range.
6.  Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7.  For long-term storage over 40°C is required, the relative humidity should be kept below 60%,and avoid direct sunlight.