ANALOG DEVICES

14-Bit, 32 MSPS TxDAC+™ with 4× Interpolation Filters

AD9774

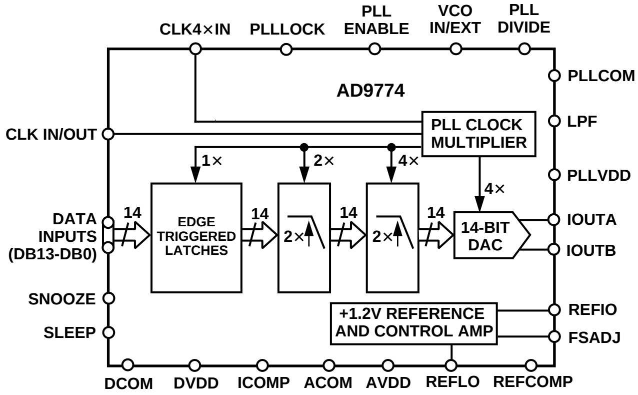
FEATURES

- Single 3 V or 5 V Supply
- 14-Bit DAC Resolution and Input Data Width
- 32 MSPS Input Data Rate at 5 V
- 13.5 MHz Reconstruction Bandwidth
- 12 ENOBS @ 1 MHz
- 77 dBc SFDR @ 5 MHz
- 4× Interpolation Filter
  - 69 dB Image Rejection
  - 84% Passband to Nyquist Ratio
  - 0.002 dB Passband Ripple
  - 23 3/4 Cycle Latency
- Internal 4× Clock Multiplier
- On-Chip 1.20 V Reference
- 44-Lead MQFP Package

APPLICATIONS

- Communication Transmit Channel:
  - Wireless Basestations
  - ADSL/HFC Modems
- Direct Digital Synthesis (DDS)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9774 is a single supply, oversampling, 14-bit digital-to-analog converter (DAC) optimized for waveform reconstruction applications requiring exceptional dynamic range. Manufactured on an advanced CMOS process, it integrates a complete, low distortion 14-bit DAC with a 4× digital interpolation filter and clock multiplier. The two-stage, 4× digital interpolation filter provides more than a six-fold reduction in the complexity of the analog reconstruction-filter. It does so by multiplying the input data rate by a factor of four while simultaneously suppressing the original inband images by more than 69 dB. The on-chip clock multiplier provides all the necessary clocks. The AD9774 can reconstruct full-scale waveforms having bandwidths as high as 13.5 MHz when operating at an input data rate of 32 MSPS and a DAC output rate of 128 MSPS.

The 14-bit DAC provides differential current outputs to support differential or single-ended applications. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The differential current outputs may be fed into a transformer or tied directly to an output resistor to provide two complementary, single-ended voltage outputs. A differential op amp topology can also be used to obtain a single-ended output voltage. The output voltage compliance range is nominally 1.25 V.

Edge-triggered input latches, a 4× clock multiplier, and a temperature compensated bandgap reference have also been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3 V and +5 V CMOS logic families. TTL logic levels can also be accommodated by reducing the AD9774 digital supply.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9774 can be driven by the on-chip reference or by a variety of external reference voltages. The full-scale current of the AD9774 can be adjusted over a 2 mA to 20 mA range, thus providing additional gain ranging capabilities.

The AD9774 is available in a 44-lead MQFP package. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. On-Chip 4× interpolation filter eases analog reconstruction filter requirements by suppressing the first three images by 69 dB.
2. Low glitch and fast settling time provide outstanding dynamic performance for waveform reconstruction or digital synthesis requirements, including communications.
3. On-chip, edge-triggered input CMOS latches interface readily to CMOS and TTL logic families. The AD9774 can support input data rates up to 32 MSPS.
4. A temperature compensated, 1.20 V bandgap reference is included on-chip, providing a complete DAC solution. An external reference may also be used.
5. The current output(s) of the AD9774 can easily be configured for various single-ended or differential circuit topologies.
6. On-chip clock multiplier generates all the high-speed clocks required by the internal interpolation filters. Both 2× and 4× clocks are generated from the lower rate data clock supplied by the user.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700   World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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AD9774–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, PLLVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = +25°C		±4		LSB
T_{MIN} to T_{MAX}				
Differential Nonlinearity (DNL)				
T_A = +25°C		±3		LSB
T_{MIN} to T_{MAX}				
Monotonicity (12-Bit)	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE			
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	–7	±1	+7	% of FSR
Gain Error (With Internal Reference)	+7.5	±1	+7.5	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range		1.25		V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		1		µA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±100		ppm of FSR/°C
POWER SUPPLY				
AVDD				
Voltage Range[4]	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})		26.5	32	mA
Analog Supply Current in SLEEP Mode (I_{AVDD})		3.2	5	mA
PLLVDD				
Voltage Range	2.7	5.0	5.5	V
Clock Multiplier Supply Current (I_{PLLVDD})		13	17	mA
DVDD				
Voltage Range	2.7	5.0	5.5	V
Digital Supply Current at 5 V (I_{DVDD})[5]		123.0	140.0	mA
Digital Supply Current at 5 V in SNOOZE Mode (I_{DVDD})		42.0	50.0	mA
Digital Supply Current at 3 V (I_{DVDD})[5]		62.0		mA
Nominal Power Dissipation				
AVDD and DVDD at 3 V[6]		415		mW
AVDD and DVDD at 5 V[6]		1125		mW
Power Supply Rejection Ratio (PSRR)[7] – AVDD	–0.2		+0.2	% of FSR/V
Power Supply Rejection Ratio (PSRR)[7] – PLLVDD	–0.025		+0.025	% of FSR/V
Power Supply Rejection Ratio (PSRR)[7] – DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

[1] Measured at IOUTA driving a virtual ground.

[2] Nominal full-scale current, IOUTFS, is 32 × the I_{REF} current.

[3] Use an external amplifier to drive any external load.

[4] For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.

[5] Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1.01 MHz.

[6] Measured as unbuffered voltage output into 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 32 MSPS and f_{OUT} = 12.8 MHz.

[7] ±5% power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, PLLVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate w/DVDD = 5 V	128			MSPS
w/DVDD = 3 V	100	128		MSPS
Output Settling Time (t_{ST}) (to 0.025%)		35		ns
Output Propagation Delay (t_{PD})		55		Clocks[1]
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		$\text{pA}/\sqrt{\text{Hz}}$[2]
AC LINEARITY TO NYQUIST				
Spurious-Free Dynamic Range (SFDR) to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.01 MHz				
0 dBFS Output		79		dB
–6 dBFS Output		86		dB
–12 dBFS Output		75		dB
–18 dBFS Output		75		dB
f_{CLOCK} = 32 MSPS; f_{OUT} = 1.01 MHz		78		dB
f_{CLOCK} = 32 MSPS; f_{OUT} = 5.01 MHz		77		dB
f_{CLOCK} = 32 MSPS; f_{OUT} = 10.01 MHz		79		dB
f_{CLOCK} = 32 MSPS; f_{OUT} = 13.01 MHz		78		dB
Total Harmonic Distortion (THD)				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.01 MHz; 0 dBFS		–75		dB
Signal-to-Noise Ratio (SNR)				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.01 MHz; 0 dBFS		76		dB

NOTES

[1] Propagation delay is delay from data input to DAC update.

[2] Measured single-ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, PLLVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)		2.5		ns
Input Hold Time (t_H)		1.5		ns
Latch Pulsewidth (t_{LPW})		4		ns

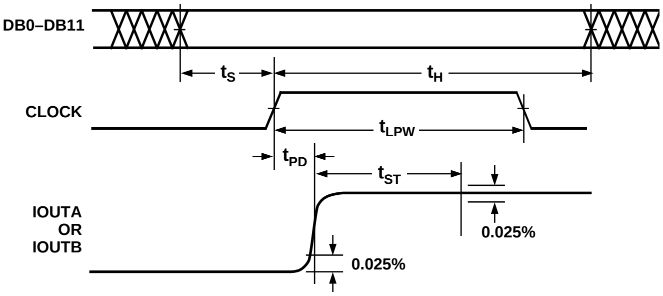


Figure 1. Timing Diagram

AD9774–SPECIFICATIONS

DIGITAL FILTER SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = +2.7 V to +5.5 V, DVDD = +2.7 V to +5.5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
MAXIMUM INPUT CLOCK RATE (f_{CLOCK})				
DVDD = 5 V	32			MSPS
DVDD = 3 V	25	32		MSPS
DIGITAL FILTER CHARACTERISTICS				
Passband Width[1]: 0.005 dB		0.410		f_{OUT}/f_{CLOCK}
Passband Width: 0.01 dB		0.414		f_{OUT}/f_{CLOCK}
Passband Width: 0.1 dB		0.420		f_{OUT}/f_{CLOCK}
Passband Width: –3 dB		0.482		f_{OUT}/f_{CLOCK}
LINEAR PHASE (FIR IMPLEMENTATION)				
STOPBAND REJECTION				
0.591 f_{CLOCK} to 3.419 f_{CLOCK}		–69.5		dB
0.591 f_{CLOCK} to 1.409 f_{CLOCK}		–79.5		dB
GROUP DELAY[2]		38		Input Clocks
IMPULSE RESPONSE DURATION				
–40 dB		53		Input Clocks
–60 dB		62		Input Clocks

NOTES

[1] Excludes sinx/x characteristic of DAC.

[2] Defined as the number of data clock cycles between impulse input and peak of output response.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
PLLVDD	PLLCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
PLLCOM	ACOM	–0.3	+0.3	V
PLLCOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
PLLVDD	DVDD	–0.3	+6.5	V
PLLVDD	AVDD	–0.3	+6.5	V
CLKIN, CLK4×IN	DVDD	–0.3	+6.5	V
SLEEP, SNOOZE	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
PLL DIVIDE, LPF	ACOM	–0.3	PLLVDD + 0.3	V
PLLLOCK	ACOM	–0.3	PLLVDD + 0.3	V
VCO IN/EXT	ACOM	–0.3	PLLVDD + 0.3	V
IOUTA/IOUTB	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
FSADJ	ACOM	–0.3	AVDD + 0.3	V
ICOMP	ACOM	–0.3	AVDD + 0.3	V
REFCOM	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9774AS	–40°C to +85°C	44-Lead MQFP	S-44
AD9774EB		Evaluation Board	

*S = Metric Quad Flatpack.

THERMAL CHARACTERISTIC

Thermal Resistance

44-Lead MQFP

θ_{JA} = 53.2°C/W

θ_{JC} = 19°C/W

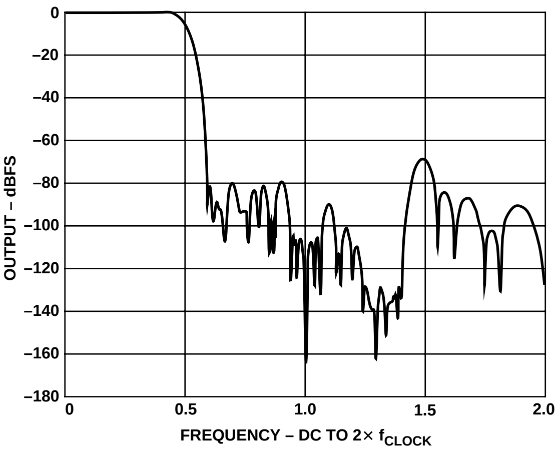


Figure 2a. FIR Filter Frequency Response

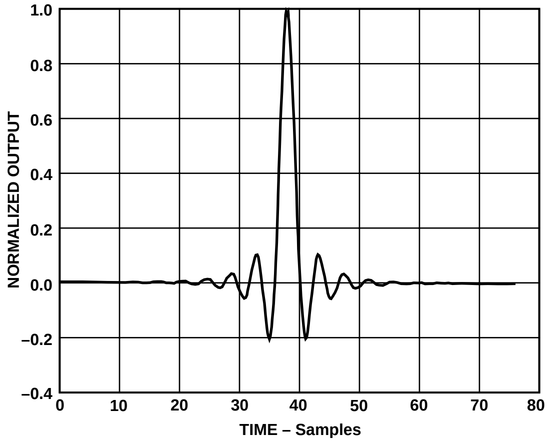


Figure 2b. FIR Filter Impulse Response

Table I. Integer Filter Coefficients for First Stage Interpolation Filter (55-Tap Halfband FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	–1
H(2)	H(54)	0
H(3)	H(53)	3
H(4)	H(52)	0
H(5)	H(51)	–7
H(6)	H(50)	0
H(7)	H(49)	15
H(8)	H(48)	0
H(9)	H(47)	–28
H(10)	H(46)	0
H(11)	H(45)	49
H(12)	H(44)	0
H(13)	H(43)	–81
H(14)	H(42)	0
H(15)	H(41)	128
H(16)	H(40)	0
H(17)	H(39)	–196
H(18)	H(38)	0
H(19)	H(37)	295
H(20)	H(36)	0
H(21)	H(35)	–447
H(22)	H(34)	0
H(23)	H(33)	706
H(24)	H(32)	0
H(25)	H(31)	–1274
H(26)	H(30)	0
H(27)	H(29)	3976
H(28)		6276

Table II. Integer Filter Coefficients for Second Stage Interpolation Filter (23-Tap Halfband FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	–6
H(2)	H(22)	0
H(3)	H(21)	37
H(4)	H(20)	0
H(5)	H(19)	–125
H(6)	H(18)	0
H(7)	H(17)	316
H(8)	H(16)	0
H(9)	H(15)	–736
H(10)	H(14)	0
H(11)	H(13)	2562
H(12)		4096

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9774 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

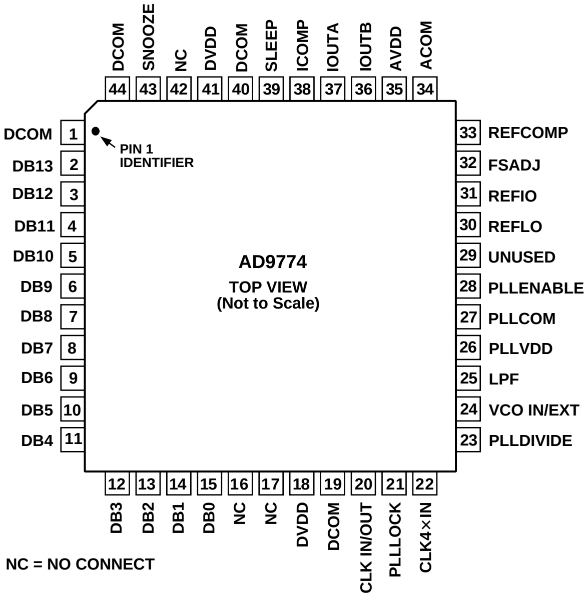
WARNING!

ESD SENSITIVE DEVICE

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1, 19, 40, 44	DCOM	Digital Common.
2	DB13	Most Significant Data Bit (MSB).
3–14	DB12–DB1	Data Bits 1–12.
15	DB0	Least Significant Data Bit (LSB).
16, 17, 42	NC	No Internal Connection.
18, 41	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
20	CLK IN/OUT	Clock Input when PLL Clock Multiplier enabled. Clock Output when PLL Clock Multiplier disabled. Data latched on rising edge.
21	PLLLOCK	Phase Lock Loop Lock Signal. Active High indicates PLL is locked to input clock.
22	CLK4×IN	External 4× Clock Input when PLL is disabled. No Connect when internal PLL is active.
23	PLLDIVIDE	PLL Range Control Pin. Connect to PLLCOM if CLKIN is above 10 MSPS. Connect to PLLVDD if CLKIN is between 10 MSPS and 5.5 MSPS.
24	VCO IN/EXT	Internal Voltage Controlled Oscillator (VCO) Enable/Disable Pin. Connect to PLLVDD to enable VCO. Connect to PLLCOM to disable VCO and drive CLK4×IN with external VCO output.
25	LPF	PLL Loop Filter Node. Connect to *externa*l VCO control input if *internal* VCO disabled.
26	PLLVDD	Phase Lock Loop (PLL) Supply Voltage (+2.7 V to +5.5 V). Must be set to similar voltage as DVDD.
27	PLLCOM	Phase Lock Loop Common.
28	PLLENABLE	Phase Lock Loop Enable. Connect to PLLVDD to enable. Connect to PLLCOM to disable.
29	UNUSED	Factory Test. Leave Open.
30	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
31	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., tie REFLO to ACOM). Requires 0.1 µF capacitor to ACOM when internal reference activated.
32	FSADJ	Full-Scale Current Output Adjust.
33	REFCOMP	Noise Reduction Node. Add 0.1 µF to AVDD.
34	ACOM	Analog Common.
35	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
36	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
37	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
38	ICOMP	Internal bias node for switch driver circuitry. Decouple to ACOM with 0.1 µF capacitor.
39	SLEEP	Power-Down Control Input. Active High. Connect to DCOM if not used.
43	SNOOZE	SNOOZE Control Input. Deactivates 4× interpolation filter to reduce digital power consumption only. Active High. Connect to DCOM if not used.

PIN CONFIGURATION


DCOM 44
SNOOZE 43
NC 42
DVDD 41
DCOM 40
SLEEP 39
ICOMP 38
IOUTA 37
IOUTB 36
AVDD 35
ACOM 34
DCOM 1
DB13 2
DB12 3
DB11 4
DB10 5
DB9 6
DB8 7
DB7 8
DB6 9
DB5 10
DB4 11
PIN 1 IDENTIFIER
AD9774
TOP VIEW
(Not to Scale)
33 REFCOMP
32 FSADJ
31 REFIO
30 REFLO
29 UNUSED
28 PLLENABLE
27 PLLCOM
26 PLLVDD
25 LPF
24 VCO IN/EXT
23 PLLDIVIDE
12 DB3
13 DB2
14 DB1
15 DB0
16 NC
17 NC
18 DVDD
19 DCOM
20 CLK IN/OUT
21 PLLLOCK
22 CLK4×IN

NC = NO CONNECT

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s, minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Signal-to-Noise Ratio (SNR)
S/N is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Passband
Frequency band in which any input applied therein passes unattenuated to the DAC output.

Stopband Rejection
The amount of attenuation of a frequency outside the passband applied to the DAC, relative to a full-scale signal applied at the DAC input within the passband.

Group Delay
Number of input clocks between an impulse applied at the device input and peak DAC output current.

Impulse Response
Response of the device to an impulse applied to the input.

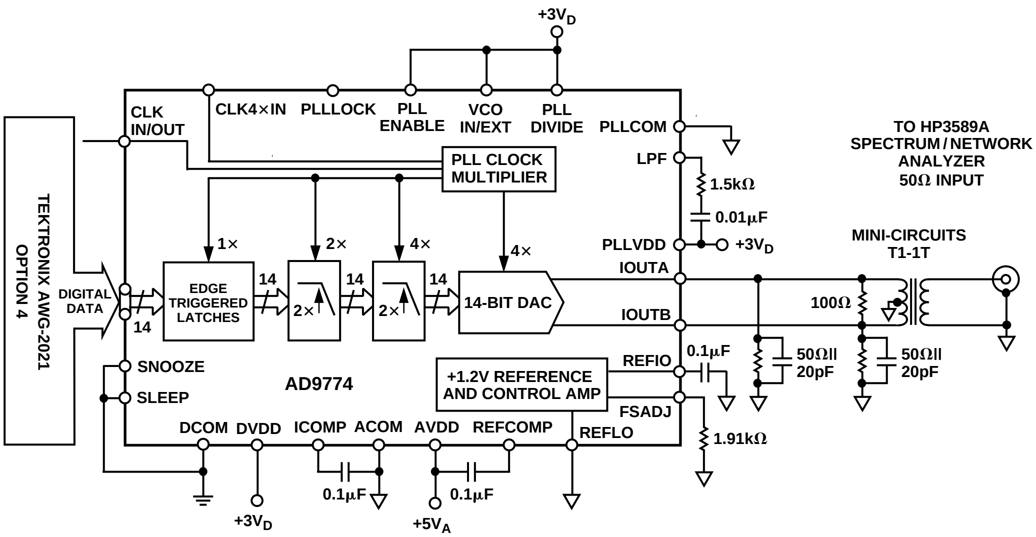

+3VD
CLK IN/OUT
CLK4×IN
PLLLOCK
PLL ENABLE
VCO IN/EXT
PLL DIVIDE
PLLCOM
LPF
PLL CLOCK MULTIPLIER
1.5kΩ
0.01μF
PLLVDD
+3VD
TO HP3589A SPECTRUM / NETWORK ANALYZER 50Ω INPUT
MINI-CIRCUITS T1-1T
TEKTRONIX AWG-2021 OPTION 4
DIGITAL DATA
14
1×
2×
4×
4×
EDGE TRIGGERED LATCHES
14
2×
14
2×
14
14-BIT DAC
IOUTA
IOUTB
100Ω
50Ω||20pF
50Ω||20pF
SNOOZE
SLEEP
AD9774
REFIO
0.1μF
+1.2V REFERENCE AND CONTROL AMP
FSADJ
REFLO
1.91kΩ
DCOM
DVDD
ICOMP
ACOM
AVDD
REFCOMP
0.1μF
0.1μF
+3VD
+5VA

Figure 3. Basic AC Characterization Test Setup

Typical AC Characterization Curves

(AVDD = +5 V, PLLVDD = +3 V, DVDD = +3 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, unless otherwise noted. Note: PLLVDD = +5 V and DVDD = +5 V for Figures 4, 5 and 6.)

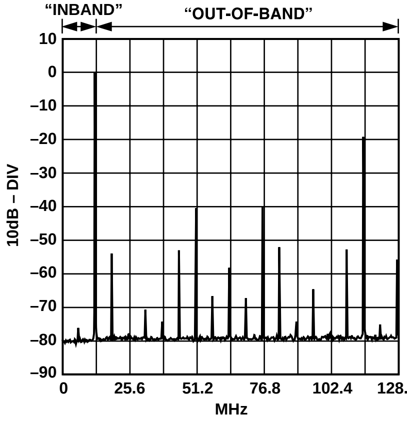


Figure 4. Single Tone Spectral Plot @ 32 MSPS w/f_{OUT} = 12.8 MHz (DC to 4 × CLKIN)

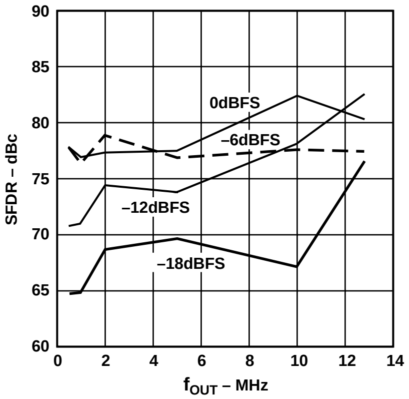


Figure 5. "Inband" SFDR vs. f_{OUT} @ 32 MSPS (DC to CLKIN/2)

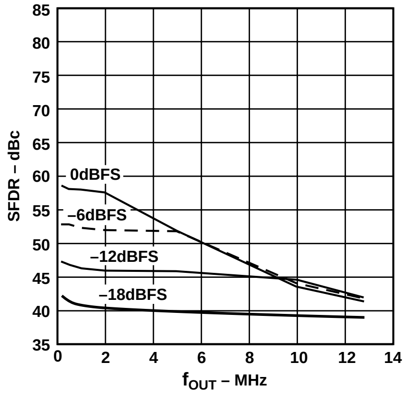


Figure 6. "Out-of-Band" SFDR vs. f_{OUT} @ 32 MSPS (CLKIN/2 to 3 1/2 CLKIN)

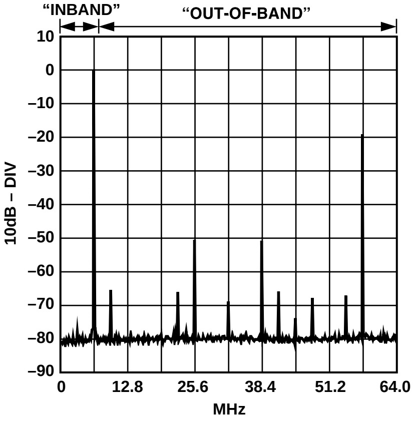


Figure 7. Single Tone Spectral Plot @ 16 MSPS w/f_{OUT} = 6.4 MHz (DC to 4 × CLKIN)

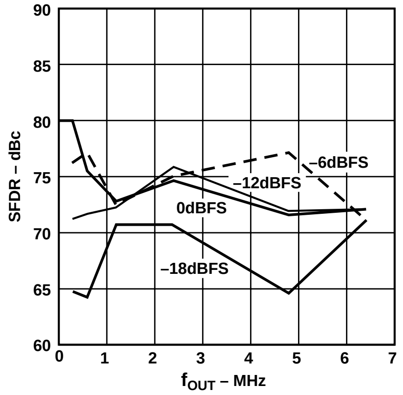


Figure 8. "Inband" SFDR vs. f_{OUT} @ 16 MSPS (DC to CLKIN/2)

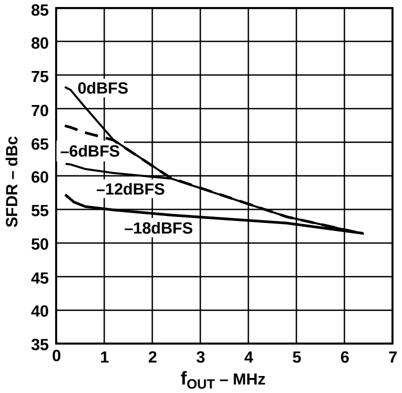


Figure 9. "Out-of-Band" SFDR vs. f_{OUT} @ 16 MSPS (CLKIN/2 to 3 1/2 CLKIN)

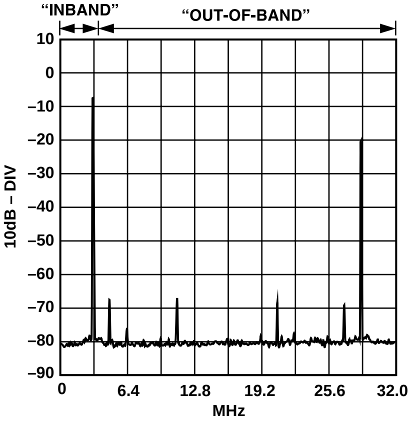


Figure 10. Single Tone Spectral Plot f_{OUT} @ 8 MSPS w/f_{OUT} = 3.2 MHz (DC to 4 × CLKIN)

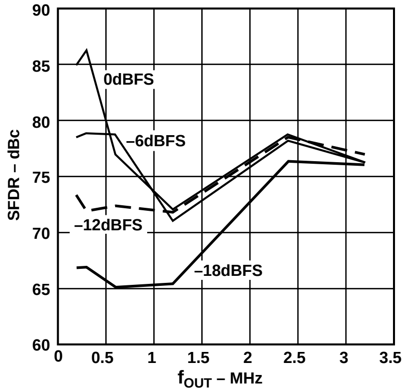


Figure 11. "Inband" SFDR vs. f_{OUT} @ 8 MSPS (DC to CLKIN/2)

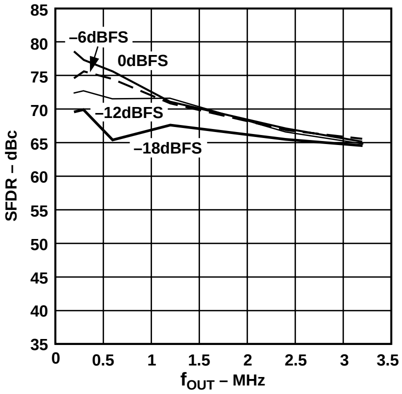


Figure 12. "Out-of-Band" SFDR vs. f_{OUT} @ 8 MSPS (CLKIN/2 to 3 1/2 CLKIN)

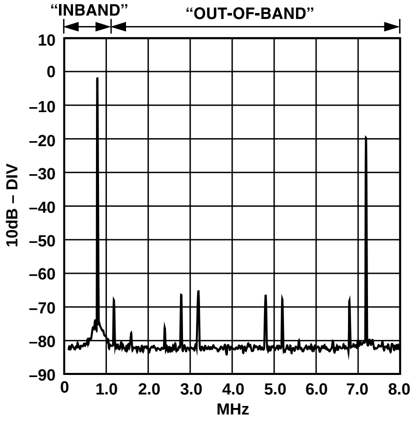


Figure 13. Single Tone Spectral Plot @ 2 MSPS w/f_{OUT} = 800 kHz (DC to 4 × CLKIN)

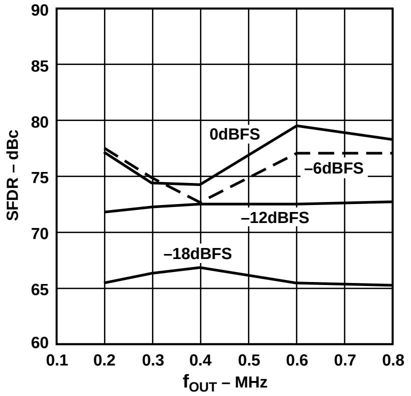


Figure 14. "Inband" SFDR vs. f_{OUT} @ 2 MSPS (DC to CLKIN/2)

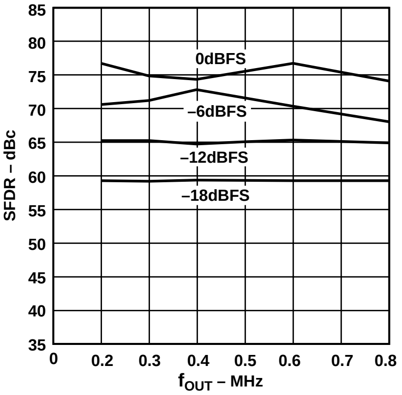


Figure 15. "Out-of-Band" SFDR vs. f_{OUT} @ 2 MSPS (CLKIN/2 to 3 1/2 CLKIN)

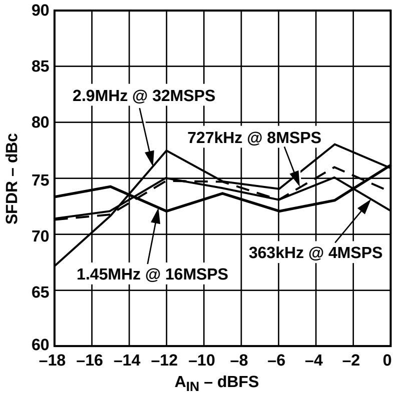


Figure 16. "In-Band" Single Tone SFDR vs. A_{IN} @ $f_{OUT} = f_{CLOCK}/7$ (DC to CLKIN/2)

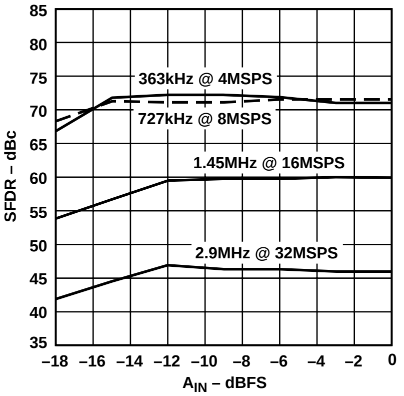


Figure 17. Out-of-Band Single Tone SFDR vs. A_{IN} @ $f_{OUT} = f_{CLOCK}/7$ (DC to 3 1/2 CLKIN)

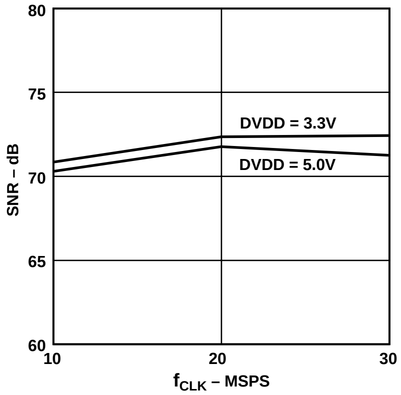


Figure 18. SNR vs. f_{CLKIN} @ f_{OUT} = 2 MHz (DC to CLKIN/2)

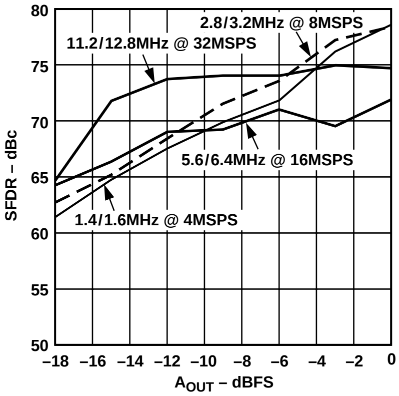


Figure 19. "In-Band" Two Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/2.7$ (DC to CLKIN/2)

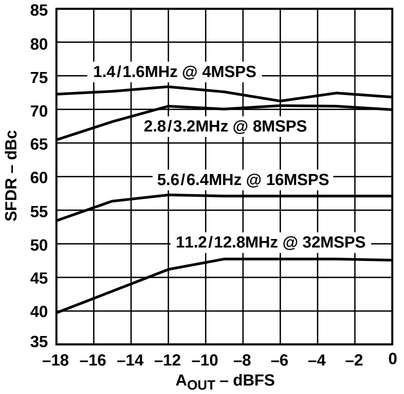


Figure 20. "Out-of-Band" Two Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/2.7$ (DC to 3 1/2 CLKIN)

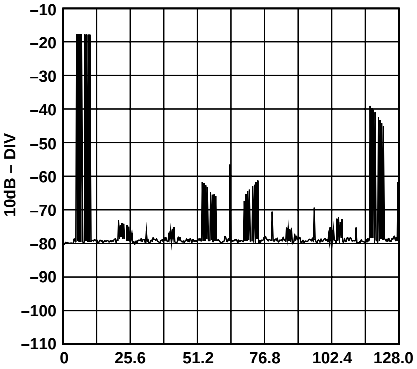


Figure 21. Multitone Spectral Plot @ 32 MSPS (DC to 4 × CLKIN)

FUNCTIONAL DESCRIPTION

Figure 22 shows a simplified block diagram of the AD9774. The AD9774 is a complete, 4× oversampling, 14-bit DAC that includes two cascaded 2× interpolation filters, a phase-locked loop (PLL) clock multiplier, and a 1.20 Volt bandgap voltage reference. The 14-bit DAC provides two complementary current outputs whose full-scale current is determined by an external resistor. Input data that is latched into the edge-triggered input latches is first interpolated by a *factor of four* by the interpolation filters before updating the 14-bit DAC. A PLL clock multiplier produces the necessary internally synchronized 1×, 2× and 4× clocks from an external reference. The AD9774 can support input data rates as high as 32 MSPS, corresponding to a DAC update rate of 128 MSPS.

The analog and digital sections of the AD9774 have separate power supply inputs (i.e., AVDD and DVDD) that can operate over a 2.7 V to 5.5 V range. A separate supply input (i.e., PLLVDD) having a similar operating range is also provided for the PLL clock multiplier. To maintain optimum noise and distortion performance, PLLVDD should be maintained at the same voltage level as DVDD.

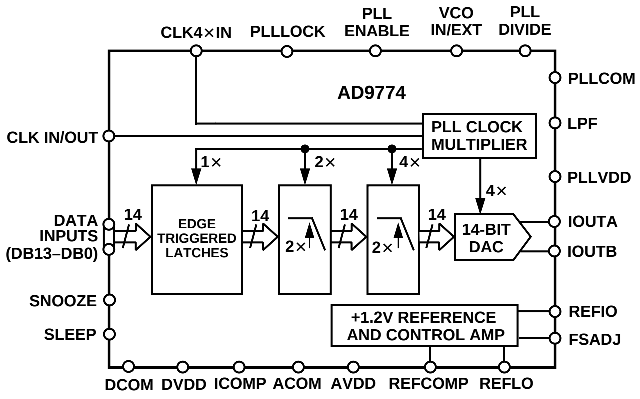

CLK4×IN
PLLLOCK
PLL ENABLE
VCO IN/EXT
PLL DIVIDE
PLLCOM
AD9774
PLL CLOCK MULTIPLIER
LPF
CLK IN/OUT
1×
2×
4×
PLLVDD
4×
DATA INPUTS (DB13–DB0)
14
EDGE TRIGGERED LATCHES
14
2×
14
2×
14
14-BIT DAC
IOUTA
IOUTB
SNOOZE
SLEEP
+1.2V REFERENCE AND CONTROL AMP
REFIO
FSADJ
DCOM
DVDD
ICOMP
ACOM
AVDD
REFCOMP
REFLO

Figure 22. Functional Block Diagram

Preceding the 14-bit DAC are two cascaded 2× digital interpolation filter stages based on a 55- and 23-tap halfband symmetric FIR topology. Edge triggered latches are used to latch the input data on the rising edge of CLK IN/OUT. The composite frequency and impulse response of both filters are shown in Figures 2a and 2b. Table I and Table II list the idealized filter coefficients for each of the filter stages. The interpolation filters essentially multiply the input data rate to the DAC by a factor of four relative to its original input data rate while simultaneously reducing the magnitude of the images associated with the original input data rate.

The benefits of an interpolation filter are clearly seen in Figure 23, which shows an example of the frequency and time domain representation of a discrete time sine wave signal before and after it is applied to a digital interpolation filter. Images of the sine wave signal appear around multiples of the DAC's input data rate as predicted by sampling theory. These undesirable images will also appear at the output of a reconstruction DAC, although modified by the DAC's sin(x)/(x) roll-off response.

In many bandlimited applications, these images must be suppressed by an analog filter following the DAC. The complexity of this analog filter is typically determined by the proximity of the desired fundamental to the first image and the required amount of image suppression. Adding to the complexity of this analog filter may be the requirement of compensating for the DAC's sin(x)/x response.

Referring to Figure 23, the "new" first image associated with the DAC's higher data rate after interpolation is "pushed" out further relative to the input signal. The "old" first image associated with the lower DAC data rate before interpolation is suppressed by the digital filter. As a result, the transition band for the analog reconstruction filter is increased, thus reducing the complexity of the analog filter. Furthermore, the sin(x)/x roll-off over the effective passband (i.e., dc to $f_{CLOCK}/2$) is significantly reduced.

The AD9774 includes a PLL clock multiplier that produces the necessary internally synchronized 1×, 2× and 4× clocks for the edge triggered latches, interpolation filters and DACs. The PLL clock multiplier typically accepts an input data clock, CLK IN/OUT, as its reference source. Alternatively, it can also be configured using an external 4× clock via CLK4×IN. The PLLDIVIDE, VCO IN/EXT, PLLENABLE, and PLLLOCK are control inputs/outputs used in the PLL clock generator. Refer to the PLL CLOCK MULTIPLIER OPERATION section for a detailed discussion on its operation.

The digital section of the AD9774 also includes several other control inputs and outputs. The SLEEP and SNOOZE inputs provide different power-saving modes as discussed in the SLEEP and SNOOZE section.

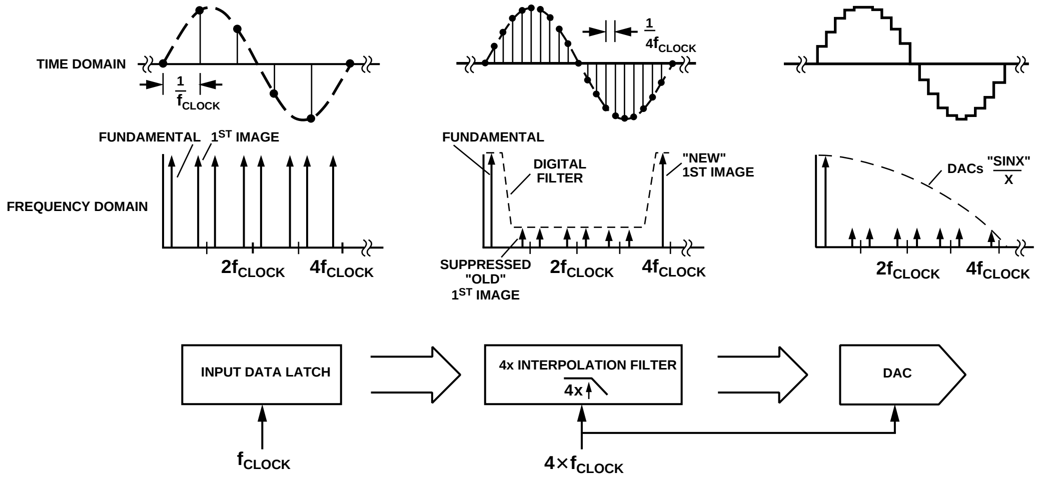

TIME DOMAIN
1/f_CLOCK
1/4f_CLOCK
FUNDAMENTAL
1ST IMAGE
FREQUENCY DOMAIN
2fCLOCK
4fCLOCK
FUNDAMENTAL
DIGITAL FILTER
"NEW" 1ST IMAGE
SUPPRESSED "OLD" 1ST IMAGE
2fCLOCK
4fCLOCK
DACs "SINX/X"
2fCLOCK
4fCLOCK
INPUT DATA LATCH
4x INTERPOLATION FILTER
4x
DAC
fCLOCK
4×fCLOCK

Figure 23. Time and Frequency Domain Example of Digital Interpolation Filter

PLL CLOCK MULTIPLIER OPERATION

The Phase Lock Loop (PLL) Clock Multiplier is intrinsic to the operation of the AD9774 in that it produces the necessary internally synchronized 1×, 2× and 4× clocks for the edge triggered latches, interpolation filters and DACs. Figure 24 shows a functional block diagram of the PLL Clock Multiplier, which consists of a phase detector, a charge pump, a voltage controlled oscillator (VCO), a divide-by-N circuit and some control inputs/outputs. It produces the required internal clocks for the AD9774 by using one of two possible externally applied reference clock sources applied to either CLKIN or CLK4×IN. PLLENABLE and VCO IN/EXT are active HIGH control inputs used to enable the charge pump and VCO respectively.

To maintain optimum noise and distortion performance, PLLVDD and DVDD should be set to similar voltage levels. If a separate supply cannot be provided for PLLVDD, PLLVDD can be tied to DVDD using an LC filter network similar to that shown in Figure 41.

Many applications will select a reference clock operating at the data input rate as shown in Figure 24. In this case, the external clock source is applied to CLKIN and the PLL Clock Multiplier is fully enabled by tying PLLENABLE and VCO IN/EXT to PLLVDD. Note, CLKIN must adhere to the timing requirements shown in Figure 1. A 1.5 kΩ resistor and 0.01 μF ceramic capacitor connected in series from LPF to PLLVDD are required to optimize the phase noise vs. settling/acquisition time characteristics of the PLL. PLLLOCK is a control output, active HIGH, which may be monitored upon system power-up to indicate that the PLL is successfully "locked" to CLKIN. Note, applications employing multiple AD9774 devices will benefit from the PLL Clock Multiplier's ability to ensure precise simultaneous updating/phase synchronization of these devices when driven by the same input clock source.

PLLDIVIDE is used to preset the "lock-in" range of the PLL. It should be tied to PLLCOM if CLKIN is greater than 10 MHz and to PLLVDD if CLKIN is between 5.5 MHz and 10 MHz. For operation below 5.5 MHz (i.e., input data rates less than 5.5 MSPS), the internal charge pump and VCO should be disabled by tying PLLENABLE and VCO IN/EXT LOW. In this case, the user MUST supply a system clock operating at 4× the input data rate as discussed below.

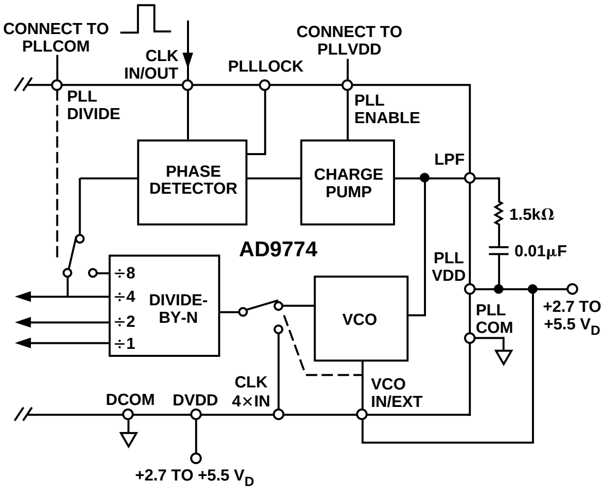


Figure 24. Clock Multiplier with PLL Enabled

There are two cases in which a user may consider or be required to disable the internal PLL Clock Multiplier and supply the AD9774 with an external 4× system clock. Applications already containing a system clock operating at four (i.e., 4×) the input data rate may consider using it as the master clock source. Applications with input data rates less than 5.5 MSPS ***must*** use a master 4× clock.

In any of these cases, the clock source is applied to CLK4×IN and the PLL is partially disabled by typing PLLENABLE and VCO IN/EXT to PLLCOM as shown in Figure 25. LPF may remain open since this portion of the PLL circuitry is disabled. The divide-by-N circuit still remains enabled providing a 1× or 2× internal clock at CLOCK IN/OUT depending on the state of PLLDIVIDE. Since the digital input data is latched into the AD9774 on the rising edge of the 1× clock, PLLDIVIDE should be tied to PLLCOM such that the 1× clock appears as an output at CLOCK IN/OUT. The input data should be stable 5 ns (i.e., data set-up) before the rising edge of the 1× clock appearing at CLOCK IN/OUT and remain stable for 1 ns after the rising edge (i.e., data hold) to ensure proper latching. Note, the rising edge of the 1× clock occurs approximately 9 ns to 15 ns relative to the falling edge of the CLK4× input. If a data timing issue exists between the AD9774 and its external driver device, the CLK4× input can be inverted via an external gate to ensure proper set-up and hold time.

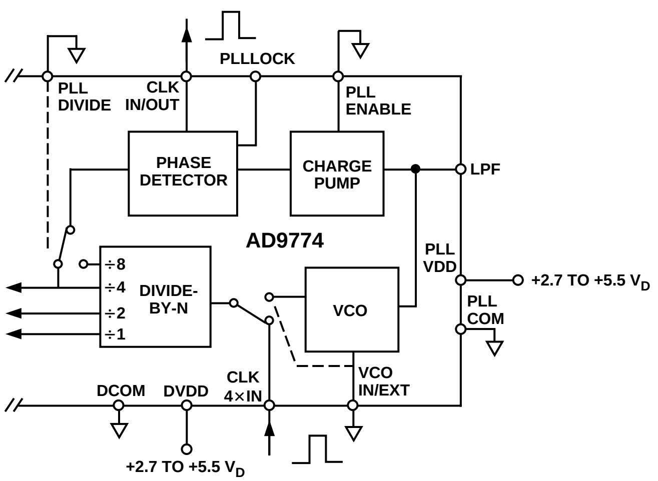


Figure 25. Clock Divider with PLL Disabled

DAC OPERATION

The 14-bit DAC along with the 1.2 V reference and reference control amplifier is shown in Figure 26. The DAC consists of a large PMOS current source array capable of providing up to 20 mA of full-scale current, I_{OUTFS}. The array is divided into 31 equal currents which make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose values are 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle-bits current sources. All of these current sources are switched to one or the other of two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., > 100 kΩ).

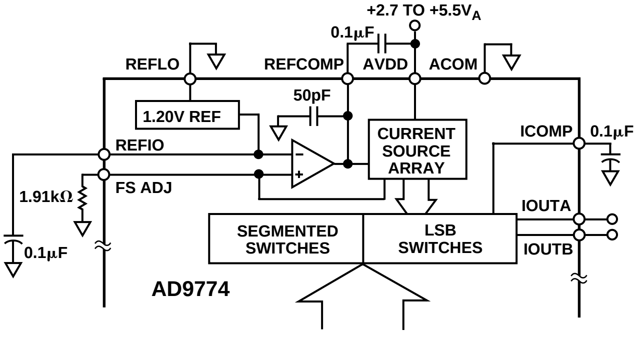


Figure 26. Block Diagram of Internal DAC, 1.2 V Reference, and Reference Control Circuits

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference, REFIO, sets the reference current, I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is exactly thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9774 provides complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383) while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as:

$$IOUTA = (DAC\ CODE/16384) \times I_{OUTFS} \tag{1}$$

$$IOUTB = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \tag{2}$$

where $DAC\ CODE = 0$ to 16383 (i.e., Decimal Representation).

As previously mentioned, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \tag{3}$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note that R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply:

$$V_{OUTA} = IOUTA \times R_{LOAD} \tag{5}$$

$$V_{OUTB} = IOUTB \times R_{LOAD} \tag{6}$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across IOUTA and IOUTB is:

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \tag{7}$$

Substituting the values of IOUTA, IOUTB and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 16383)/16384\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \tag{8}$$

These last two equations highlight some of the advantages of operating the AD9774 differentially. First, the differential operation will help cancel common-mode error sources associated with IOUTA and IOUTB such as noise, distortion and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (VOUTA and VOUTB) or differential output (V_{DIFF}) of the AD9774 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

REFERENCE OPERATION

The AD9774 contains an internal 1.20 V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output,* depending on whether the internal or external reference is selected. If REFLO is tied to ACOM, as shown in Figure 27, the internal reference is activated, and REFIO provides a 1.20 V output. In this case, the internal reference *must* be compensated externally with a ceramic chip capacitor of 0.1 μF or greater from REFIO to REFLO. If any additional loading is required, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA.

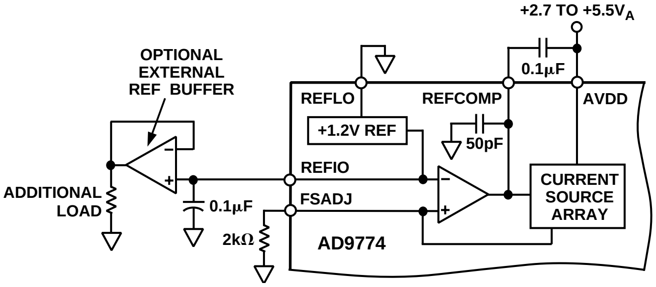


Figure 27. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 28. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 μF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

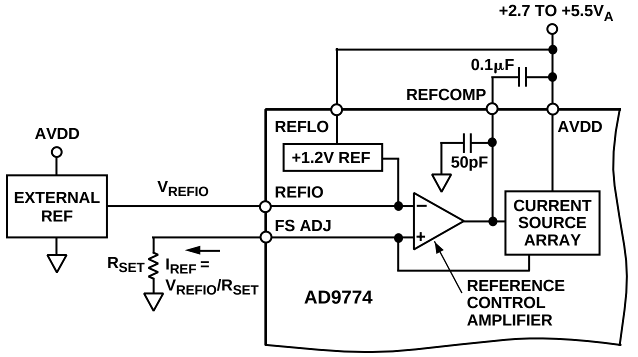

+2.7 TO +5.5V$_A$
0.1μF
REFCOMP
REFLO
AVDD
AVDD
+1.2V REF
50pF
EXTERNAL REF
V_{REFIO}
REFIO
FS ADJ
CURRENT SOURCE ARRAY
R_{SET}
I_{REF} = V_{REFIO}/R_{SET}
AD9774
REFERENCE CONTROL AMPLIFIER

Figure 28. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9774 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 28, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 μA and 625 μA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9774, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

There are two methods by which I_{REF} can be varied for a fixed R_{SET}. The first method is suitable for a single-supply system in which the internal reference is disabled, and the common-mode voltage of REFIO is varied over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1 MΩ, a simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 30 using the AD7524 and an external 1.2 V reference, the AD1580.

The second method may be used in a dual-supply system in which the common-mode voltage of REFIO is fixed, and I_{REF} is varied by an external voltage, V_{GC}, applied to R_{SET} via an amplifier. An example of this method is shown in Figure 29 in which the internal reference is used to set the common-mode voltage of the control amplifier to 1.20 V. The external voltage, V_{GC}, is referenced to ACOM and should not exceed 1.2 V. The value of R_{SET} is such that I_{REFMAX} and I_{REFMIN} do not exceed 62.5 μA and 625 μA, respectively. The associated equations in Figure 29 can be used to determine the value of R_{SET}.

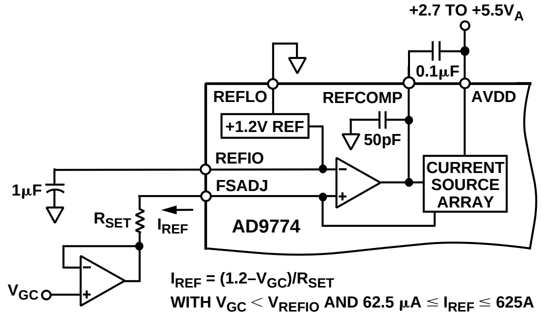

+2.7 TO +5.5V$_A$
0.1μF
REFLO
REFCOMP
AVDD
+1.2V REF
50pF
REFIO
FSADJ
1μF
CURRENT SOURCE ARRAY
R_{SET}
I_{REF}
AD9774
V_{GC}
$I_{REF} = (1.2–V_{GC})/R_{SET}$
WITH $V_{GC} < V_{REFIO}$ AND 62.5 μA ≤ I_{REF} ≤ 625A

Figure 29. Dual Supply Gain Control Circuit

ANALOG OUTPUTS

The AD9774 produces two complementary current outputs, IOUTA and IOUTB, which may be configured for single-end or differential operation. IOUTA and IOUTB can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 31 shows the equivalent analog output circuit of the AD9774 consisting of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches and is typically 100 kΩ in parallel with 5 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, AVDD, and full-scale current, I_{OUTFS}. Although the output impedance's signal dependency can be a source of dc nonlinearity and ac linearity (i.e., distortion), its effects can be limited if certain precautions are noted.

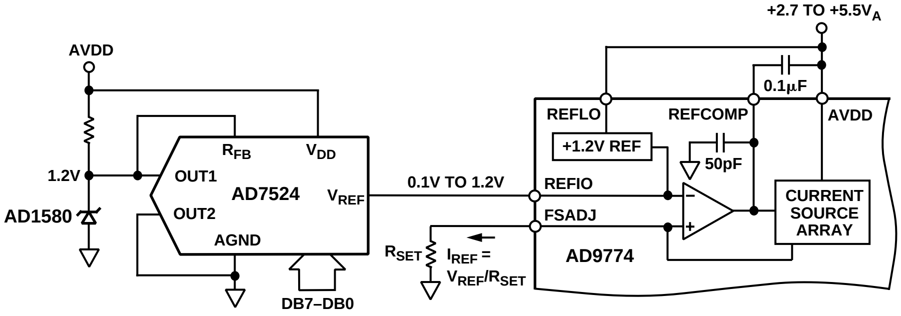

+2.7 TO +5.5V$_A$
AVDD
0.1μF
REFLO
REFCOMP
AVDD
+1.2V REF
50pF
R_{FB}
V_{DD}
1.2V
OUT1
AD7524
V_{REF}
0.1V TO 1.2V
REFIO
AD1580
OUT2
FSADJ
CURRENT SOURCE ARRAY
AGND
R_{SET}
I_{REF} = V_{REF}/R_{SET}
AD9774
DB7–DB0

Figure 30. Single Supply Gain Control Circuit

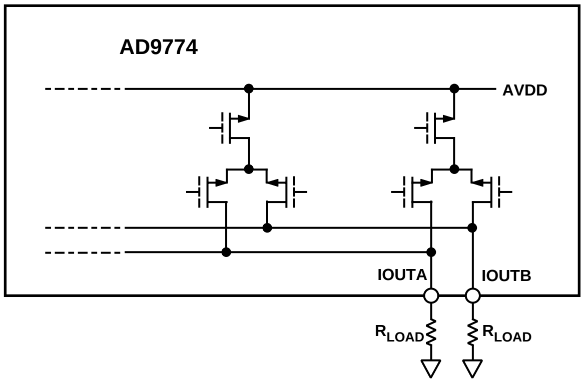


Figure 31. Equivalent Analog Output Circuit

IOUTA and IOUTB also have a negative and positive voltage compliance range. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9774. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. Operation beyond the positive compliance range will induce clipping of the output signal, which severely degrades the AD9774's linearity and distortion performance.

For applications requiring the optimum dc linearity, IOUTA and/or IOUTB should be maintained at a virtual ground via an I-V op amp configuration. Maintaining IOUTA and/or IOUTB at a virtual ground keeps the output impedance of the AD9774 fixed, significantly reducing its effect on linearity. However, it does not necessarily lead to the optimum distortion performance due to limitations of the I-V op amp. Note that the INL/DNL specifications for the AD9774 are measured in this manner using IOUTA. In addition, these dc linearity specifications remain virtually unaffected over the specified power supply range of 2.7 V to 5.5 V.

Operating the AD9774 with reduced voltage output swings at IOUTA and IOUTB in a differential or single-ended output configuration reduces the signal dependency of its output impedance thus enhancing distortion performance. Although the voltage compliance range of IOUTA and IOUTB extends from –1.0 V to +1.25 V, optimum distortion performance is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed approximately 0.5 V. A properly selected transformer with a grounded center-tap will allow the AD9774 to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at IOUTA and IOUTB. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to Applying the AD9774 section for examples of various output configurations.

The most significant improvement in the AD9774's distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both IOUTA and IOUTB can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed waveform's frequency content increases and/or its amplitude decreases.

The distortion and noise performance of the AD9774 is also slightly dependent on the analog and digital supply as well as the full-scale current setting, I_{OUTFS}. Operating the analog supply at 5.0 V ensures maximum headroom for its internal PMOS current sources and differential switches leading to improved distortion performance. Although I_{OUTFS} can be set between 2 mA and 20 mA, selecting an I_{OUTFS} of 20 mA will provide the best distortion and noise performance. The noise performance of the AD9774 is affected by the digital supply (DVDD), output frequency, and increases with increasing clock rate. Operating the AD9774 with low voltage logic levels between 3 V and 3.3 V will slightly reduce the amount of on-chip digital noise.

In summary, the AD9774 achieves the optimum distortion and noise performance under the following conditions:

(1) Differential Operation.
(2) Positive voltage swing at IOUTA and IOUTB limited to +0.5 V.
(3) IOUTFS set to 20 mA.
(4) Analog Supply (AVDD) set at 5.0 V.
(5) Digital Supply (DVDD) and Phase Lock Loop Supply (PLLVDD) set at 3.0 V to 3.3 V with appropriate logic levels.

Note that the ac performance of the AD9774 is characterized under the above-mentioned operating conditions.

DIGITAL INPUTS/OUTPUTS

The digital input of the AD9774 consists of 14 data input pins and a clock input pin, and several control input pins. Since some of the internal logic is operated from DVDD and PLLVDD, they must be set to the same or similar levels to ensure proper compatibility with any external logic/drivers. The two digital outputs of the AD9774, PLL LOCK and CLK OUT originate from the internal PLL circuitry and thus its output logic levels will be set by PLLVDD.

The 14-bit parallel data inputs follow standard positive binary coding where DB13 is the most significant bit (MSB), and DB0 is the least significant bit (LSB). IOUTA produces a full-scale output current when all data bits are at Logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch and is designed to support a clock and input data rate as high as 32 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth as shown in Figure 1. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met. The digital inputs are CMOS-compatible with logic thresholds, $V_{THRESHOLD,}$ set to approximately half the digital positive supply (i.e., DVDD or PLLVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9774 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers $V_{OH(MAX)}$. A DVDD of 3 V to 3.3 V will typically ensure proper compatibility with most TTL logic families. Figure 32 shows the equivalent digital input circuit for the data and clock inputs.

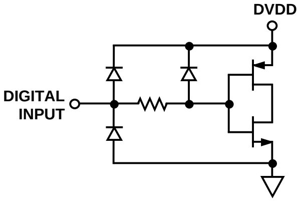


Figure 32. Equivalent Digital Input

Since the AD9774 is capable of being updated up to 32 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9774 with reduced logic swings and a corresponding digital supply (DVDD) will result in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9774 as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9774 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough.

The external clock driver circuitry should provide the AD9774 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

SLEEP AND SNOOZE MODE OPERATION

The AD9774 has a SLEEP function that turns off the output current and reduces the supply current to less than 5 mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. The AD9774 takes less than 0.1 µs to power down and approximately 6.4 µs to power back up.

The SNOOZE mode should be considered as an alternative power-savings option if the power-up characteristics of the SLEEP mode are unsuitable. This mode, which is also activated by applying a logic level "1" to the SNOOZE pin, disables the AD9774's digital filters only, resulting in significant power savings. Both the SLEEP and SNOOZE pins should be tied to DCOM if power savings is not required.

POWER DISSIPATION

The power dissipation, P_D, of the AD9774 is dependent on several factors, including: (1) AVDD, PLLVDD, and DVDD, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; and (4) the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 33, and is insensitive to f_{CLOCK}.

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 34 and 35 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note, how I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

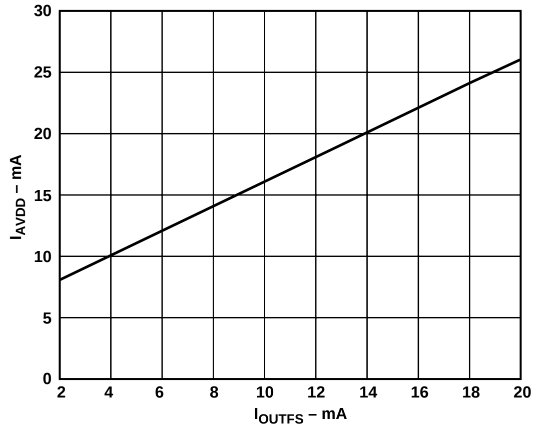


Figure 33. I_{AVDD} vs. I_{OUTFS}

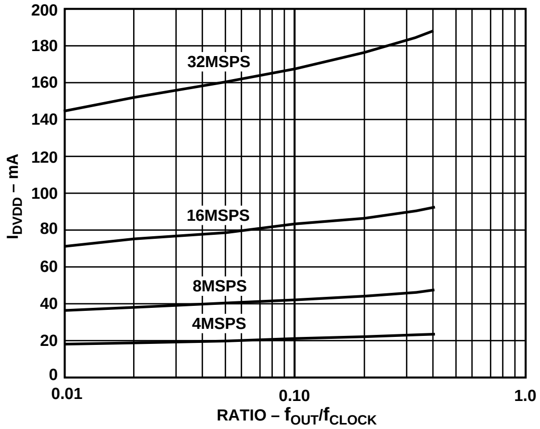


Figure 34. I_{DVDD} vs. Ratio @ DVDD = 5 V

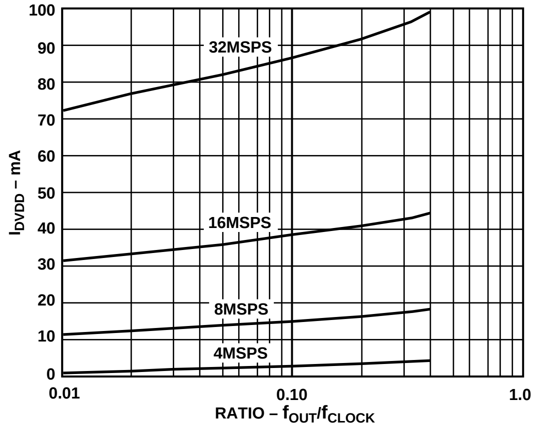


Figure 35. I_{DVDD} vs. Ratio @ DVDD = 3 V

For those applications requiring the AD9774 to operate under the following conditions: (1) AVDD, PLLVDD and DVDD = +5 V; (2) f_{CLOCK} > 25 MSPS; and (3) ambient temperatures > 70°C; proper thermal management via a heatsink or thermal epoxy is recommended.

APPLYING THE AD9774

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9774. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an approximately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting IOUTA or IOUTB into a negative unipolar voltage. This configuration provides the best dc linearity since IOUTA or IOUTB is maintained at a virtual ground.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 36. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

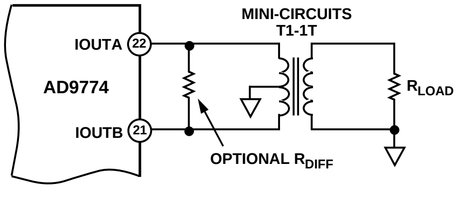


Figure 36. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9774. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 37. The AD9774 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's high slewing output from overloading the op amp's input.

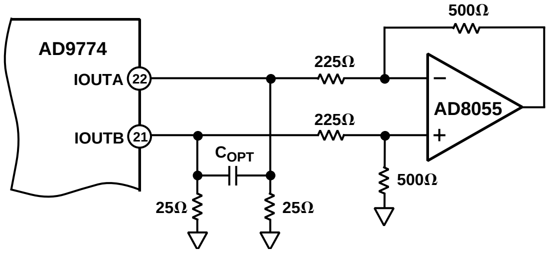


Figure 37. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8055 is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9774 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 38 provides the necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the AD9774 and the op amp, is also used to level-shift the differential output of the AD9774 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

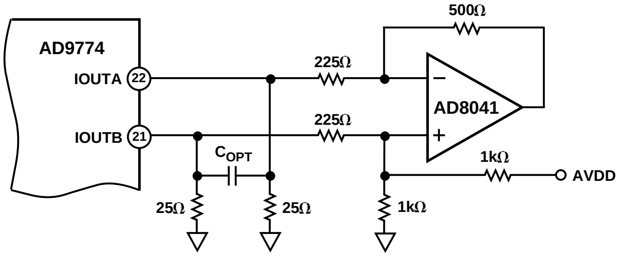


Figure 38. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 39 shows the AD9774 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by IOUTA. The unused output (IOUTB) can be connected to ACOM directly. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

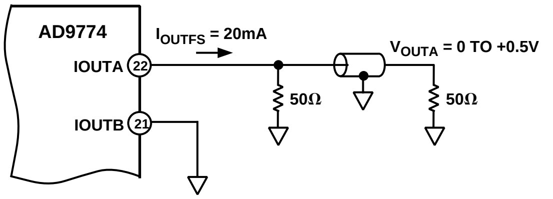


Figure 39. 0 V to +0.5 V Unbuffered Voltage Output

SINGLE-ENDED BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 40 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9774 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

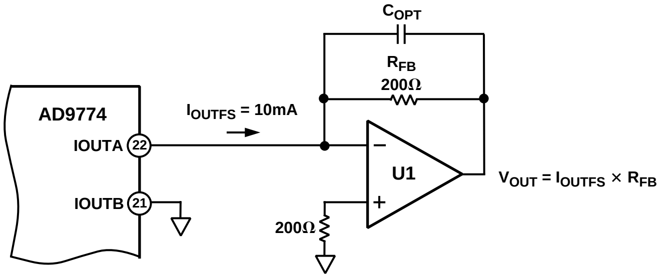


Figure 40. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing and supply bypassing and grounding. Figures 44–49 illustrate the recommended printed circuit board ground, power and signal plane layouts that are implemented on the AD9774 evaluation board.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9774 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM and PLLVDD, the Phase Lock Loop Supply, should be decoupled to PLLCOM.

For those applications requiring a single +5 V or +3 V supply for both the analog, digital supply and Phase Lock Loop supply, a clean AVDD and/or PLLVDD may be generated using the circuit shown in Figure 41. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

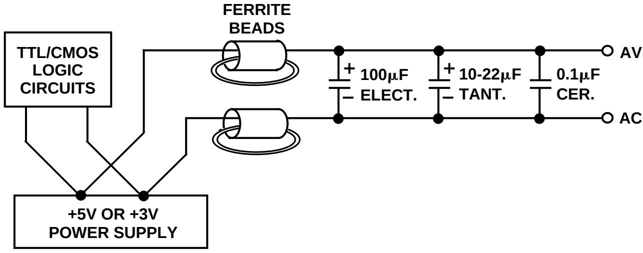


Figure 41. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtain optimum results from the AD9774. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistors should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

MULTITONE PERFORMANCE CONSIDERATIONS AND CHARACTERIZATION

The frequency domain performance of high speed DACs has traditionally been characterized by analyzing the spectral output of a reconstructed full-scale (i.e., 0 dBFS), single-tone sine wave at a particular output frequency and update rate. Although this characterization data is useful, it is often insufficient to reflect a DAC's performance for a reconstructed multitone or spread-spectrum waveform. In fact, evaluating a DAC's spectral performance using a full-scale, single tone at the highest specified frequency (i.e., f_H) of a bandlimited waveform is typically indicative of a DAC's "worst-case" performance for that given waveform. In the time domain, this full-scale sine wave represents the lowest peak-to-rms ratio or crest factor (i.e., V_{PEAK}/V rms) that this bandlimited signal will encounter.

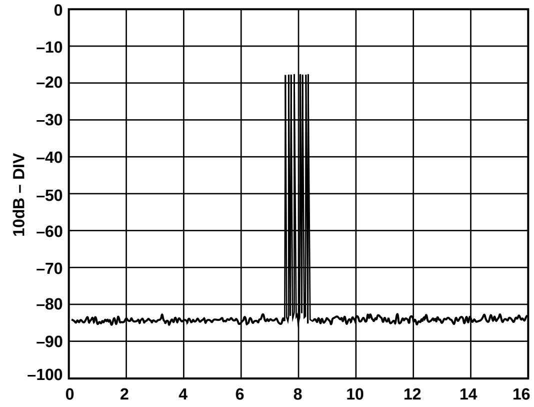


Figure 42a. Multitone Spectral Plot

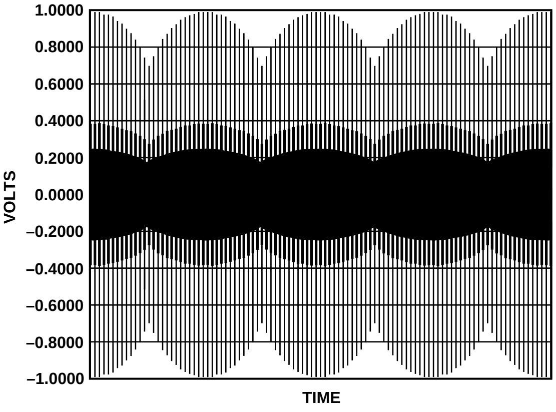


Figure 42b. Time Domain "Snapshot" of the Multitone Waveform

However, the inherent nature of a multitone, spread spectrum, or QAM waveform, in which the spectral energy of the waveform is spread over a designated bandwidth, will result in a higher peak-to-rms ratio when compared to the case of a simple sine wave. As the reconstructed waveform's peak-to-average ratio increases, an increasing amount of the signal energy is concentrated around the DAC's midscale value. Figure 42a is just one example of a bandlimited multitone vector (i.e., eight tones) centered around one-half the Nyquist bandwidth (i.e., $f_{CLOCK}/4$). This particular multitone vector, has a peak-to-rms ratio of 13.5 dB compared to a sine waves peak-to-rms ratio of 3 dB. A "snapshot" of this reconstructed multitone vector in the time domain as shown in Figure 43b reveals the higher signal content around the midscale value. As a result, a DAC's "small-scale" dynamic and static linearity becomes increasingly critical in obtaining low intermodulation distortion and maintaining sufficient carrier-to-noise ratios for a given modulation scheme.

A DAC's small-scale linearity performance is also an important consideration in applications where additive dynamic range is required for gain control purposes or "predistortion" signal conditioning. For instance, a DAC with sufficient dynamic range can be used to provide additional gain control of its reconstructed signal. In fact, the gain can be controlled in 6 dB increments by simply performing a shift left or right on the DAC's digital input word. Other applications may intentionally predistort a DAC's digital input signal to compensate for nonlinearities associated with the subsequent analog components in the signal chain. For example, the signal compression associated with a power amplifier can be compensated for by predistorting the DAC's digital input with the inverse nonlinear transfer function of the power amplifier. In either case, the DAC's performance at reduced signal levels should be carefully evaluated.

A full-scale single tone will induce all of the dynamic and static nonlinearities present in a DAC that contribute to its distortion and hence SFDR performance. As the frequency of this reconstructed full-scale, single-tone waveform increases, the dynamic nonlinearities of any DAC (i.e., AD9774) tend to dominate thus contributing to the roll-off in its SFDR performance. However, unlike most DACs, which employ an R-2R ladder for the lower bit current segmentation, the AD9774 (as well as other TxDAC members) exhibits an improvement in distortion performance as the amplitude of a single tone is reduced from its full-scale level. This improvement in distortion performance at reduced signal levels is evident if one compares the SFDR performance vs. frequency at different amplitudes (i.e., 0 dBFS, –6 dBFS and –12 dBFS) and sample rates as shown in Figures 4 through 15. Maintaining decent "small-scale" linearity across the full span of a DAC transfer function is also critical in maintaining excellent multitone performance.

Although characterizing a DAC's multitone performance tends to be application-specific, much insight into the potential performance of a DAC can also be gained by evaluating the DAC's swept power (i.e., amplitude) performance for single, dual and multitone test vectors at different clock rates and carrier frequencies. The DAC is evaluated at different clock rates when reconstructing a specific waveform whose amplitude is decreased in 3 dB increments from full-scale (i.e., 0 dBFS). For each specific waveform, a graph showing the SFDR (over Nyquist) performance vs. amplitude can be generated at the different tested clock rates as shown in Figures 19 and 20. Note that the carrier(s)-to-clock ratio remains constant in each figure.

A multitone test vector may consist of several equal amplitude, spaced carriers each representative of a channel within a defined bandwidth as shown in Figure 42a. In many cases, one or more tones are removed so the intermodulation distortion performance of the DAC can be evaluated. Nonlinearities associated with the DAC will create spurious tones of which some may fall back into the "empty" channel thus limiting a channel's carrier-to-noise ratio. Other spurious components falling outside the band of interest may also be important, depending on the system's spectral mask and filtering requirements.

This particular test vector was centered around one-half the Nyquist bandwidth (i.e., $f_{CLOCK}/4$) with a passband of $f_{CLOCK}/16$. Centering the tones at a much lower region (i.e., $f_{CLOCK}/10$) would lead to an improvement in performance while centering the tones at a higher region (i.e., $f_{CLOCK}/2.5$) would result in a degradation in performance. Figure 43a shows the SFDR vs. amplitude at 32 MSPS up to the Nyquist frequency while Figure 43b shows the SFDR vs. amplitude within the passband of the test vector. In assessing a DAC's multitone performance, it is also recommended that several units be tested under exactly the same conditions to determine any performance variability.

AD9774 EVALUATION BOARD

General Description

The AD9774-EB is an evaluation board for the AD9774 14-bit DAC converter. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to easily and effectively evaluate the AD9774 in signal reconstruction applications, where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9774 in various configurations. The digital inputs are designed to be driven directly from various word generators with the onboard option to add a resistor network for proper load termination. Provisions are also made to operate the AD9774 with either the internal or external reference or to exercise the SLEEP or SNOOZE power-savings feature.

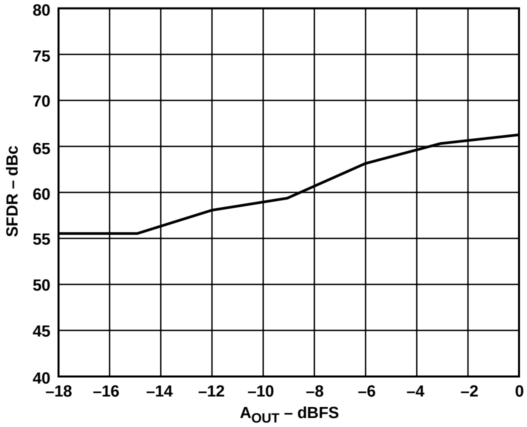


Figure 43a. Multitone SFDR vs. A_{OUT} @ 32 MSPS (Up to Nyquist)

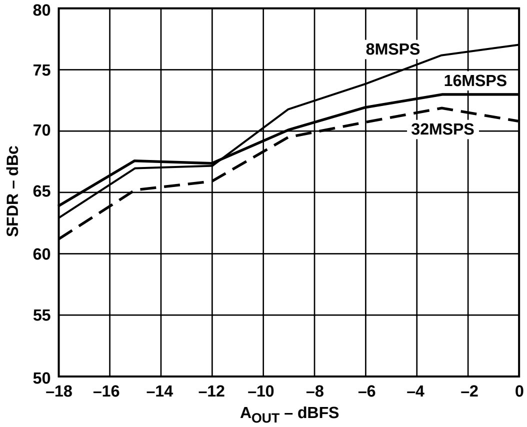


Figure 43b. Multitone SFDR vs. A_{OUT} @ 32 MSPS (Within Multitone Passband)

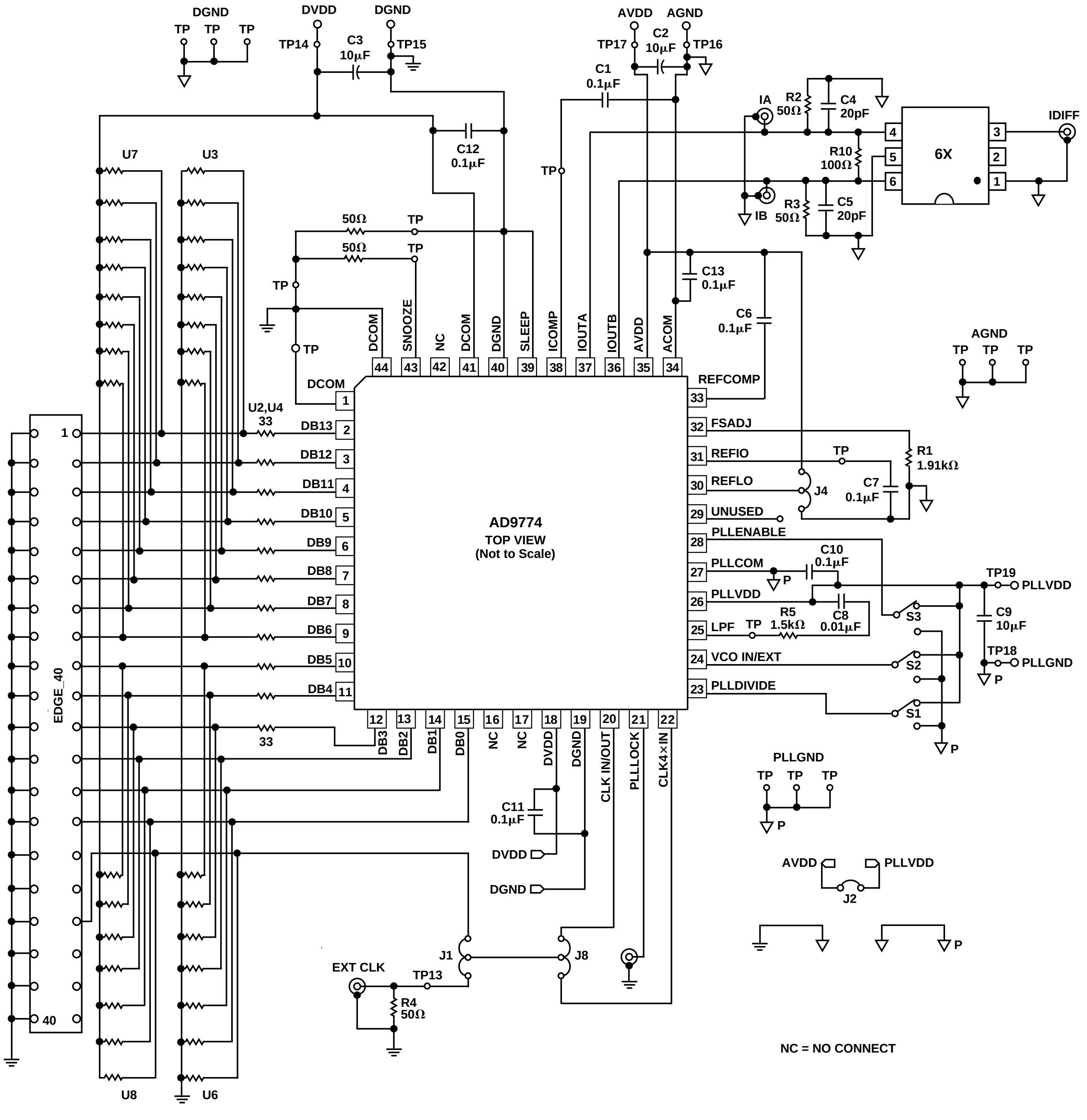

DGND
TP
TP
TP
DVDD
DGND
TP14
C3
10μF
TP15
AVDD
AGND
C2
10μF
TP17
TP16
C1
0.1μF
C12
0.1μF
IA
R2
50Ω
C4
20pF
IDIFF
R10
100Ω
6X
IB
R3
50Ω
C5
20pF
U7
U3
50Ω
50Ω
TP
TP
TP
TP
TP
C13
0.1μF
C6
0.1μF
DCOM
SNOOZE
NC
DCOM
DGND
SLEEP
ICOMP
IOUTA
IOUTB
AVDD
ACOM
44
43
42
41
40
39
38
37
36
35
34
AGND
TP
TP
TP
DCOM
1
REFCOMP
33
U2,U4
33
DB13
2
DB12
3
DB11
4
DB10
5
DB9
6
DB8
7
DB7
8
DB6
9
DB5
10
DB4
11
32
FSADJ
31
REFIO
30
REFLO
29
UNUSED
28
PLLENABLE
27
PLLCOM
26
PLLVDD
25
LPF
24
VCO IN/EXT
23
PLLDIVIDE
R1
1.91kΩ
J4
C7
0.1μF
AD9774
TOP VIEW
(Not to Scale)
C10
0.1μF
P
C8
0.01μF
R5
1.5kΩ
S3
S2
S1
TP19
PLLVDD
C9
10μF
TP18
PLLGND
P
P
EDGE_40
1
40
33
12
13
14
15
16
17
18
19
20
21
22
DB3
DB2
DB1
DB0
NC
NC
DVDD
DGND
CLK IN/OUT
PLLLOCK
CLK4×IN
C11
0.1μF
DVDD
DGND
PLLGND
TP
TP
TP
P
AVDD
PLLVDD
J2
P
J1
J8
EXT CLK
TP13
R4
50Ω
U8
U6
NC = NO CONNECT

Figure 44. Evaluation Board Schematic

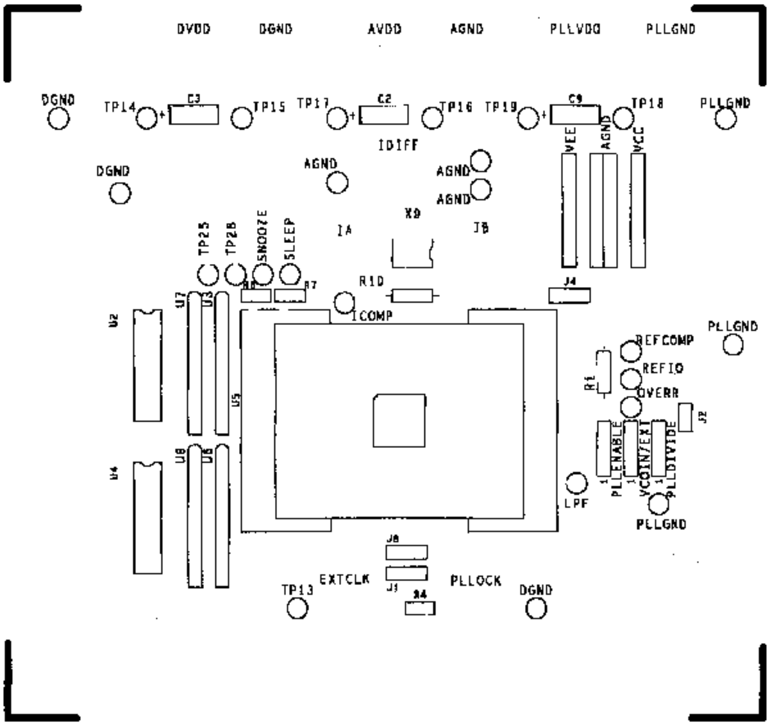

DVDD
DGND
AVDD
AGND
PLLVDD
PLLGND
DGND
TP14
C3
TP15
TP17
C2
TP16
TP19
C9
TP18
PLLGND
IDIFF
VEE
AGND
VCC
DGND
AGND
AGND
AGND
X9
IA
IB
TP25
TP28
SNOOZE
SLEEP
R8
R7
R10
J4
ICOMP
U2
U7
U3
U5
PLLGND
REFCOMP
R1
REFIO
OVERR
J2
PLLENABLE
VCOIN/EXT
PLLDIVIDE
U4
U8
U6
LPF
PLLGND
J8
EXTCLK
J1
PLLOCK
TP13
R4
DGND

Figure 45. Silkscreen Layer—Top

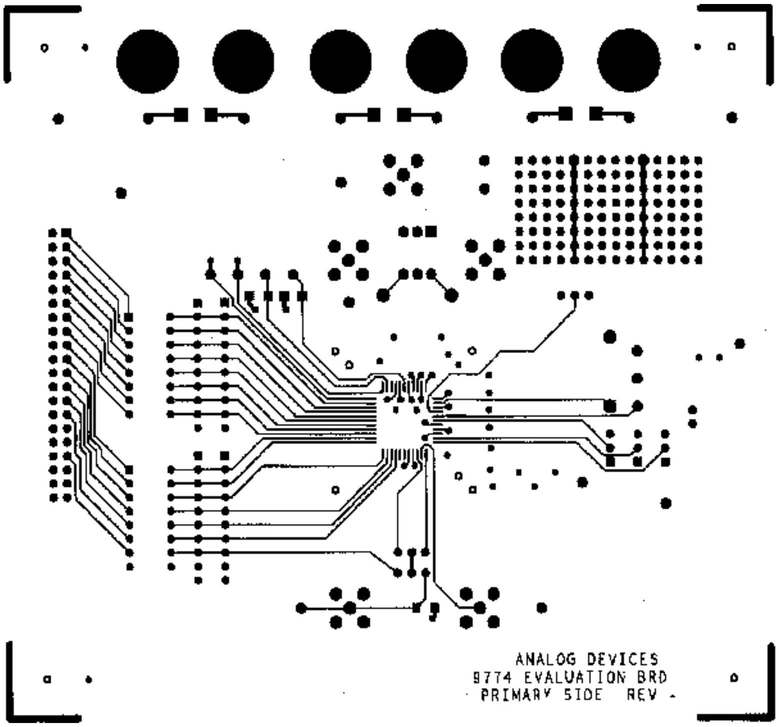

ANALOG DEVICES
9774 EVALUATION BRD
PRIMARY SIDE REV -

Figure 46. Component Side PCB Layout (Layer 1)

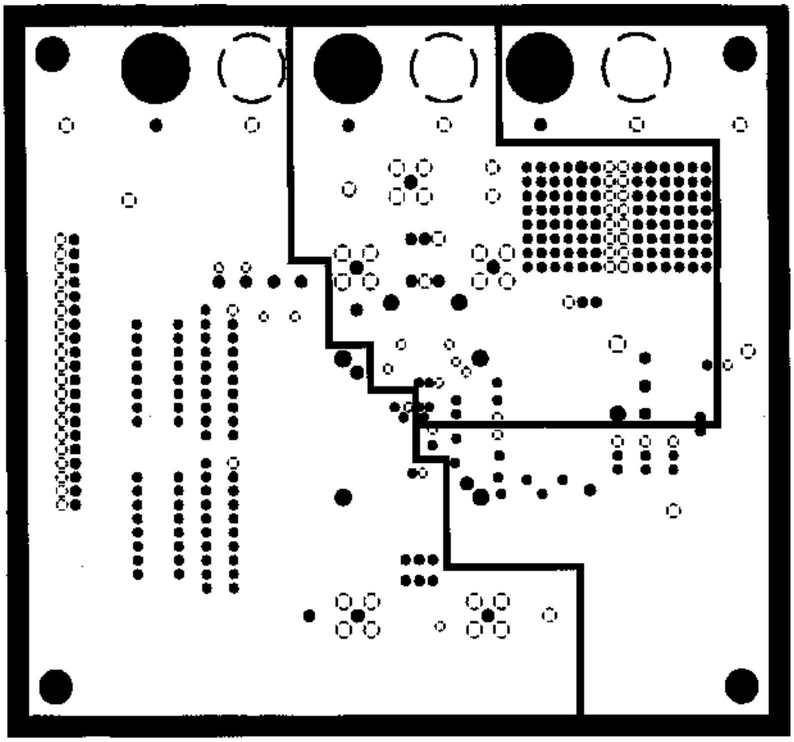


Figure 47. Ground Plane PCB Layout (Layer 2)

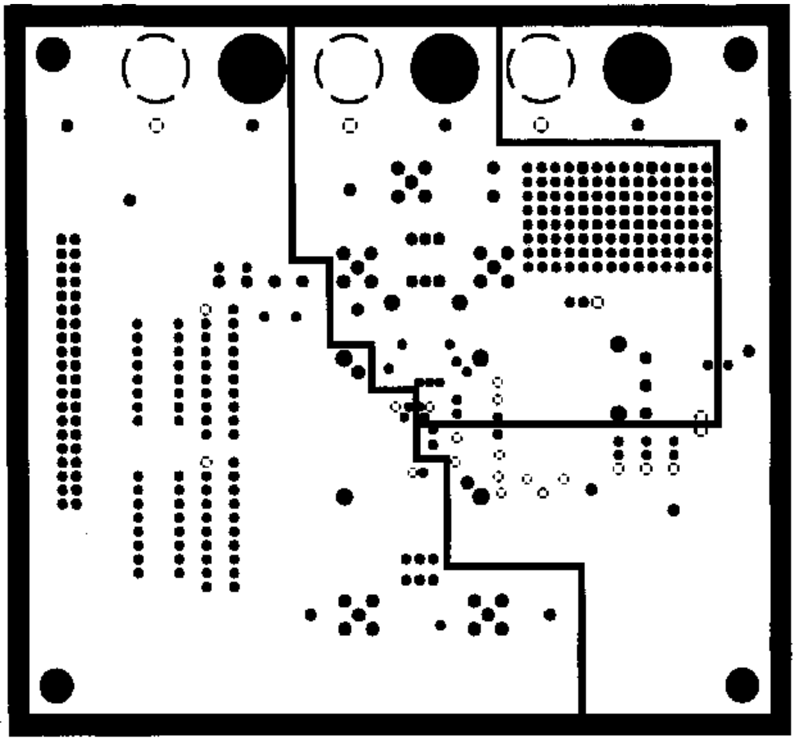


Figure 48. Power Plane PCB Layout (Layer 3)

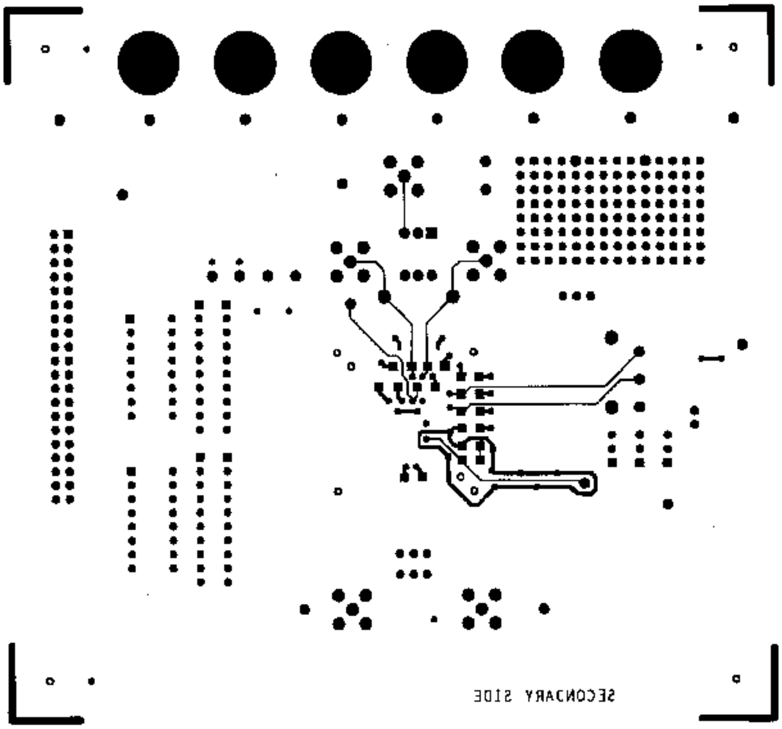

SECONDARY SIDE

Figure 49. Solder Side PCB Layout (Layer 4)

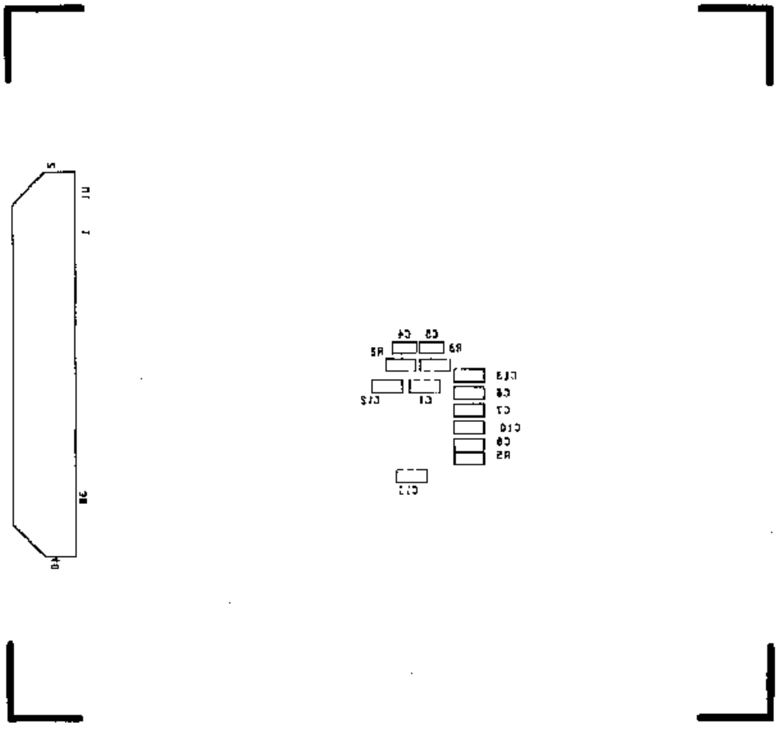
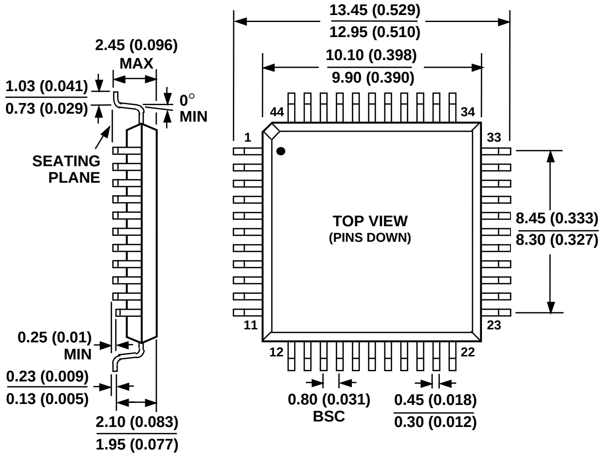


Figure 50. Silkscreen Layer—Bottom

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches).

44-Lead Metric Quad Flatpack
(S-44)


13.45 (0.529)
12.95 (0.510)
10.10 (0.398)
9.90 (0.390)
2.45 (0.096) MAX
1.03 (0.041)
0.73 (0.029)
0° MIN
SEATING PLANE
44
34
1
33
TOP VIEW
(PINS DOWN)
8.45 (0.333)
8.30 (0.327)
11
23
12
22
0.25 (0.01) MIN
0.23 (0.009)
0.13 (0.005)
2.10 (0.083)
1.95 (0.077)
0.80 (0.031) BSC
0.45 (0.018)
0.30 (0.012)

C3198b–0–11/98

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