



Example Configurations

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BOARD REFERENCE:	WM8904-6201-FL32-M-REV1
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8904
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INTRODUCTION

The WM8904-6201-FL32-M-REV1 Customer Mini Board is compatible with the 6201-EV1-REV2 customer evaluation board and together provide a complete hardware platform for evaluation of the WM8904. The WM8904 Customer Mini Board can also be used independently and connected directly to a processor board using flying field wires or appropriate headers. This document will cover both, but performance data will be based on the Wolfson system with 6201-EV1-REV2 mainboard. Configurations covered are listed below:

- DAC to Headphone playback
- IN1L/R to ADC Recording
- IN1L+2L / IN1R+2R to ADC Recording (differential input)
- IN1L/R to LINEOUTL/R (analogue bypass)
- IN1L/R to LINEOUTL/R (digital loopback)

This document should be used as a starting point for evaluation of WM8904 but it will not cover every possible configuration.

Assumptions:

1. The user is familiar with the 6201-EV1-REV2 main board and that the board is correctly configured for the path of interest (see related documents below)
2. The user has control of the WM8904 register settings, for example by installing Wolfson WISCE software.

Related documents:

1. WM8904 datasheet
2. WM8904-6201-FL32-M-REV1 Schematic and Layout.pdf
3. 6201-EV1-REV2 Schematic and Layout.pdf
4. WISCE Quick Start Guide.pdf

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BOARD CONFIGURATION STAND-ALONE

The WM8904 Customer Mini Board can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 1 below shows the connections required to power-up and control the WM8904 Customer Mini Board.

Please refer to the Table 1 for further detail on external I/O connections.

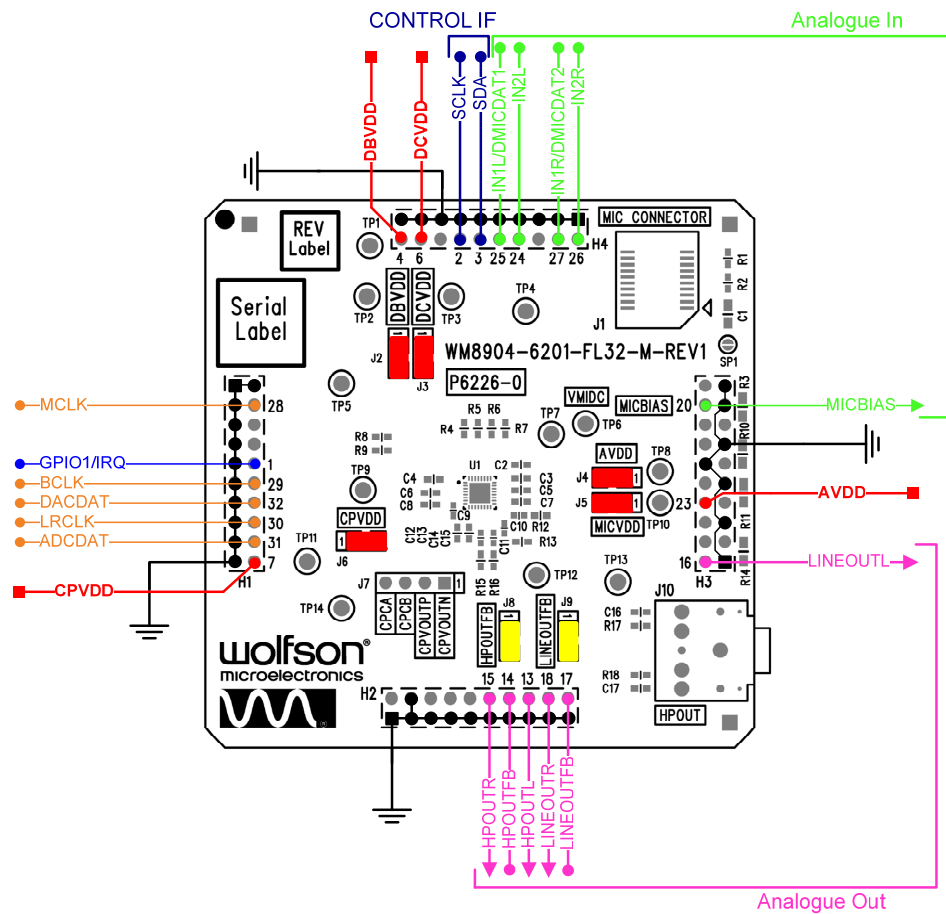


Figure 1 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
Voltage Supplies		
AVDD	H3: pin 8	AVDD = 1.71V to 2.0V
CPVDD	H1: pin 20	CPVDD = 1.71 to 2.0V
DCVDD	H4: pin 18	DCVDD = 0.95V to 1.98V
DBVDD	H4: pin 20	DBVDD = 1.42V to 3.6V
MICVDD	J5, TP10	MICVDD=1.71 to 3.6V , connected by default to AVDD, can also be supplied to pin 2 of J5
Ground		
DGND	Common Ground	Analogue and digital grounds must always be within 0.3V of each other
AGND		
CPGND		
Control Interface		
SDA	H4: pin 12	Both control interface signals should swing between DGND and DBVDD
SCLK	H4: pin 14	
Master Clock		
MCLK	H1: pin 4	Signal should swing between DGND and DBVDD
Digital I/O & Audio Interface		
GPIO1/IRQ	H1: pin 10	Signals should swing between DGND and DBVDD
BCLK/GPIO4	H1: pin 12	
DACDAT	H1: pin 14	
LRCLK	H1: pin 16	
ADCDAT	H1: pin 18	
Digital / Analogue Inputs		
IN2R	H4: pin 2	Observe maximum input levels as per WM8904 datasheet
IN1R/DMICDAT2	H4: pin 4	
IN2L	H4: pin 8	
IN1L/DMICDAT1	H4: pin 10	
MICBIAS	H3: pin 18	Analogue microphone bias voltage output
Analogue Outputs		
HPOUTR	H2: pin 12	Ground referenced headphone output
HPOUTL	H2: pin 16	
HPOUTFB	H2: pin 14	HP reference pin, recommended to be connected to the common ground at headphone connector
LINOUTR	H2: pin 18	Ground referenced line output
LINOUTL	H3: pin 2	
LINOUTFB	H2: pin 20	LINE reference pin, recommended to be connected to the common ground at line output connector.
Charge Pump & VMID		
CPVOUTP	J7: pin 2	Charge Pump and VMIDC test points
CPVOUTN	J7: pin 1	
CPCA	J7: pin 4	
CPCB	J7: pin 3	
VMIDC	TP6	

Table 1 I/O Configuration

SHORTING POINTS AND JUMPER LINKS TABLE

REFERENCE	FUNCTION	
SP1	Short this pin to be able to use the onboard MIC connector. If shorted this links pin 1 of the MIC connector to LINPUT2 of the device	
J2	DBVDD	These jumpers link the relevant pins on the DUT to the different supply voltages.
J3	DCVDD	
J4	AVDD	To supply different voltages disconnect the relevant jumper link and apply the chosen voltage directly to pin 2 of the relevant jumper.
J5	MICVDD	
J6	CPVDD	
J8	HPOUTFB	These jumper links are set by default and connect the headphone and lineout reference to common ground.
J9	LINEOUTFB	

Table 2 Shorting Points and Jumper Links Table

BOARD CONFIGURATION WITH 6201-EV1-REV2 MAIN BOARD

This section focuses on evaluation of the WM8904-6201-FL32-M-REV1 Customer Mini Board in combination with the 6201-EV1-REV2 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

DAC TO HEADPHONE PLAYBACK

The following section details the configuration for DAC to headphone playback through HPOUTL/R. For board configuration, please refer to Figure 3

BLOCK DIAGRAM

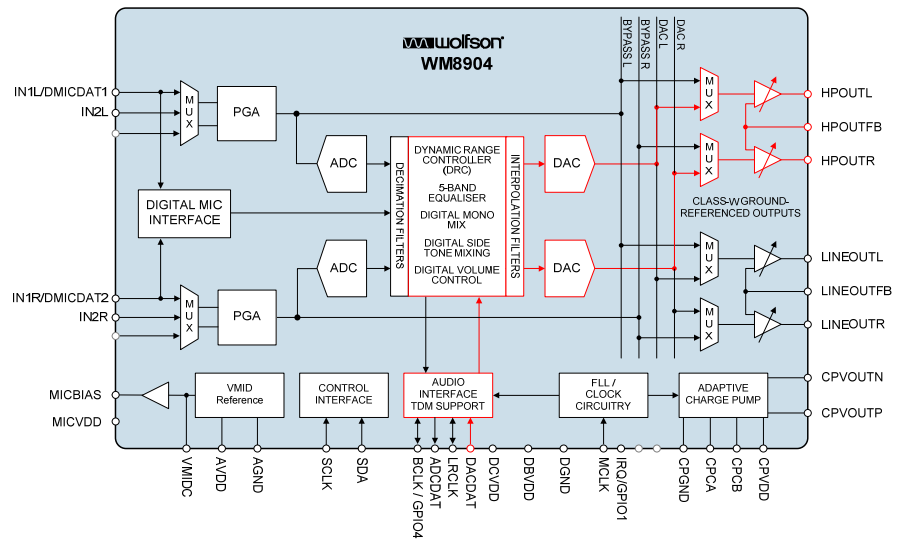


Figure 2 Path Diagram DAC to HPOUTL/R

BOARD CONFIGURATION

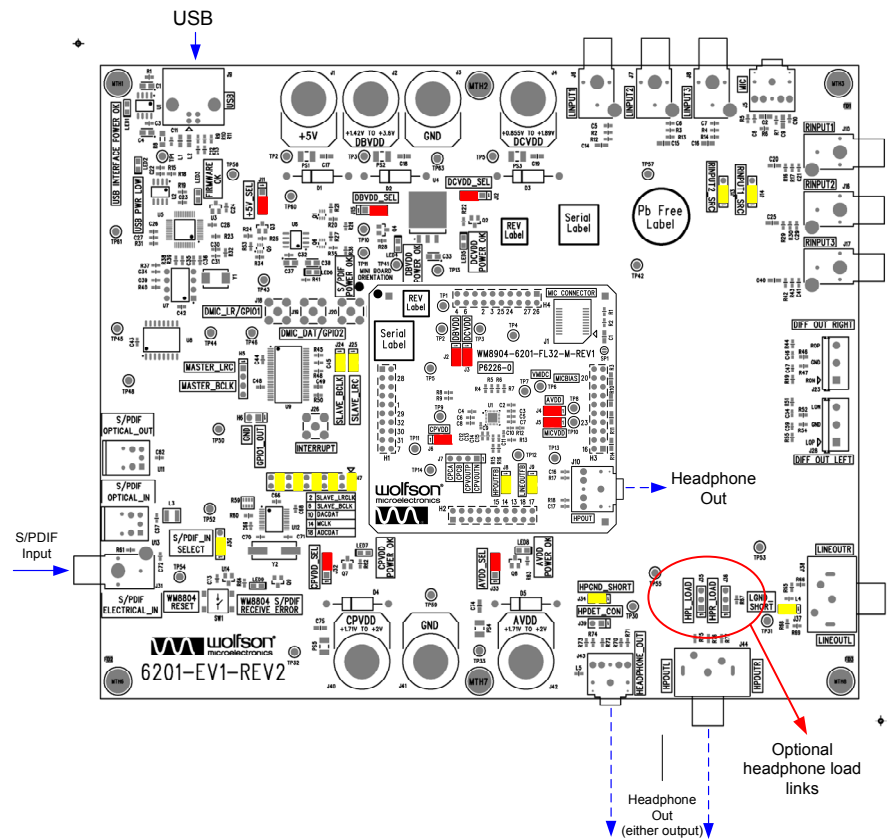


Figure 3 Board Configuration DAC to HPOUTL/R

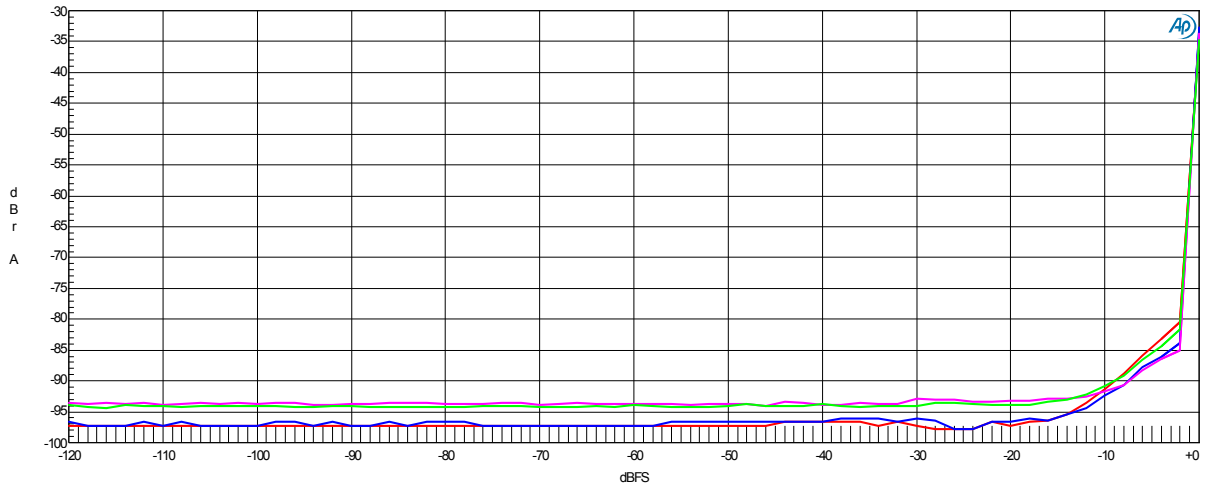
REGISTER SETTINGS

Register settings provided below are the typical sequence to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	SW Reset
0x6C	0x0100	WSEQ_ENA=1, WSEQ_WRITE_INDEX=0_0000
0x6F	0x0100	WSEQ_ABORT=0, WSEQ_START=1, WSEQ_START_INDEX=00_0000
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0 (Required for MMCs: SGY, KRT see erratum CE000546)
0x39	0x0039	HPOUTL_MUTE=0, HPOUT_VU=0, HPOUTLZC=0, HPOUTL_VOL=11_1001
0x3A	0x00B9	HPOUTR_MUTE=0, HPOUT_VU=1, HPOUTRZC=0, HPOUTR_VOL=11_1001
0x21	0x0000	DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_UNMUTE_RAMP=0, DAC_OSR128=0, DAC_MUTE=0, DEEMPH=00
0x68	0x0005	CP_DYN_PWR=1

Table 3 Register Settings DAC to HPOUTL/R

PERFORMANCE PLOT



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anir:THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Left
1	2	Blue	Solid	2	Anir:THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Right
2	1	Green	Solid	2	Anir:THD+N Ampl	Left	22Hz-20kHz, AES17, Left
2	2	Magenta	Solid	2	Anir:THD+N Ampl	Left	22Hz-20kHz, AES17, Right

System AP2
 Board: 6201-EV1-REV2 + WM8904-6201-FL32-M-REV1
 Device Date Code: 96AAKRT
 Input Path: SPDIF_IN
 Input Signal: 997Hz 0dBFS, 24-bit, 256fs (fs=48kHz)
 Output Path: HP-OUT (32R load)
 Output Reference: 0dBFS = -0.497 dBV
 Supplies: AVDD=CPVDD=DCVDD=1.8V, DVDD=1.8V, MCVDD=1.8V
 BW Filter: as stated
 Additional Filtering: as stated
 RMS or Averaging: Averaging

Figure 4 Performance Plot DAC to HPOUTL/R

IN1L/R TO ADC RECORDING

The following section details the configuration for IN1L/R to ADC recording. For board configuration, please refer to Figure 6.

BLOCK DIAGRAM

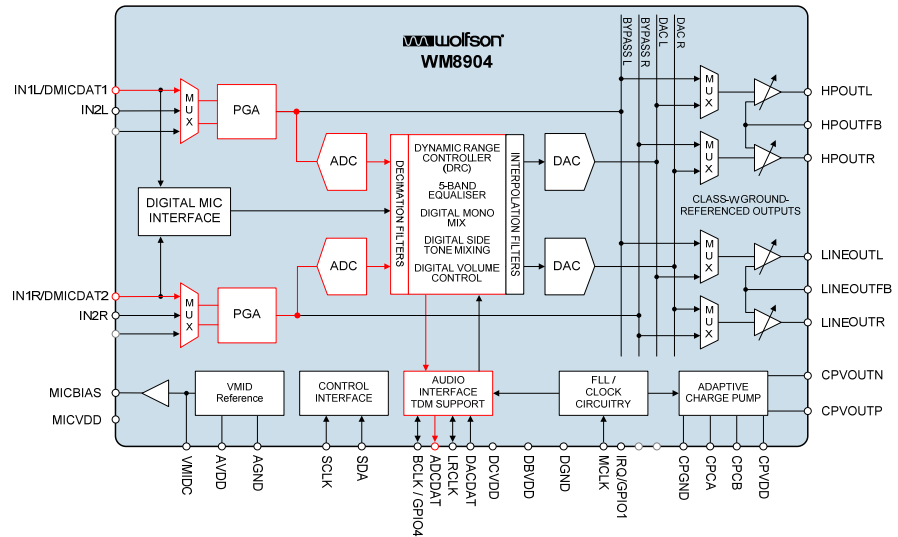


Figure 5 Path Diagram IN1L/R to ADC

BOARD CONFIGURATION

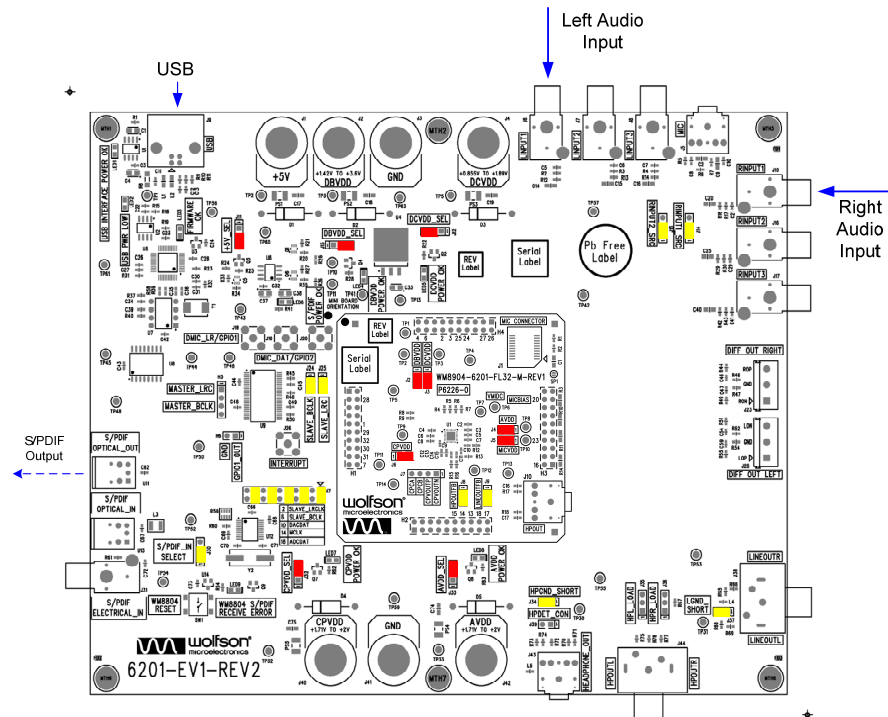


Figure 6 Board Configuration IN1L/R to ADC

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	SW Reset
0x04	0x0009	POBCTRL=0, ISEL=10, STARTUP_BIAS_ENA=0, BIAS_ENA=1
0x05	0x0043	VMID_BUF_ENA=1, VMID_RES=01, VMID_ENA=1
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0 (Required for MMCs: SGY, KRT see erratum CE000546)
0x0C	0x0003	INL_ENA=1, INR_ENA=1
0x12	0x0003	DACL_ENA=0, DACR_ENA=0, ADCL_ENA=1, ADCR_ENA=1
0x2C	0x0005	LINMUTE=0, LIN_VOL=0_0101
0x2D	0x0005	RINMUTE=0, RIN_VOL=0_0101

Table 4 Register Settings IN1L/R to ADC

PERFORMANCE PLOT

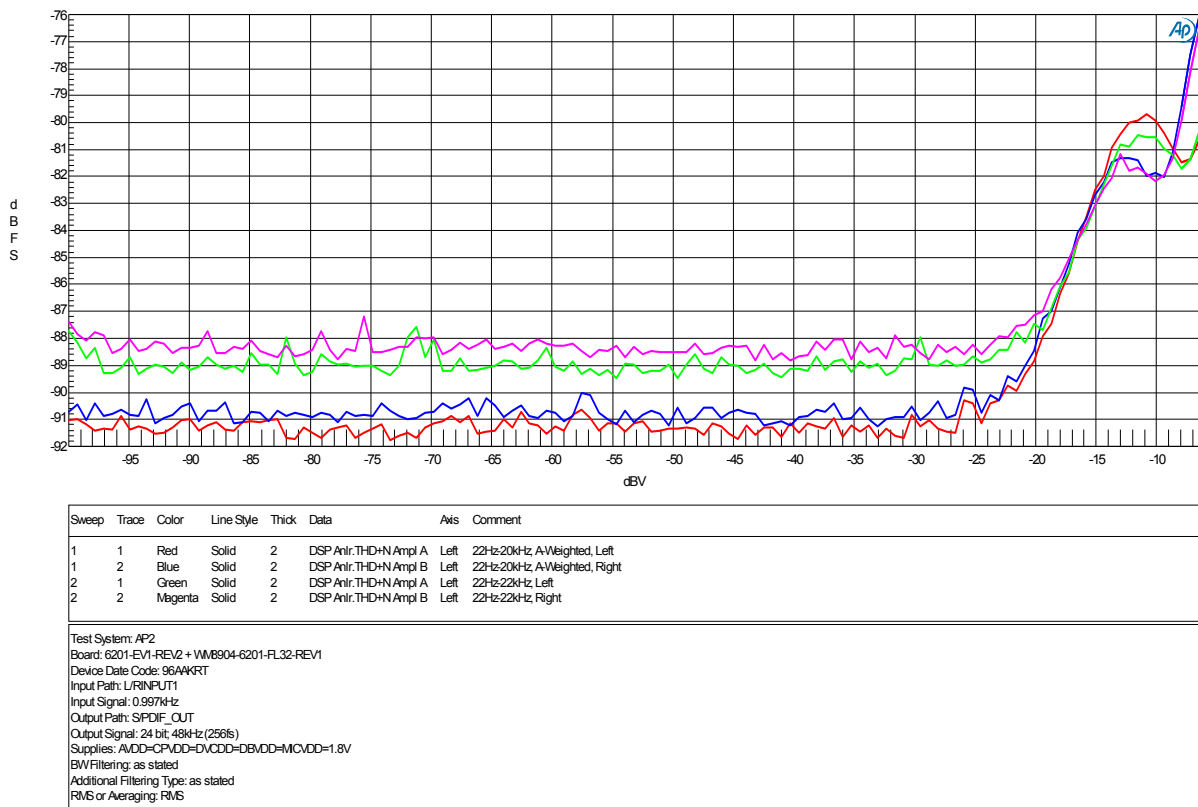


Figure 7 Performance Plot IN1L/R to ADC

REGISTER SETTINGS

Register settings provided below are the typical sequence to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	SW Reset
0x04	0x0019	POBCTRL=1, ISEL=10, STARTUP_BIAS_ENA=0, BIAS_ENA=1
0x05	0x0043	VMID_BUF_ENA=1, VMID_RES=01, VMID_ENA=1
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0 (Required for MMCs: SGY, KRT see erratum CE000546)
0x0C	0x0003	INL_ENA=1, INR_ENA=1
0x12	0x0003	DACL_ENA=0, DACR_ENA=0, ADCL_ENA=1, ADCR_ENA=1
0x2C	0x001F	LINMUTE=0, LIN_VOL=1_1111
0x2D	0x001F	RINMUTE=0, RIN_VOL=1_1111
0x2E	0x0046	INL_CM_ENA=1, L_IP_SEL_N=00, L_IP_SEL_P=01, L_MODE=10
0x2F	0x0046	INR_CM_ENA=1, R_IP_SEL_N=00, R_IP_SEL_P=01, R_MODE=10

Table 5 IN1L+2L / IN1R+2R to ADC (differential MIC input)

PERFORMANCE PLOT

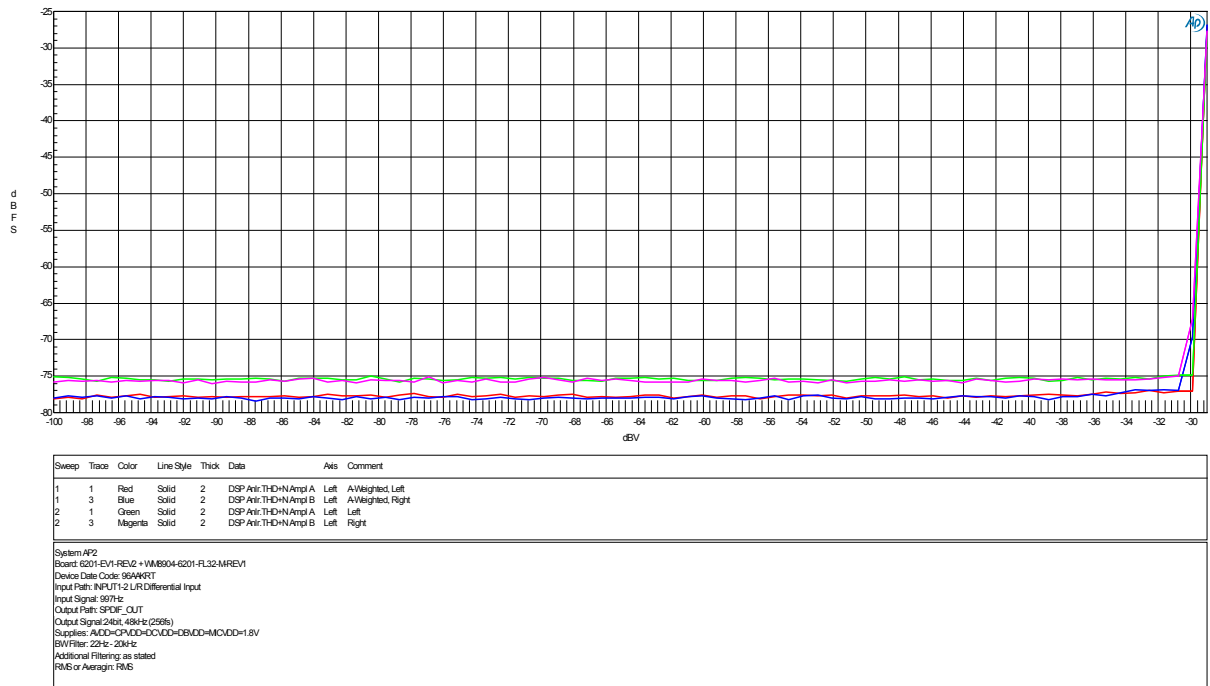


Figure 10 Performance Plot IN1L+2L / IN1R+2R to ADC (differential MIC)

IN1L/R TO LINEOUTL/R (ANALOGUE BYPASS)

The following section details the configuration of an analogue bypass from IN1L/R to LINEOUTL/R. For board configuration, please refer to Figure 12.

BLOCK DIAGRAM

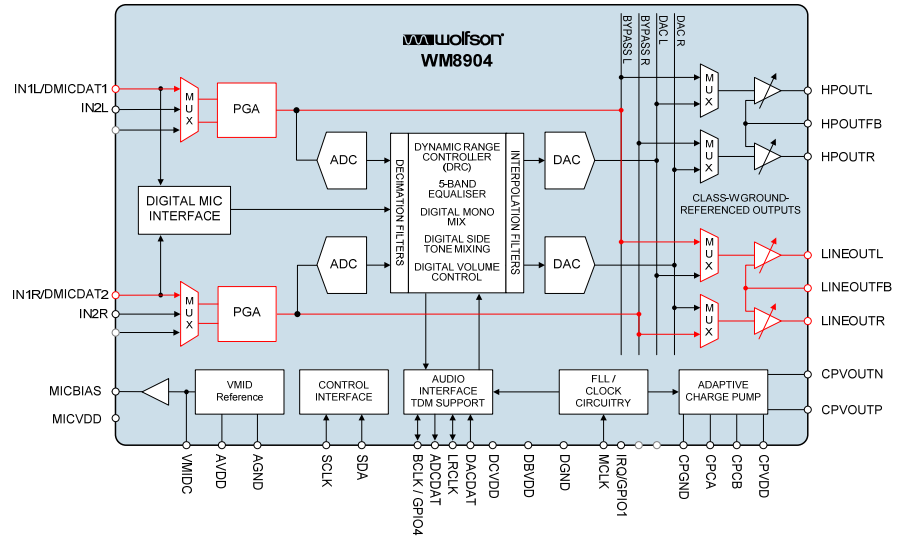


Figure 11 Path Diagram IN1L/R to LINEOUTL/R

BOARD CONFIGURATION

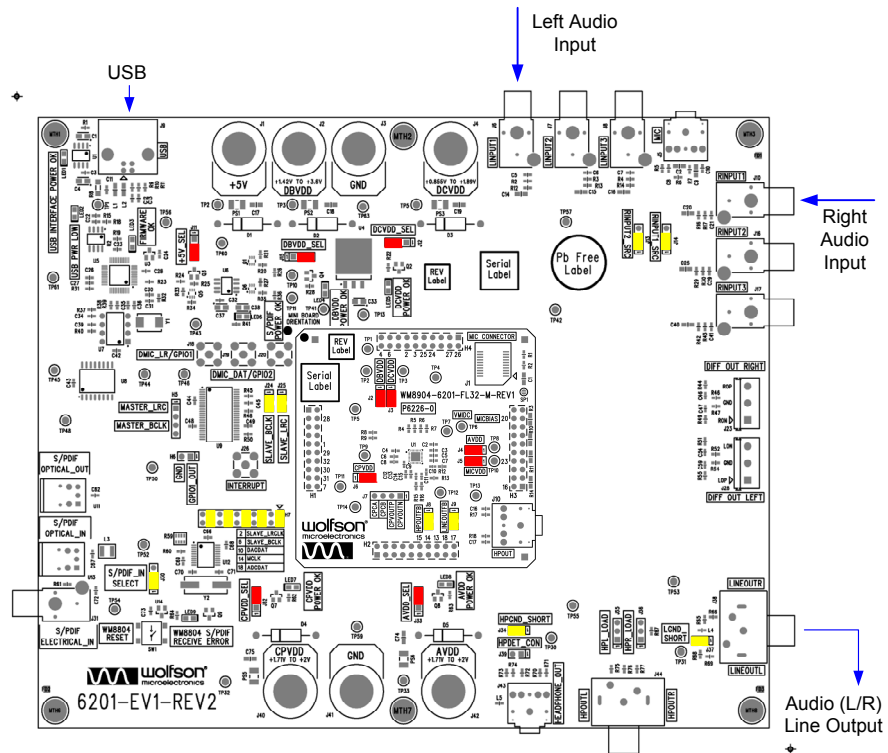


Figure 12 Board Configuration IN1L/R to LINEOUTL/R

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	SW Reset
0x04	0x0009	POBCTRL=0, ISEL=10, STARTUP_BIAS_ENA=0, BIAS_ENA=1
0x05	0x0043	VMID_BUF_ENA=1, VMID_RES=01, VMID_ENA=1
0x0C	0x0003	INL_ENA=1, INR_ENA=1
0x0F	0x0003	LINEOUTL_PGA_ENA=1, LINEOUTR_PGA_ENA=1
0x2C	0x0005	LINMUTE=0, LIN_VOL=0_0101
0x2D	0x0005	RINMUTE=0, RIN_VOL=0_0101
0x3D	0x0003	HPL_BYP_ENA=0, HPR_BYP_ENA=0, LINEOUTL_BYP_ENA=1, LINEOUTR_BYP_ENA=1
0x5E	0x00FF	LINEOUTL_RMV_SHORT=1, LINEOUTL_ENA_OUTP=1, LINEOUTL_ENA_DLY=1, LINEOUTL_ENA=1, LINEOUTR_RMV_SHORT=1, LINEOUTR_ENA_OUTP=1, LINEOUTR_ENA_DLY=1, LINEOUTR_ENA=1
0x62	0x0001	CP_ENA=1

Table 6 Register Settings IN1L/R to LINEOUTL/R

PERFORMANCE PLOT

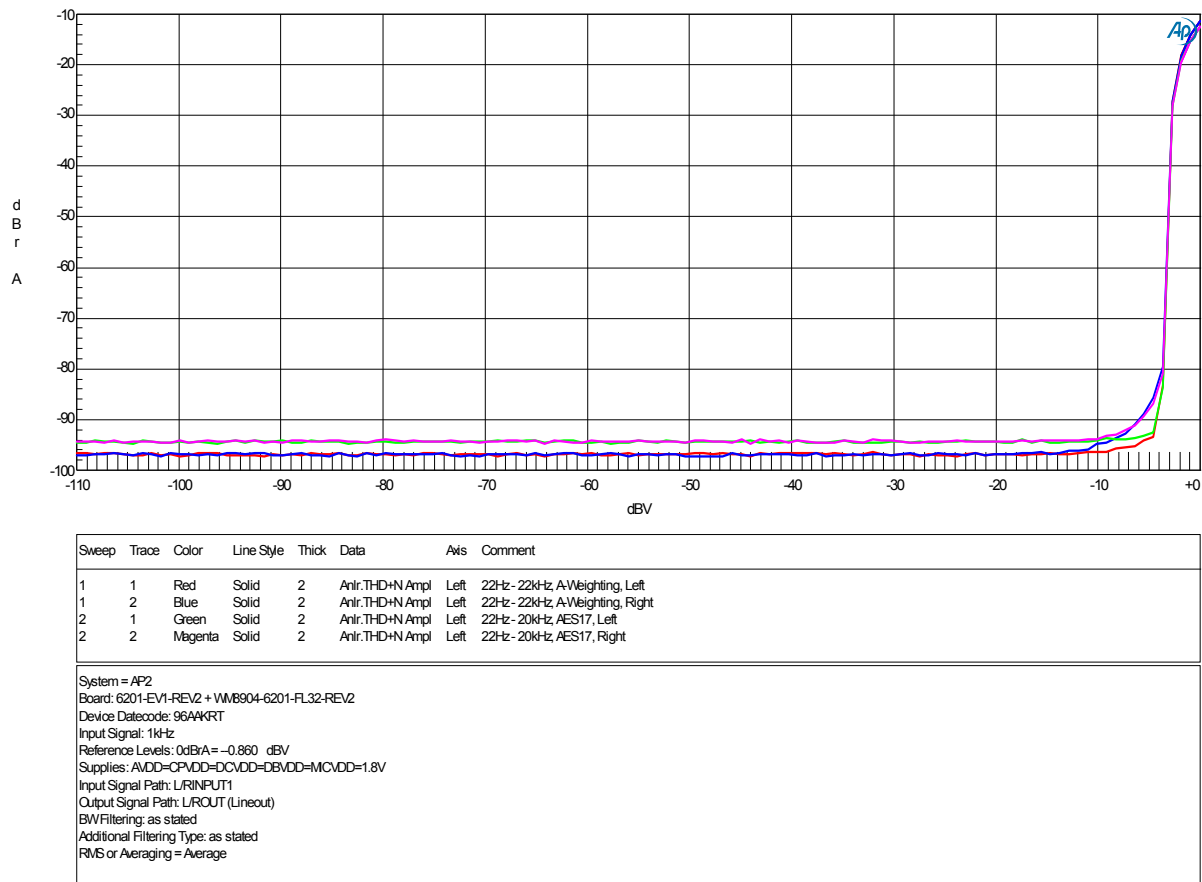


Figure 13 Performance Plot (IN1L/R to LINEOUTL/R)

IN1L/R TO LINEOUTL/R (DIGITAL LOOPBACK)

The following section details the configuration for the digital loopback path.

BLOCK DIAGRAM

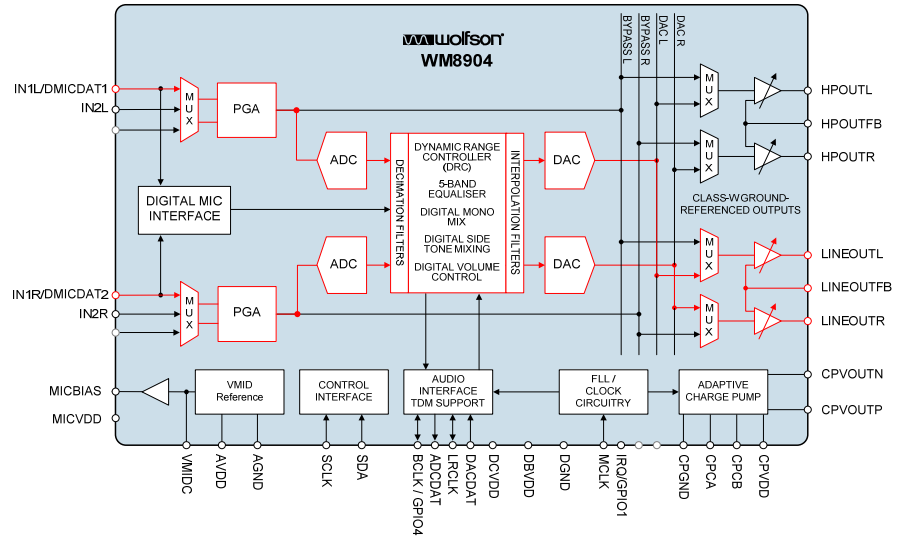


Figure 14 Path Diagram IN1L/R to LINEOUTL/R (digital loopback)

BOARD CONFIGURATION

The board configuration for this path is equivalent to the one used for the analogue bypass. See Figure 12 for reference.

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	SW Reset
0x04	0x0019	POBCTRL=1, ISEL=10, STARTUP_BIAS_ENA=0, BIAS_ENA=1
0x05	0x0043	VMID_BUF_ENA=1, VMID_RES=01, VMID_ENA=1
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0 (Required for MMCs: SGY, KRT see erratum CE000546)
0x0C	0x0003	INL_ENA=1, INR_ENA=1
0x0F	0x0003	LINEOUTL_PGA_ENA=1, LINEOUTR_PGA_ENA=1
0x12	0x000F	DACL_ENA=1, DACR_ENA=1, ADCL_ENA=1, ADCR_ENA=1
0x18	0x0150	DACL_DATINV=0, DACR_DATINV=0, DAC_BOOST=00, LOOPBACK=1, AIFADCL_SRC=0, AIFADCR_SRC=1, AIFDACL_SRC=0, AIFDACR_SRC=1, ADC_COMP=0, ADC_COMPMODE=0, DAC_COMP=0, DAC_COMPMODE=0
0x21	0x0000	DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_UNMUTE_RAMP=0, DAC_OSR128=0, DAC_MUTE=0, DEEMPH=00
0x2C	0x0005	LINMUTE=0, LIN_VOL=0_0101
0x2D	0x0005	RINMUTE=0, RIN_VOL=0_0101
0x5E	0x00FF	LINEOUTL_RMV_SHORT=1, LINEOUTL_ENA_OUTP=1, LINEOUTL_ENA_DLY=1, LINEOUTL_ENA=1, LINEOUTR_RMV_SHORT=1, LINEOUTR_ENA_OUTP=1, LINEOUTR_ENA_DLY=1, LINEOUTR_ENA=1
0x68	0x0005	CP_DYN_PWR=1
0x62	0x0001	CP_ENA=1

Table 7 Register Settings IN1L/R to LINEOUTL/R (digital loopback)

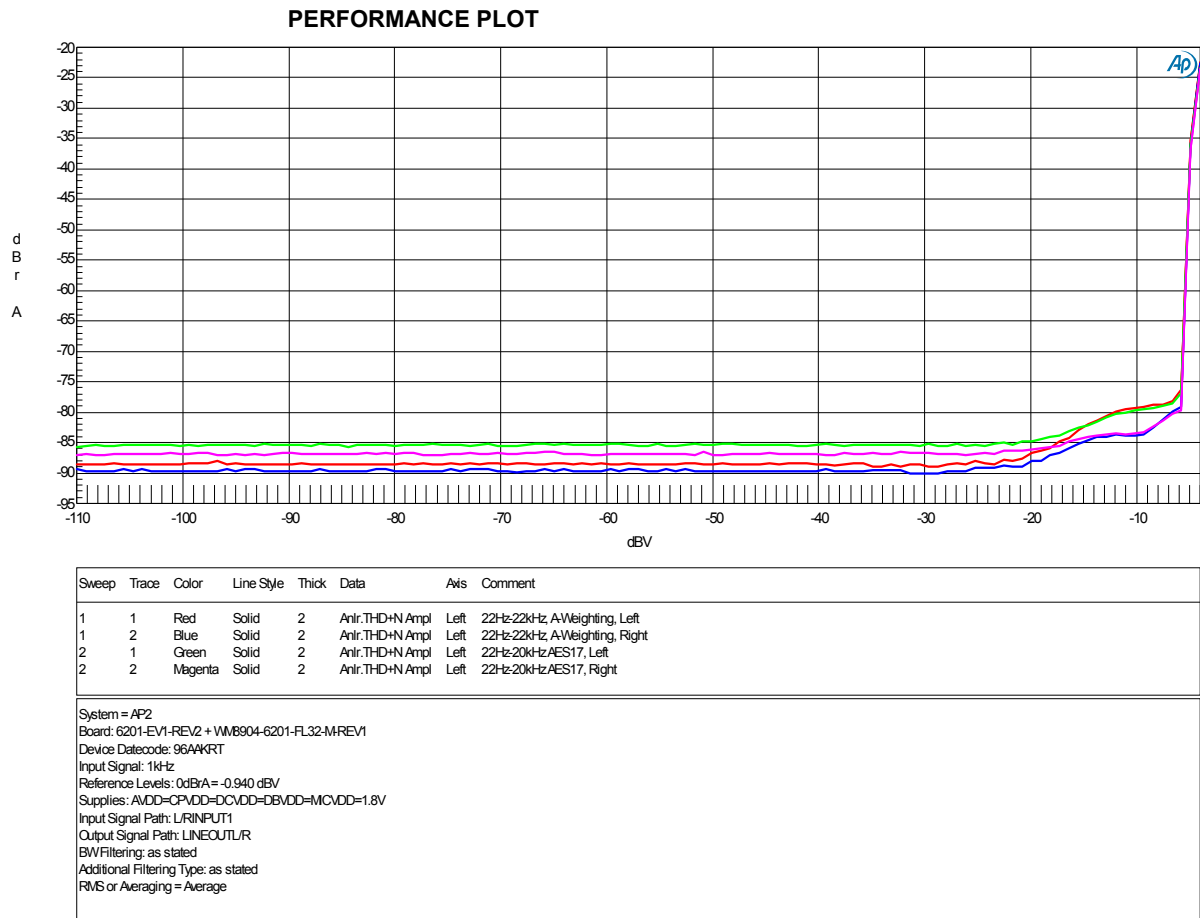


Figure 15 Performance Plot IN1L/R to LINEOUTL/R (digital loopback)

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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