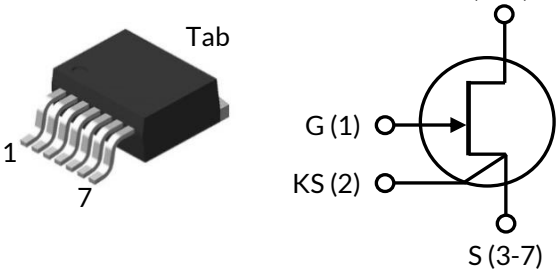
DATASHEET

UF3N170400B7S

1700V-400mΩ SiC Normally-on JFET

Preliminary, February 2020



Part Number	Package	Marking
UF3N170400B7S	D^2PAK-7L	UF3N170400B7S

Description

UnitedSiC offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- Typical on-resistance $R_{DS(on),typ}$ of 400mΩ
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical applications

- Over Current Protection Circuits
- DC-AC Inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1700	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC [1]	-30 to +20	V
Continuous drain current [2]	I_D	T_C = 25°C	6.8	A
		T_C = 100°C	5.1	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	16	A
Power dissipation	P_{tot}	T_C = 25°C	68	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 3	260	°C

1. +20V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by $T_{J,max}$
3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			1.7	2.2	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=-20V, I_D=0.3mA	1700			V
Total drain leakage current	I_{DSS}	V_{DS}=1700V, V_{GS}=-20V, T_J=25°C		2.2	60	µA
		V_{DS}=1700V, V_{GS}=-20V, T_J=175°C		9		
Total gate leakage current	I_{GSS}	V_{GS}=-20V, T_J=25°C		0.15	6	µA
		V_{GS}=-20V, T_J=175°C		0.8		µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=2V, I_D=5A, T_J=25°C		350		mΩ
		V_{GS}=0V, I_D=5A, T_J=25°C		400	500	
		V_{GS}=2V, I_D=5A, T_J=175°C		928		
		V_{GS}=0V, I_D=5A, T_J=175°C		1040		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=4.5mA	-14	-9.5	-6	V
Gate resistance	R_G	f=1MHz, open drain		5		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=-20V f=100kHz		225		pF
Output capacitance	C_{oss}			22		
Reverse transfer capacitance	C_{rss}			18		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 1200V, V_{GS}=-20V		11.4		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=1200V, V_{GS}=-20V		8.2		µJ
Total gate charge	Q_G	V_{DS}=1200V, I_D=5A, V_{GS} = -18V to 0V		30		nC
Gate-drain charge	Q_{GD}			17		
Gate-source charge	Q_{GS}			5		
Turn-on delay time	$t_{d(on)}$	V_{DS}=1200V, I_D=5A, Gate Driver =-18V to 0V, R_G=1Ω, Inductive Load, FWD: 2x UJ3D1210TS in series T_J=25°C		5		ns
Rise time	t_r			19		
Turn-off delay time	$t_{d(off)}$			9		
Fall time	t_f			37		
Turn-on energy	E_{ON}			125		µJ
Turn-off energy	E_{OFF}			38		
Total switching energy	E_{TOTAL}			163		
Turn-on delay time	$t_{d(on)}$	V_{DS}=1200V, I_D=5A, Gate Driver =-18V to 0V, R_G=1Ω, Inductive Load, FWD: 2x UJ3D1210TS in series, T_J=150°C		5		ns
Rise time	t_r			16		
Turn-off delay time	$t_{d(off)}$			8		
Fall time	t_f			34		
Turn-on energy	E_{ON}			114		µJ
Turn-off energy	E_{OFF}			31		
Total switching energy	E_{TOTAL}			145		

Typical Performance Diagrams

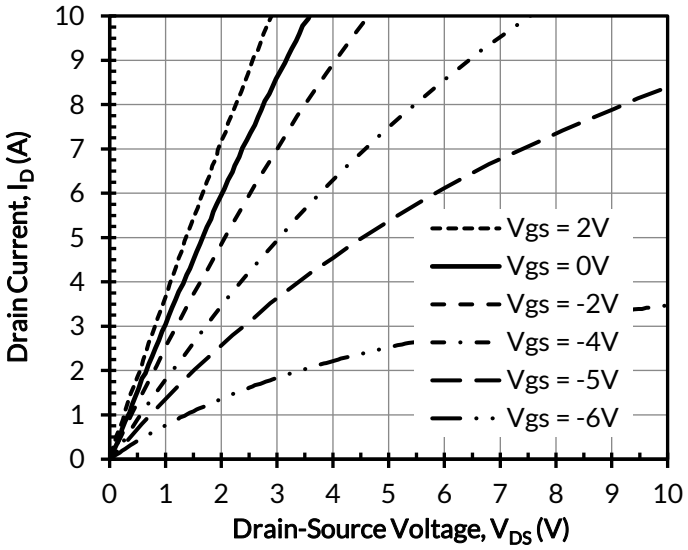


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

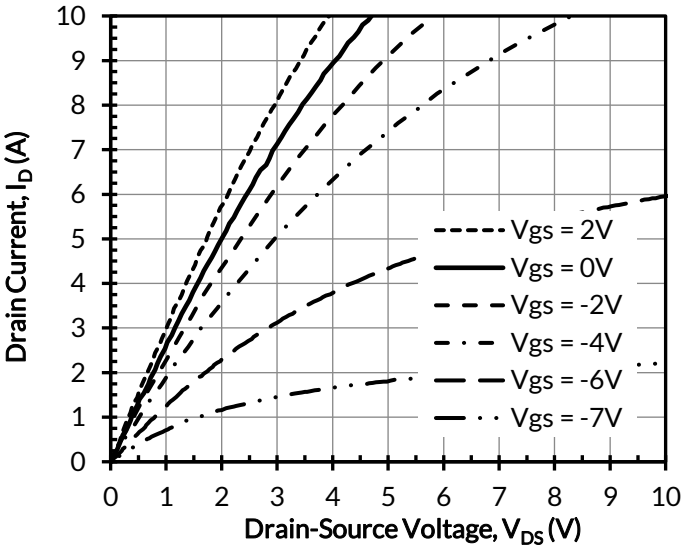


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

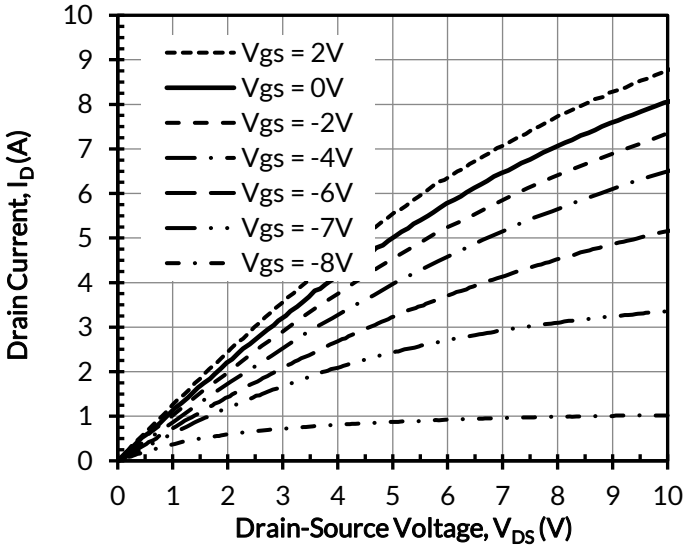


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

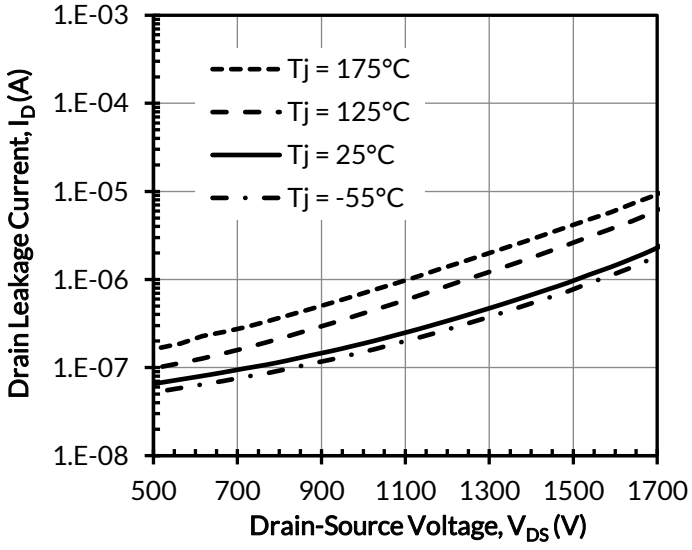


Figure 4. Typical drain-source leakage at V_{GS} = -20V

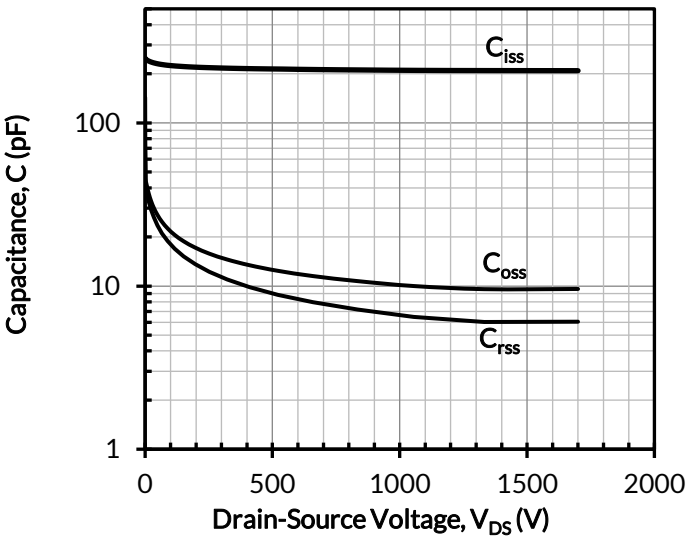


Figure 5. Typical capacitances at f = 100kHz and V_{GS} = -20V

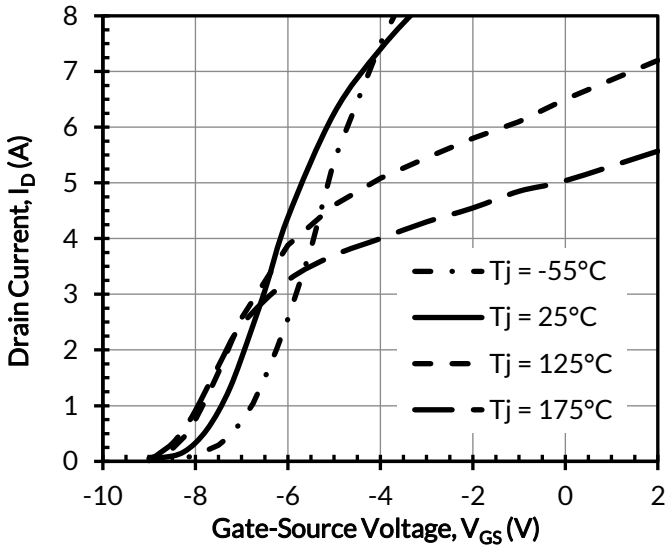


Figure 6. Typical transfer characteristics at V_{DS} = 5V

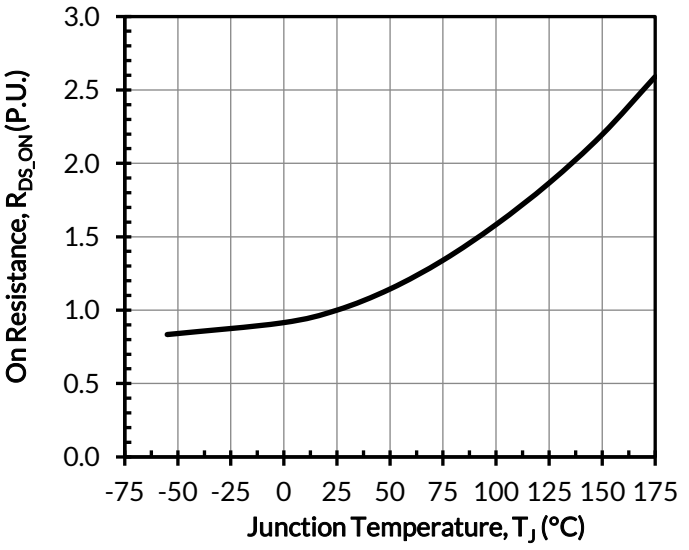


Figure 7. Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 5A

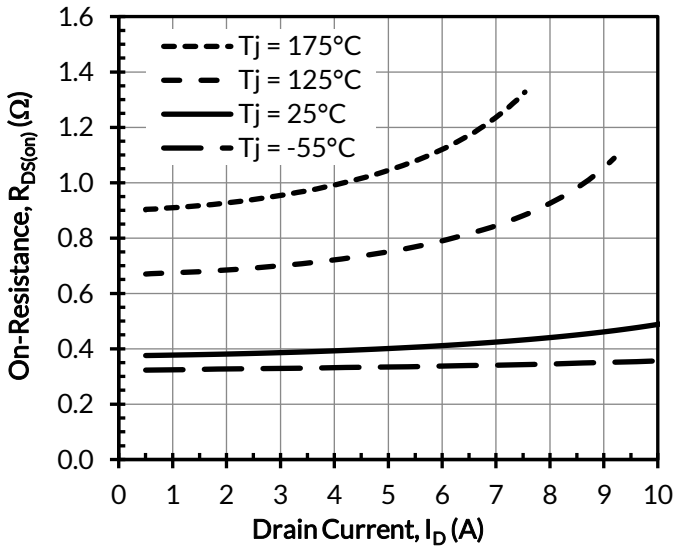


Figure 8. Typical drain-source on-resistances at V_{GS} = 0V

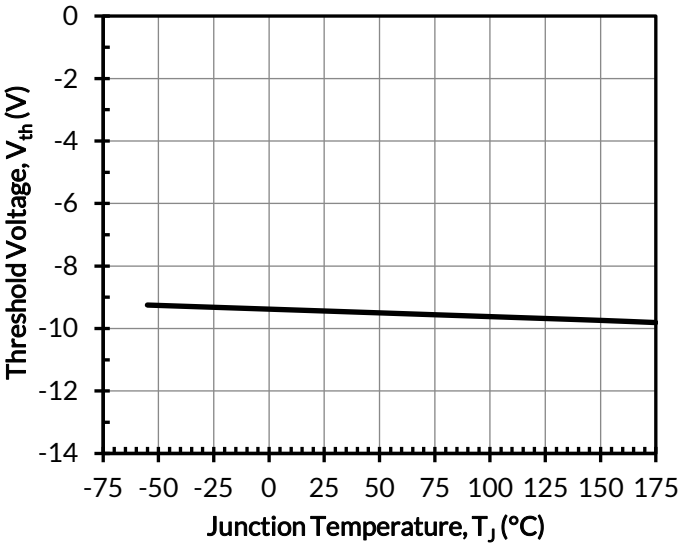


Figure 9. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 4.5mA

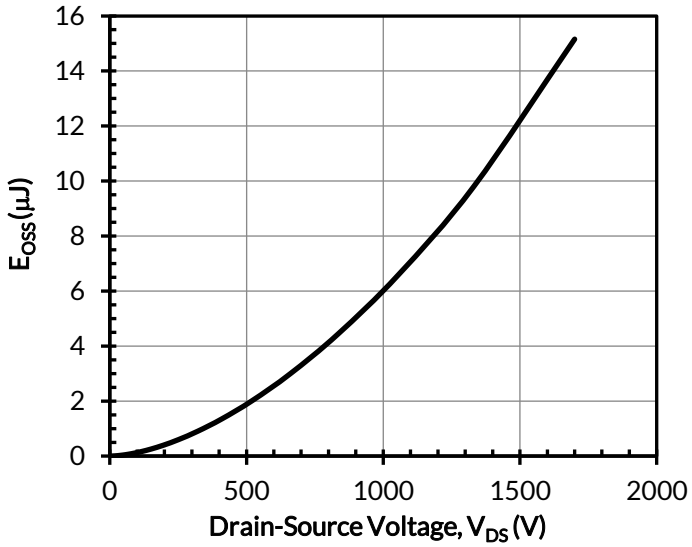


Figure 10. Typical stored energy in C_{OSS} at V_{GS} = -20V

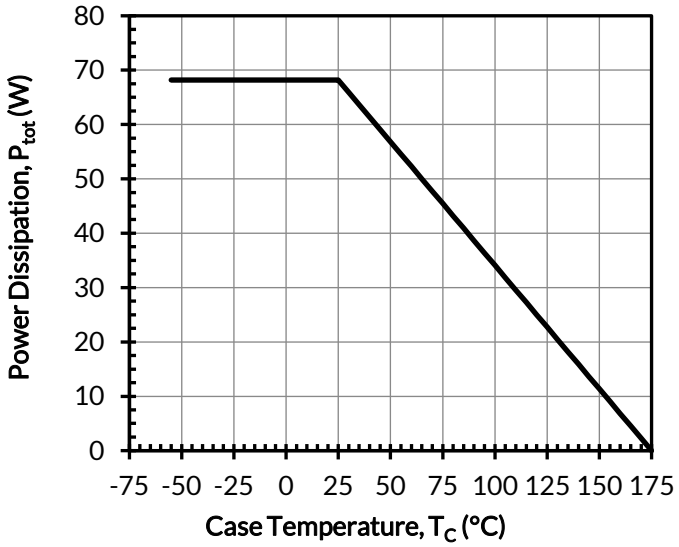


Figure 11. Total power Dissipation

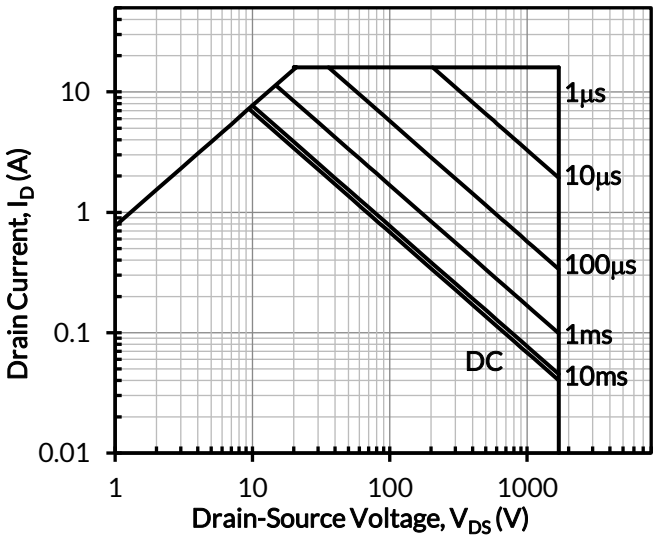


Figure 12. Safe operation area at T_C =25°C, Parameter t_p

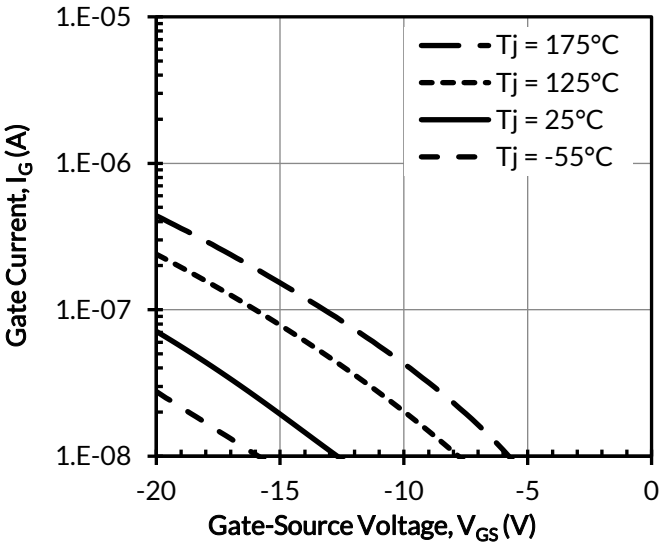


Figure 13. Typical gate leakage at V_{DS} = 0V

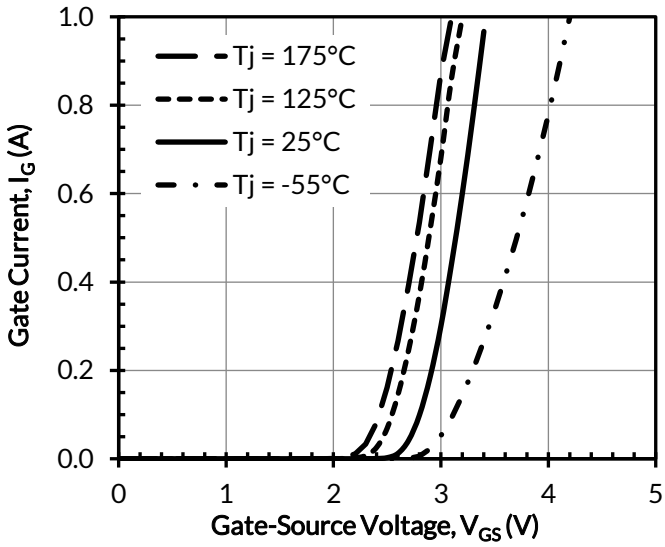


Figure 14. Typical gate forward current at V_{DS} = 0V

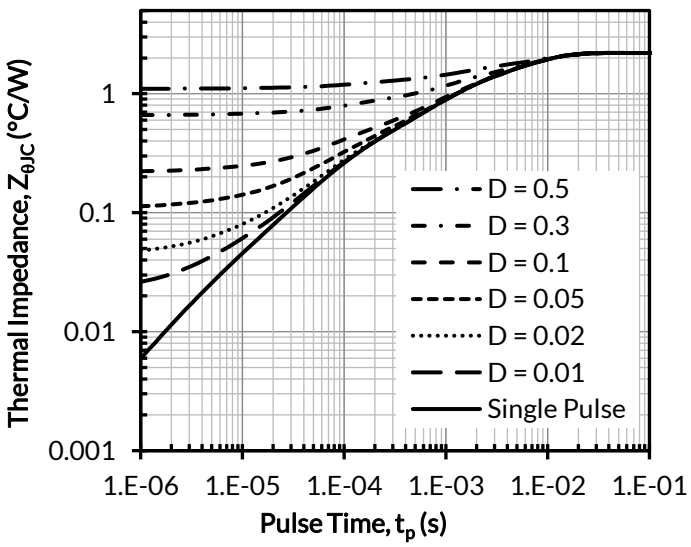


Figure 15. Maximum transient thermal impedance

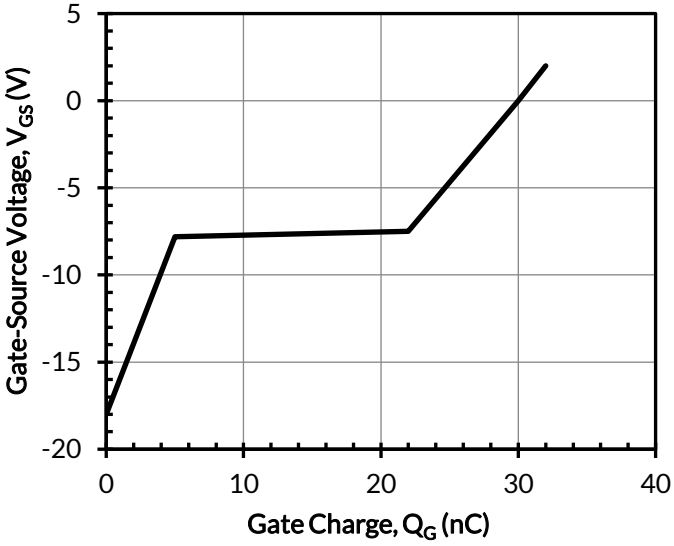


Figure 16. Typical gate charge at V_{DS} = 1200V and I_D = 5A

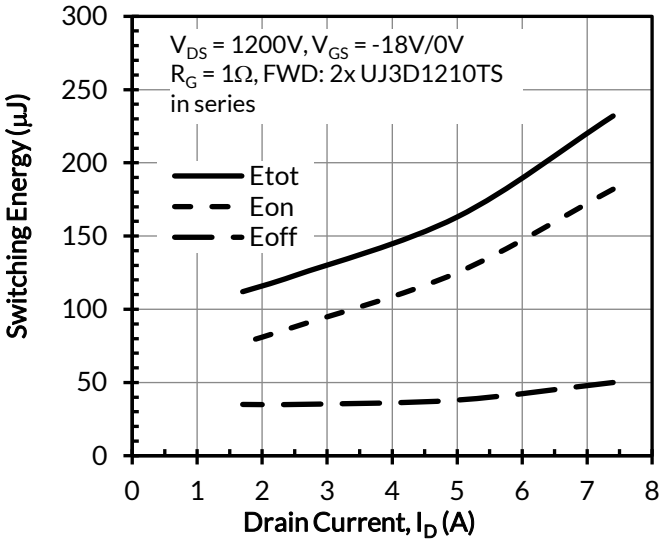


Figure 17. Clamped inductive switching energy vs. drain current at T_J = 25°C

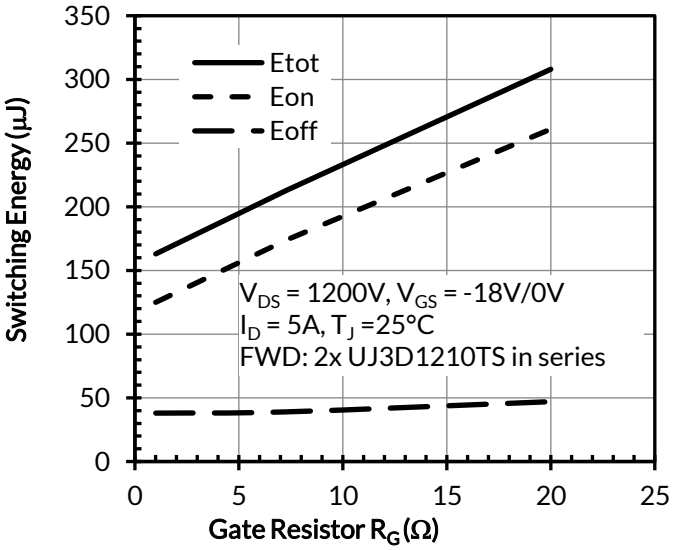


Figure 18. Clamped inductive switching energy vs. gate resistor R_G

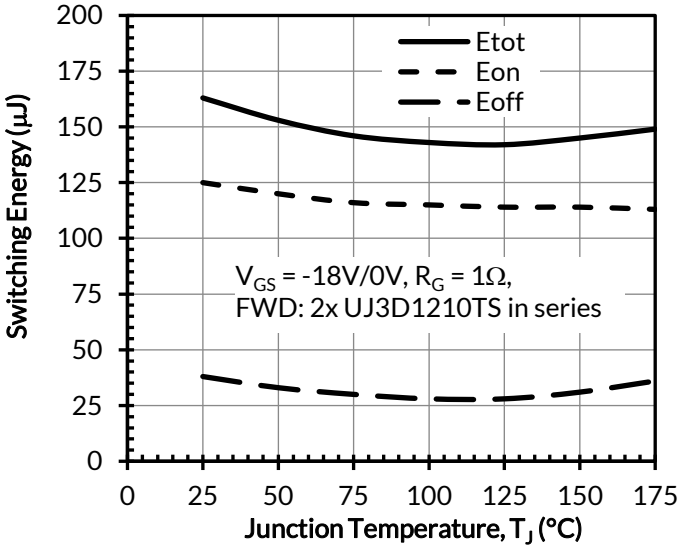


Figure 19. Clamped inductive switching energy vs. junction temperature at V_{DS} = 1200V and I_D = 5A

Disclaimer

UnitedSiC reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. UnitedSiC assumes no responsibility or liability for any errors or inaccuracies within.

Information on all products and contained herein is intended for description only. No license, express or implied, to any intellectual property rights is granted within this document.

UnitedSiC assumes no liability whatsoever relating to the choice, selection or use of the UnitedSiC products and services described herein.