



TISP4125H3BJ/TISP4219H3BJ,
TISP4125M3BJ/TISP4219M3BJ

**LCAS RING AND TIP PROTECTION PAIRS
BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS**

TISP4xxxH3/M3BJ Series for LCAS Protection

Customized Voltage for LCAS Protection

Battery-Backed Ringing 87 V rms
Ground-Backed Ringing 101 V rms

Device	V _{DRM} V	V _(BO) V	LCAS TERMINAL
'4125	100	125	TIP
'4219	180	219	RING

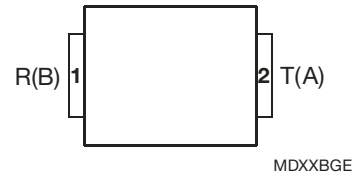
Low Differential Capacitance 39 pF max.

..... UL Recognized Components

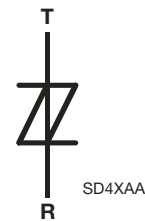
Rated for International Surge Wave Shapes

Wave Shape	Standard	I _{TSP} A	
		H3 SERIES	M3 SERIES
2/10 μs	GR-1089-CORE	500	300
8/20 μs	IEC 61000-4-5	300	220
10/160 μs	FCC Part 68	250	120
10/700 μs	ITU-T K.20/21/45	200	100
10/560 μs	FCC Part 68	160	75
10/1000 μs	GR-1089-CORE	100	50

SMBJ Package (Top View)



Device Symbol



Terminals T and R correspond to the alternative line designators of A and B

Description

These protector pairs have been formulated to limit the peak voltages on the line terminals of the '7581/2/3 LCAS (Line Card Access Switches) type devices. An LCAS may also be referred to as a Solid State Relay, SSR, i.e. a replacement of the conventional electro-mechanical relay.

Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. These overvoltages are initially clipped by protector breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. For negative surges, the high crowbar holding current helps prevent d.c. latchup with the SLIC current, as the surge current subsides.

Each protector consists of a symmetrical voltage-triggered bidirectional thyristor. They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities.

How to Order

Device	Package	Carrier	Order As
TISP4125H3BJ	BJ (J-Bend DO-214AA/SMB)	Embossed Tape Reeled	TISP4125H3BJR-S
TISP4219H3BJ			TISP4219H3BJR-S
TISP4125M3BJ			TISP4125M3BJR-S
TISP4219M3BJ			TISP4219M3BJR-S



WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

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*RoHS Directive 2002/95/EC Jan. 27, 2003 including Annex.

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TISP4xxxH3/M3BJ Series for LCAS Protection

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TISP4125H3BJ & TISP4219H3BJ

Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	V_{DRM}	± 100	V
		± 180	
Non-repetitive peak on-state pulse current (see Notes 2 and 3)	I_{TSP}	500	A
2/10 μs (GR-1089-CORE, 2/10 μs voltage wave shape)		300	
8/20 μs (IEC 61000-4-5, 1.2/50 μs voltage, 8/20 current combination wave generator)		250	
10/160 μs (FCC Part 68, 10/160 μs voltage wave shape)		220	
5/200 μs (VDE 0433, 10/700 μs voltage wave shape)		200	
0.2/310 μs (I3124, 0.5/700 μs voltage wave shape)		200	
5/310 μs (ITU-T K.20/21, 10/700 μs voltage wave shape)		200	
5/310 μs (FTZ R12, 10/700 μs voltage wave shape)		160	
10/560 μs (FCC Part 68, 10/560 μs voltage wave shape)		100	
10/1000 μs (GR-1089-CORE, 10/1000 μs voltage wave shape)			
Non-repetitive peak on-state current (see Notes 2, 3 and 4)	I_{TSM}	55	A
20 ms (50 Hz) full sine wave		60	
16.7 ms (60 Hz) full sine wave		2.1	
1000 s 50 Hz/60 Hz a.c.			
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A	di_T/dt	400	A/ μs
Junction temperature	T_J	-40 to +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

- NOTES: 1. See Applications Information for voltage values at lower temperatures.
 2. Initially, the TISP4xxxH3BJ must be in thermal equilibrium with $T_J = 25\text{ }^\circ\text{C}$.
 3. The surge may be repeated after the TISP4xxxH3BJ returns to its initial conditions.
 4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 10 for the current ratings at other durations. Derate current values at $-0.61\text{ }^\circ\text{C}$ for ambient temperatures above $25\text{ }^\circ\text{C}$.

Recommended Operating Conditions

Component	Condition	Min	Typ	Max	Unit
R_S Series current limiting resistor	GR-1089-CORE first-level surge survival	0			Ω
	GR-1089-CORE first-level and second-level surge survival	0			Ω
	K.20, K.21 and K.45 coordination pass with a 400 V primary protector	6			Ω
V_{RING} AC ringing voltage	Figure 12, $V_{BAT} = -48\text{ V} \pm 2.5\text{ V}$, $R1 = R2 = 300\text{ }\Omega$, $0\text{ }^\circ\text{C} < T_A < +85\text{ }^\circ\text{C}$	Battery-backed		87	V rms
		Ground-backed		101	V rms

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TISP4xxxH3/M3BJ Series for LCAS Protection

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Electrical Characteristics, TISP4xxxH3, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_D = V_{DRM}$ $T_A = 25\text{ }^\circ\text{C}$ $T_A = 85\text{ }^\circ\text{C}$			± 5 ± 10	μA
$V_{(BO)}$ Breakover voltage	$dv/dt = \pm 250\text{ V/ms}$, $R_{SOURCE} = 300\ \Omega$	'4125 '4219		± 125 ± 219	V
$V_{(BO)}$ Impulse breakover voltage	$dv/dt \leq \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $di/dt = \pm 20\text{ A}/\mu\text{s}$, Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$	'4125 '4219		± 134 ± 229	V
$I_{(BO)}$ Breakover current	$dv/dt = \pm 250\text{ V/ms}$, $R_{SOURCE} = 300\ \Omega$	± 0.15		± 0.6	A
V_T On-state voltage	$I_T = \pm 5\text{ A}$, $t_W = 100\ \mu\text{s}$			± 3	V
I_H Holding current	$I_T = \pm 5\text{ A}$, $di/dt = \pm 30\text{ mA/ms}$	± 0.15		± 0.6	A
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value $< 0.85V_{DRM}$	± 5			$\text{kV}/\mu\text{s}$
I_D Off-state current	$V_D = \pm 50\text{ V}$ $T_A = 85\text{ }^\circ\text{C}$			± 10	μA
C_{off} Off-state capacitance	$f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = 0$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -1\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -2\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -50\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -100\text{ V}$ (see Note 5)		80 71 65 30 23	90 79 74 35 28	pF

NOTE 5: To avoid possible voltage clipping, the '4125 is tested with $V_D = -98\text{ V}$.

Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$ Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$, (see Note 6)			113	$^\circ\text{C}/\text{W}$
	265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$		50		

NOTE 6: EIA/JESD51-2 environment and the PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

TISP4xxxH3/M3BJ Series for LCAS Protection

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TISP4125M3BJ & TISP4219M3BJ

Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 7)	V_{DRM}	± 100 ± 180	V
Non-repetitive peak on-state pulse current (see Notes 8 and 9)	I_{TSP}		A
2/10 μs (GR-1089-CORE, 2/10 μs voltage wave shape)		300	
8/20 μs (IEC 61000-4-5, 1.2/50 μs voltage, 8/20 current combination wave generator)		220	
10/160 μs (FCC Part 68, 10/160 μs voltage wave shape)		120	
5/200 μs (VDE 0433, 10/700 μs voltage wave shape)		110	
0.2/310 μs (I3124, 0.5/700 μs voltage wave shape)		100	
5/310 μs (ITU-T K.20/21, 10/700 μs voltage wave shape)		100	
5/310 μs (FTZ R12, 10/700 μs voltage wave shape)		100	
10/560 μs (FCC Part 68, 10/560 μs voltage wave shape)		75	
10/1000 μs (GR-1089-CORE, 10/1000 μs voltage wave shape)		50	
Non-repetitive peak on-state current (see Notes 8, 9 and 10)	I_{TSM}		A
20 ms (50 Hz) full sine wave		30	
16.7 ms (60 Hz) full sine wave		32	
1000 s 50 Hz/60 Hz a.c.		2.1	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A	di_T/dt	300	A/ μs
Junction temperature	T_J	-40 to +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

- NOTES: 7. See Applications Information for voltage values at lower temperatures.
 8. Initially, the TISP4xxxM3BJ must be in thermal equilibrium with $T_J = 25\text{ }^\circ\text{C}$.
 9. The surge may be repeated after the TISP4xxxM3BJ returns to its initial conditions.
 10. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 11 for the current ratings at other durations. Derate current values at $-0.61\text{ }^\circ\text{C}$ for ambient temperatures above $25\text{ }^\circ\text{C}$.

Recommended Operating Conditions

Component	Condition	Min	Typ	Max	Unit
R_S Series current limiting resistor	GR-1089-CORE first-level surge survival	10			Ω
	GR-1089-CORE first-level and second-level surge survival	12			Ω
	K.20, K.21 and K.45 coordination pass with a 400 V primary protector	6			Ω
V_{RING} AC ringing voltage	Figure 12, $V_{BAT} = -48\text{ V} \pm 2.5\text{ V}$, $R1 = R2 = 300\text{ }\Omega$, $0\text{ }^\circ\text{C} < T_A < +85\text{ }^\circ\text{C}$	Battery-backed		87	V rms
		Ground-backed		101	V rms

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TISP4xxxH3/M3BJ Series for LCAS Protection

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Electrical Characteristics, TISP4xxxM3, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_D = V_{DRM}$ $T_A = 25\text{ }^\circ\text{C}$ $T_A = 85\text{ }^\circ\text{C}$			± 5 ± 10	μA
$V_{(BO)}$ Breakover voltage	$dv/dt = \pm 250\text{ V/ms}$, $R_{SOURCE} = 300\ \Omega$	'4125 '4219		± 125 ± 219	V
$V_{(BO)}$ Impulse breakover voltage	$dv/dt \leq \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $di/dt = \pm 20\text{ A}/\mu\text{s}$, Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$	'4125 '4219		± 132 ± 226	V
$I_{(BO)}$ Breakover current	$dv/dt = \pm 250\text{ V/ms}$, $R_{SOURCE} = 300\ \Omega$	± 0.15		± 0.6	A
V_T On-state voltage	$I_T = \pm 5\text{ A}$, $t_W = 100\ \mu\text{s}$			± 3	V
I_H Holding current	$I_T = \pm 5\text{ A}$, $di/dt = \pm 30\text{ mA/ms}$	± 0.15		± 0.6	A
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value $< 0.85V_{DRM}$	± 5			$\text{kV}/\mu\text{s}$
I_D Off-state current	$V_D = \pm 50\text{ V}$ $T_A = 85\text{ }^\circ\text{C}$			± 10	μA
C_{off} Off-state capacitance	$f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = 0$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -1\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -2\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -50\text{ V}$, $f = 1\text{ MHz}$, $V_d = 1\text{ V rms}$, $V_D = -100\text{ V}$ (see Note 11)		62 56 52 26 21	74 67 62 31 25	pF

NOTE 11: To avoid possible voltage clipping, the '4125 is tested with $V_D = -98\text{ V}$.

Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$ Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$, (see Note 12)			115	$^\circ\text{C}/\text{W}$
	265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$		52		

NOTE 12: EIA/JESD51-2 environment and the PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

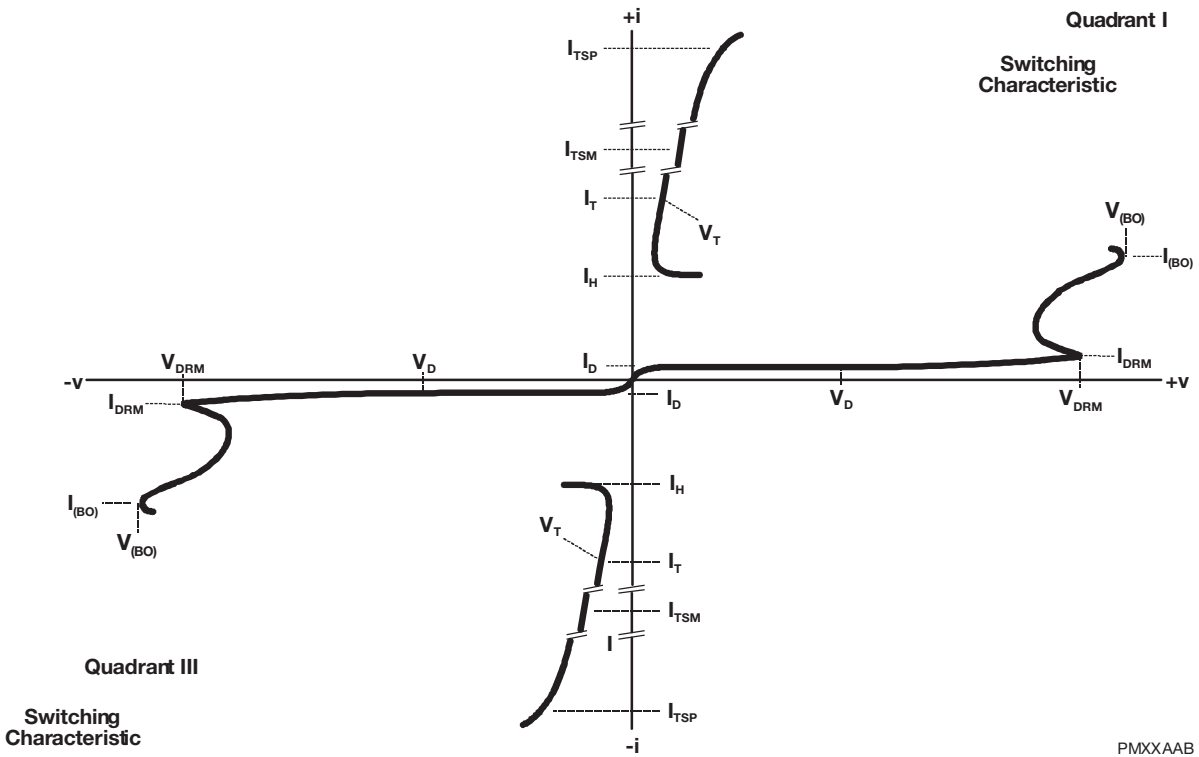


Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

PMXXAAB

TISP4xxxH3BJ Typical Characteristics

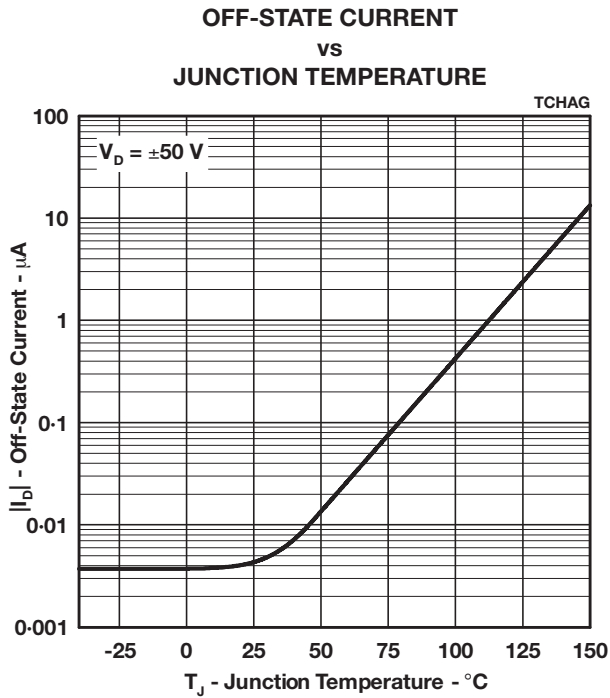


Figure 2.

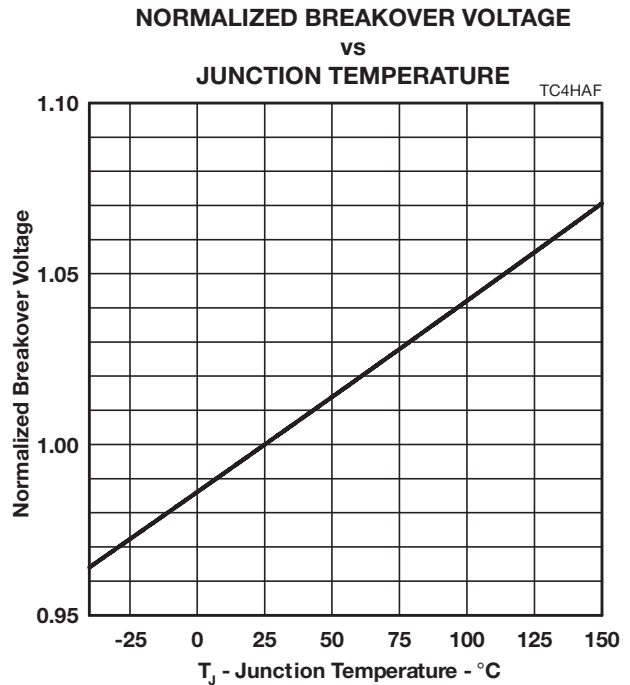


Figure 3.

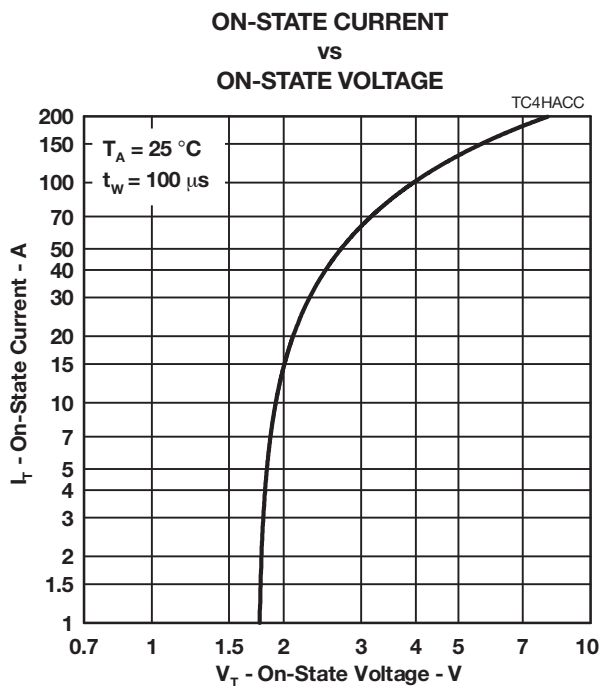


Figure 4.

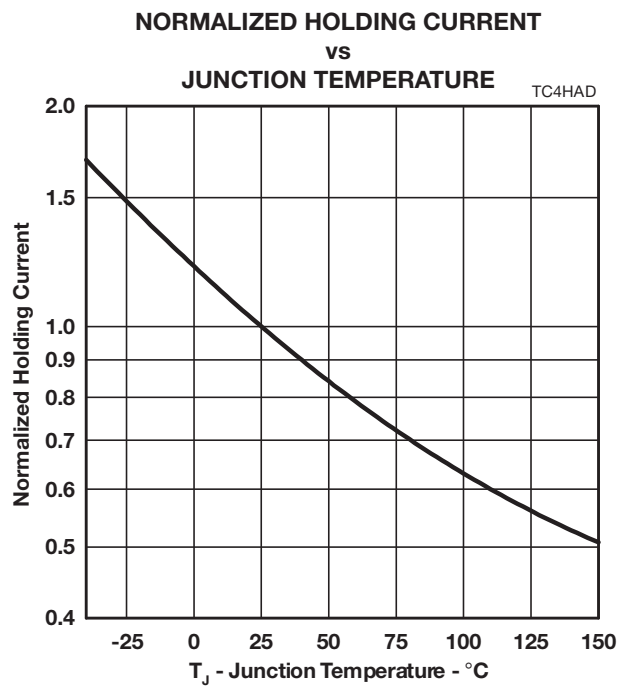


Figure 5.

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TISP4xxxM3BJ Typical Characteristics

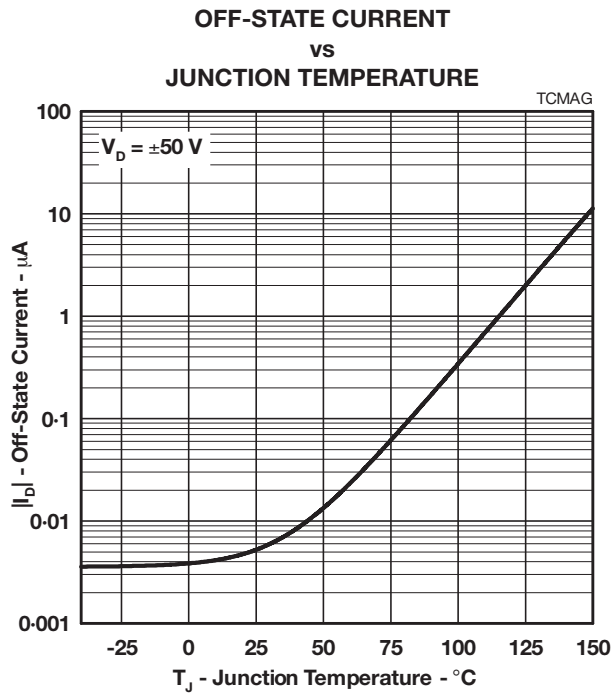


Figure 6.

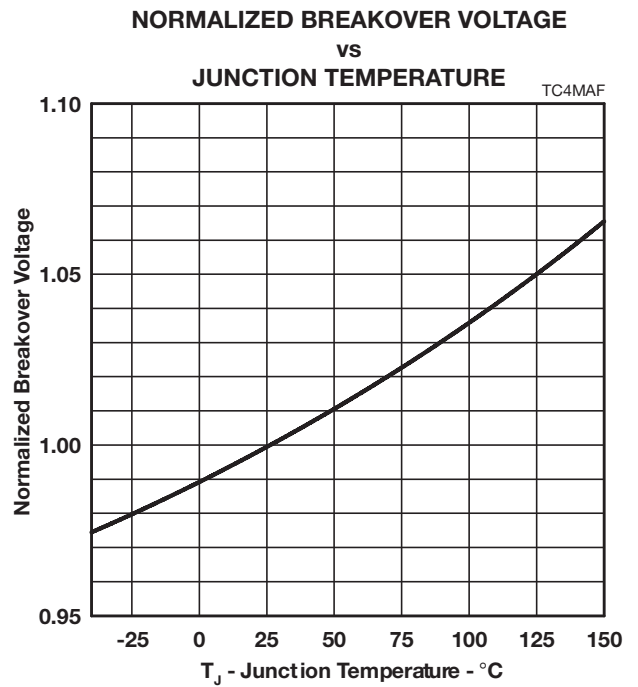


Figure 7.

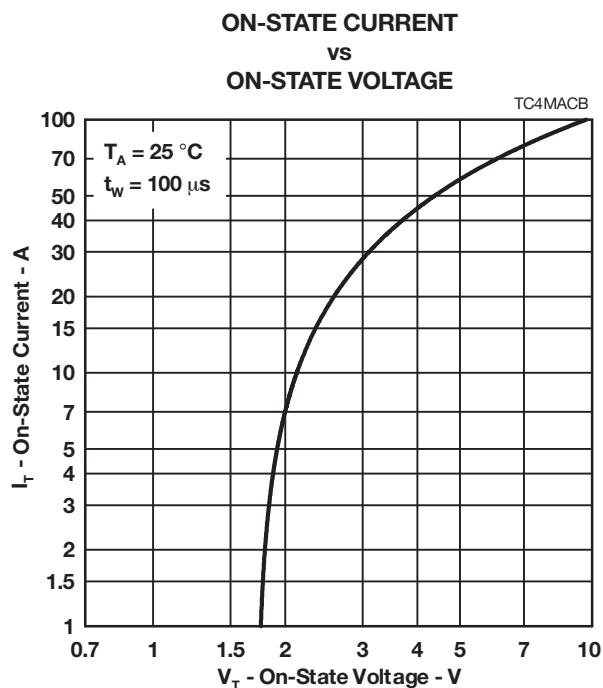


Figure 8.

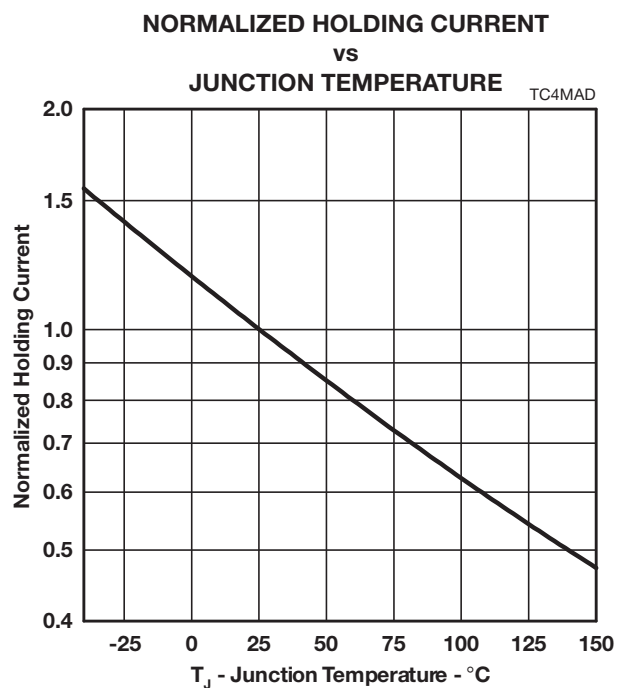


Figure 9.

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Rating Information

TISP4xxxH3BJ

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

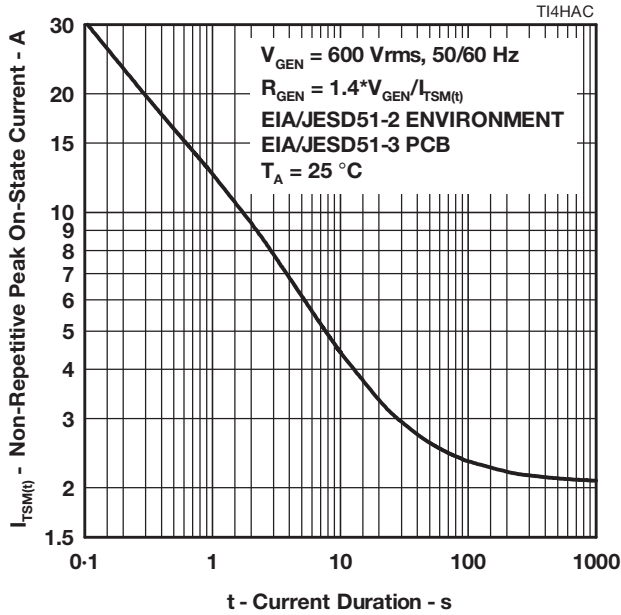


Figure 10.

TISP4xxxM3BJ

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

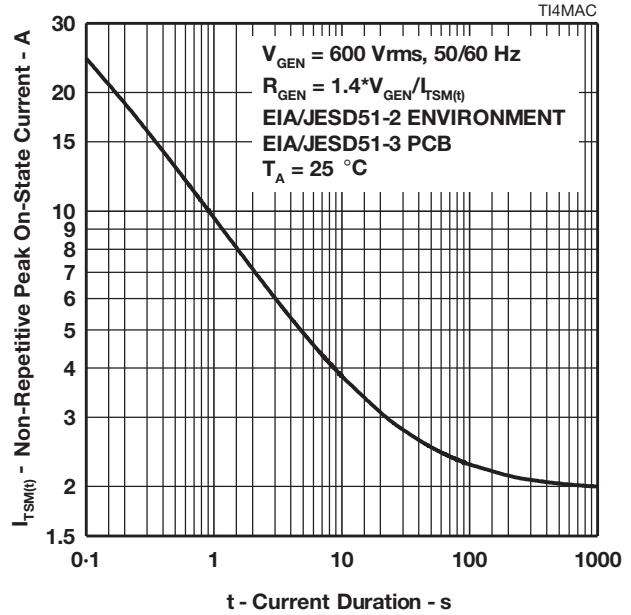


Figure 11.

APPLICATIONS INFORMATION

Introduction

These protector pairs have been designed to limit the peak voltages on the line terminals of '7581/7582/7583 LCAS (Line Card Access Switch) parts. An LCAS may also be referred to as a Solid-State Relay, SSR, i.e. a replacement of the conventional electro-mechanical relay.

The '7581 LCAS has two solid-state switches which connect the telephone line to the line card SLIC (Subscriber Line Interface Circuit), Figure 12, SW1 and SW2. A further two solid-state switches connect the telephone ringing generator to the line, Figure 12, SW3 and SW4. Applied 5-volt logic signals control the condition of the switches to perform the functions of line disconnect, connection to the SLIC and application of ringing. If excessive long-term overdissipation occurs, a thermal sensor activates thermal shutdown and opens the switches. The SLIC side of switches SW1 and SW2 is limited in voltage by internal protectors Th3 and Th4. The line-side of the LCAS is voltage limited by the two TISP® parts.

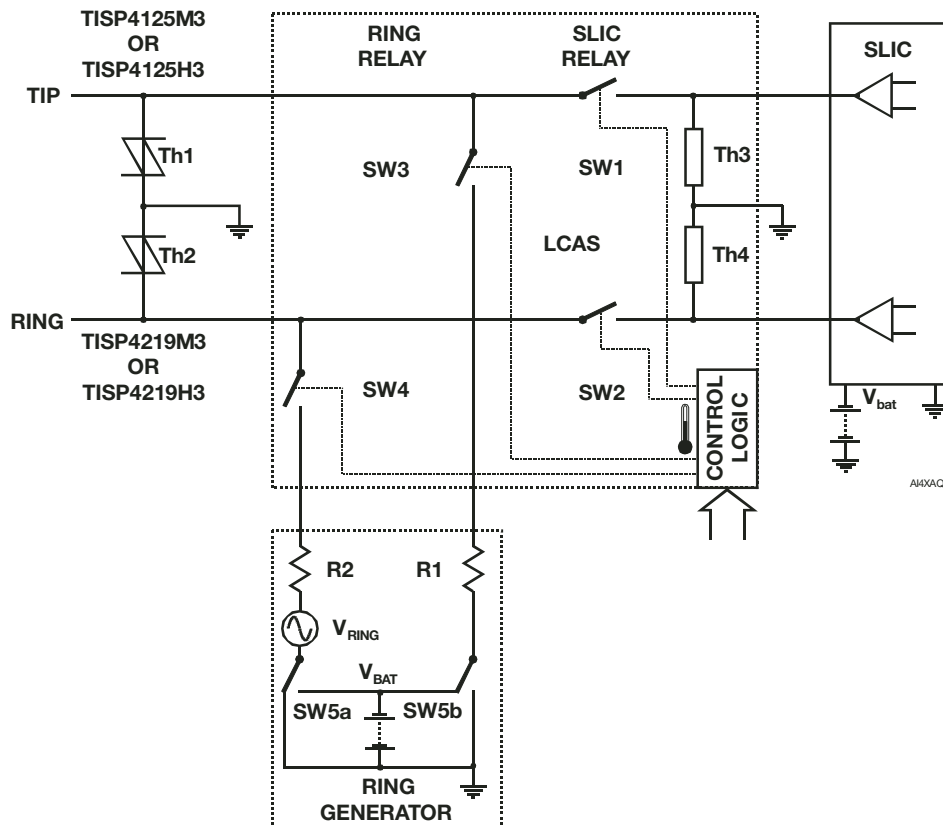


Figure 12. Basic LCAS Arrangement

Additional functions are provided by the '7582 (line test access) and the '7583 (test-in and test-out access). Up to three conventional electro-mechanical relays may be replaced by the LCAS. The resulting size reduction can double the line density of a line card.

This document covers the types of overvoltage protection required by the '7581 LCAS and how the TISP® part voltages are selected to provide these requirements. The LCAS '7582 and '7583 are also covered as the additional switches used in these parts are similar to the '7581.

LCAS Switch Ratings

When a switch is in the off state, the maximum withstand voltage may be set by the switch itself or by the control line to the switch. At 25°C, the switch terminal to ground voltage rating for all the switches is ± 320 V. Switches SW1 to SW3 are bidirectional MOS types and can withstand ± 320 V between terminals. Switch SW4 is a bidirectional thyristor which is rated at ± 465 V between terminals.

Overcurrents as well as overvoltages occur on telephone lines. In the on state, the thyristor switch, SW4, is capable of withstanding high levels of current overload. For currents above about 200 mA, the MOS switches, SW1 to SW3, will go into a current limited condition. This will cause the voltage to rise across the switch and large amounts of power to be developed. In the longer term, this power loss increases the overall chip temperature. When the temperature exceeds about 125 °C, thermal shutdown occurs and the switches are set to the off state. Without power loss, the LCAS will cool. Eventually, the thermal trip will reset, setting the switches back in the high power loss condition again. The cycle of temperature increase, thermal shutdown, temperature decrease and switch re-activation will continue until the overcurrent ceases.

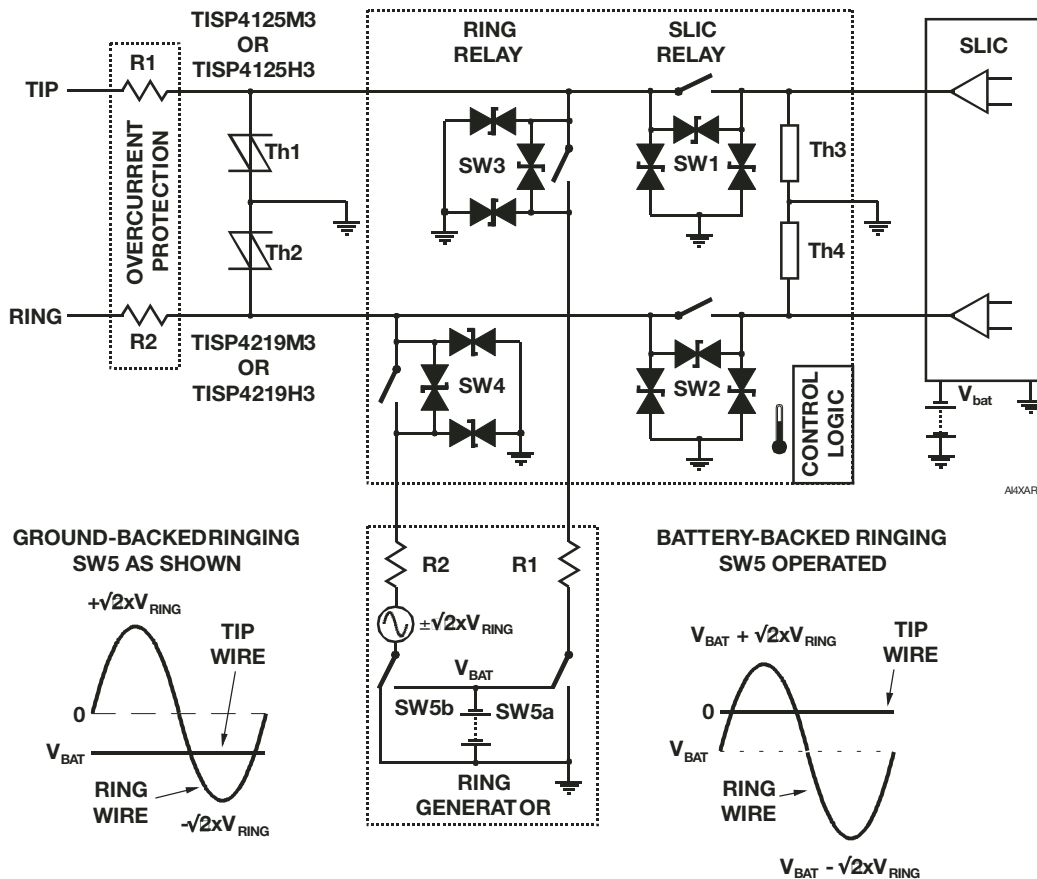


Figure 13. LCAS Shown with Switch Breakdown Limits

Equivalent Circuit

Figure 13 shows the LCAS switch voltage ratings as breakdown diodes, which must not be allowed to conduct. Each switch has three diodes; one between poles and the other two from each pole to ground. At 25 °C, switches SW1 through to SW3 have breakdown diode voltages of ± 320 V. Switch SW4 has breakdown diode voltage values of ± 465 V for the one between poles and ± 320 V for the two diodes connected to ground. Note that only protection to ground is required, as in the limit, the inter-switch voltage limitation of ± 640 V is the same as the switch to ground limitation of +320 V and -320 V in both polarities.

Protector Voltages

Protector working and protection voltage design calculations for the LCAS are described in the IEEE Std. C62.37.1-2000, *IEEE Guide for the Application of Thyristor Surge Protection Devices*, pp 40-43. These calculations comprehend:

- the temperature variation of LCAS voltage ratings,
- increase in protection voltage with ambient temperature rise, long term a.c. heating and under impulse conditions,
- decrease in working voltage with ambient temperature fall,
- ground-backed and battery-backed ringing configurations (see Figure 13).

These calculation techniques were used to set the TISP® part voltages. Using these TISP® parts allows normal system voltage levels of ± 100 V on TIP and ± 180 V on RING without clipping at 25 °C. At 0 °C ambient, these voltage levels become ± 97 V on TIP and ± 174 V on RING. Under open circuit line conditions, this means that the peak ringing voltage cannot exceed ± 174 V for equipment operation down to 0 °C ambient.

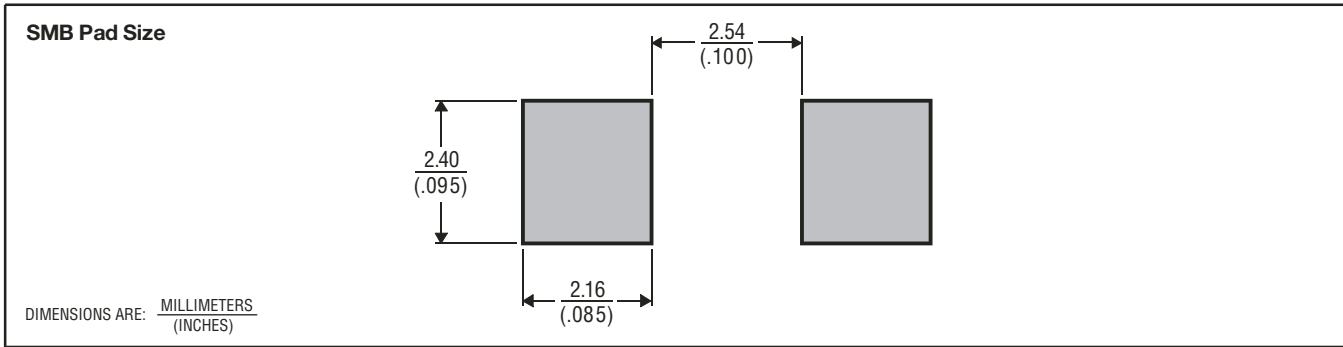
Assuming a battery voltage of 48 V ± 2.5 V and battery-backed ringing, the maximum peak a.c. ring voltage is $174 \text{ V} - 50.5 \text{ V} = 123.5 \text{ V}$ or 87 V rms. The working voltage of ± 97 V on TIP is more than half the ± 174 V working voltage on RING. As a result, the TIP working voltage does not represent a limitation for systems where the TIP return resistance is equal or less than the RING source resistance.

For balanced impedance ground-backed ringing, the maximum peak a.c. ring voltage under short line conditions (short between TIP and RING) is limited by the TIP working voltage of ± 97 V. In the negative ring polarity, the limit of the voltage is made up from half the battery voltage plus half of the peak a.c. ring voltage. The maximum peak a.c. ring voltage is $2 \times (97 - 50.5/2) = 143.5 \text{ V}$ or 101 V rms.

Line test voltage levels must be considered, whether they be applied by using LCAS switches or separate electro-mechanical relays. For these TISP® parts, the applied test voltage should not exceed the lowest working voltage, which is ± 97 V.

MECHANICAL DATA

Recommended Printed Wiring Footprint



MDXX BIA

Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code
TISP4125H3BJ	4125H3
TISP4219H3BJ	4219H3
TISP4125M3BJ	4125M3
TISP4219M3BJ	4219M3

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