

3-W High-Voltage Switchmode Regulator

DESCRIPTION

The Si9102 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10 to 120 V unregulated dc power source.

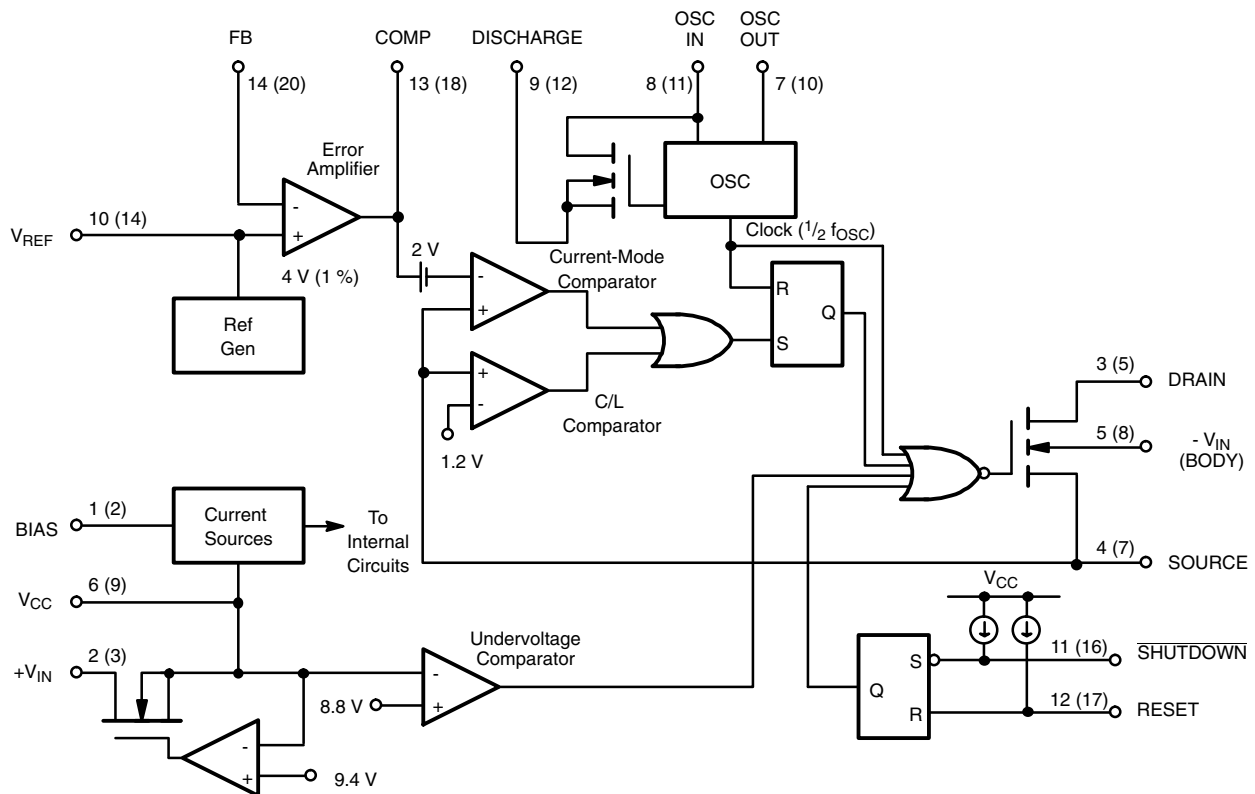
This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9102 is available in both standard and lead (Pb)-free 14-pin plastic DIP and 20-pin PLCC packages which are specified to operate over the industrial temperature range of -40 °C to 85 °C.

FEATURES

- 10 to 120 V Input Range
- Current-Mode Control
- On-chip 200 V, 7 Ω MOSFET Switch
- SHUTDOWN and RESET
- High Efficiency Operation (> 80 %)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

FUNCTIONAL BLOCK DIAGRAM



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Si9102



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| ABSOLUTE MAXIMUM RATINGS | | | |
|--|--|-----------------------------|------|
| Parameter | | Limit | Unit |
| Voltages Referenced to - V_{IN} ($V_{CC} < +V_{IN} + 0.3 V$) | | | |
| V_{CC} | | 15 | V |
| $+V_{IN}$ | | 120 | |
| V_{DS} | | 200 | |
| I_D (Peak) (Note: 300 μs pulse, 2 % duty cycle) | | 2 | A |
| I_D (rms) | | 250 | mA |
| Logic Inputs (RESET, SHUTDOWN, OSC IN) | | - 0.3 V to $V_{CC} + 0.3 V$ | V |
| Linear Inputs (FEEDBACK, SOURCE) | | - 0.3 to 7 | |
| HV Pre-Regulator Input Current (continuous) | | 3 | mA |
| Storage Temperature | | - 65 to 125 | °C |
| Operating Temperature | | - 40 to 85 | |
| Junction Temperature (T_J) | | 150 | |
| Power Dissipation (Package) ^a | 14-Pin Plastic DIP (J Suffix) ^b | 750 | mW |
| | 20-Pin PLCC (N Suffix) ^c | 1400 | |
| Thermal Impedance (Θ_{JA}) | 14-Pin Plastic DIP | 167 | °C/W |
| | 20-Pin PLCC | 90 | |

Notes:

- a. Device Mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25 °C.
c. Derate 11.2 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

| RECOMMENDED OPERATING RANGE | | | |
|-----------------------------------|--|-------------------------------|------|
| Parameter | | Limit | Unit |
| Voltages Referenced to - V_{IN} | | | |
| V_{CC} | | 9.5 to 13.5 | V |
| R_{OSC} | | 25 k Ω to 1 M Ω | |
| Linear Inputs | | 0 to 7 | V |
| $+V_{IN}$ | | 10 to 120 | V |
| f_{OSC} | | 40 kHz to 1 MHz | |
| Digital Inputs | | 0 to V_{CC} | |

| SPECIFICATIONS ^a | | | | | | | |
|--------------------------------------|--------------|---|-------------------|----------------------------------|------------------|------------------|------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified DISCHARGE = - $V_{IN} = 0 V$ $V_{CC} = 10 V, +V_{IN} = 48 V$ $R_{BIAS} = 390 k\Omega, R_{OSC} = 330 k\Omega$ | Temp ^b | Limits D Suffix - 40 to 85 °C | | | Unit |
| | | | | Min ^d | Typ ^c | Max ^d | |
| Reference | | | | | | | |
| Output Voltage | V_R | OSC IN = - V_{IN} (OSC Disabled) $R_L = 10 M\Omega$ | Room Full | 3.92 3.86 | 4.0 | 4.08 4.14 | V |
| Output Impedance ^e | Z_{OUT} | | Room | 15 | 30 | 45 | k Ω |
| Short Circuit Current | I_{SREF} | $V_{REF} = -V_{IN}$ | Room | 70 | 100 | 130 | μA |
| Temperature Stability ^e | T_{REF} | | Full | | 0.5 | 1.0 | mV/°C |
| Oscillator | | | | | | | |
| Maximum Frequency ^e | f_{MAX} | $R_{OSC} = 0$ | Room | 1 | 3 | | MHz |
| Initial Accuracy | f_{OSC} | $R_{OSC} = 330 k\Omega^g$ | Room | 80 | 100 | 120 | kHz |
| | | $R_{OSC} = 150 k\Omega^g$ | Room | 160 | 200 | 240 | |
| Voltage Stability | $\Delta f/f$ | $\Delta f/f = f(13.5 V) - f(9.5 V)/f(9.5 V)$ | Room | | 10 | 15 | % |
| Temperature Coefficient ^e | T_{OSC} | | Full | | 200 | 500 | ppm/°C |



| SPECIFICATIONS ^a | | | | | | | |
|---|----------------------|--|-------------------|----------------------------------|------------------|------------------|----------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified DISCHARGE = - V _{IN} = 0 V V _{CC} = 10 V, + V _{IN} = 48 V R _{BIAS} = 390 k Ω , R _{OSC} = 330 k Ω | Temp ^b | Limits D Suffix - 40 to 85 °C | | | Unit |
| | | | | Min ^d | Typ ^c | Max ^d | |
| Error Amplifier | | | | | | | |
| Feedback Input Voltage | V _{FB} | FB Tied to COMP OSC IN = - V _{IN} (OSC Disabled) | Room | 3.96 | 4.00 | 4.04 | V |
| Input BIAS Current | I _{FB} | OSC IN = - V _{IN} , V _{FB} = 4 V, OSC IN = - V _{IN} (OSC Disabled) | Room | | 25 | 500 | nA |
| Open Loop Voltage Gain ^e | A _{VOL} | | Room | 60 | 80 | | dB |
| Unity Gain Bandwidth ^e | BW | | Room | 0.7 | 1 | | MHz |
| Dynamic Output Impedance ^e | Z _{OUT} | | Room | | 1000 | 2000 | Ω |
| Output Current | I _{OUT} | Source (V _{FB} = 3.4 V) | Room | | - 2.0 | - 1.4 | mA |
| Input OFFSET Voltage | V _{OS} | OSC IN = - V _{IN} (OSC Disabled) | Room | | \pm 15 | \pm 40 | mV |
| Output Current | I _{OUT} | Sink (V _{FB} = 4.5 V) | Room | 0.12 | 0.15 | | mA |
| Power Supply Rejection | PSRR | 9.5 V \leq V _{CC} \leq 13.5 V | Room | 50 | 70 | | dB |
| Current Limit | | | | | | | |
| Threshold Voltage | V _{SOURCE} | R _L = 100 Ω from DRAIN to V _{CC} V _{FB} = 0 V | Room | 1.0 | 1.2 | 1.4 | V |
| Delay to Output ^e | t _d | R _L = 100 Ω from DRAIN to V _{CC} V _{SOURCE} = 1.5 V, See Figure 1 | Room | | 100 | 200 | ns |
| Pre-Regulator/Start-Up | | | | | | | |
| Input Voltage | + V _{IN} | I _{IN} = 10 μ A | Room | | | 120 | V |
| Input Leakage Current | + I _{IN} | V _{CC} \geq 10 V | Room | | | 10 | μ A |
| Pre-Regulator Start-Up Current | I _{START} | Pulse Width \leq 300 μ s, V _{CC} = 7 V | Room | 8 | 15 | | mA |
| V _{CC} Pre-Regulator Turn-Off Threshold Voltage | V _{REG} | I _{PRE-REGULATOR} = 10 μ A | Room | 7.8 | 9.4 | 9.7 | V |
| Undervoltage Lockout | V _{UVLO} | R _L = 100 Ω from DRAIN to V _{CC} See Detailed Description | Room | 7.0 | 8.8 | 9.2 | |
| V _{REG} , - V _{UVLO} | V _{DELTA} | | Room | 0.3 | 0.6 | | |
| Supply | | | | | | | |
| Supply Current | I _{CC} | | Room | 0.45 | 0.6 | 1.0 | mA |
| Bias Current | I _{BIAS} | | Room | 10 | 15 | 20 | μ A |
| Logic | | | | | | | |
| SHUTDOWN Delay ^e | t _{SD} | V _{SOURCE} = - V _{IN} , See Figure 2 | Room | | 50 | 100 | ns |
| SHUTDOWN Pulse Width ^e | t _{SW} | See Figure 3 | Room | 50 | | | |
| RESET Pulse Width ^e | t _{RW} | | Room | 50 | | | |
| Latching Pulse Width ^e SHUTDOWN and RESET Low | t _{LW} | | Room | 25 | | | |
| Input Low Voltage | V _{IL} | | Room | | | 2.0 | V |
| Input High Voltage | V _{IH} | | Room | 8.0 | | | |
| Input Current Input Voltage High | I _{IH} | V _{IN} = 10 V | Room | | 1 | 5 | μ A |
| Input Current Input Voltage Low | I _{IL} | V _{IN} = 0 V | Room | - 35 | - 25 | | |
| MOSFET Switch | | | | | | | |
| Breakdown Voltage | V _{BR(DSS)} | I _{DRAIN} = 100 μ A | Full | 200 | 220 | | V |
| Drain-Source On Resistance ^f | r _{DS(on)} | I _{DRAIN} = 100 mA | Room | | | 7 | Ω |
| Drain Off Leakage Current | I _{DSS} | V _{DRAIN} = 100 V | Room | | 5 | 10 | μ A |
| Drain Capacitance | C _{DS} | | Room | | 35 | | pF |

Notes:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Temperature coefficient of r_{DS(on)} is 0.75 % per °C, typical.
- C_{STRAY} Pin 8 = \leq 5 pF.



TIMING WAVEFORMS

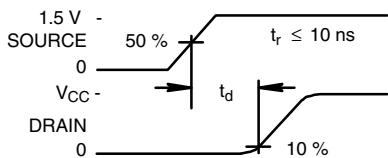


Figure 1.

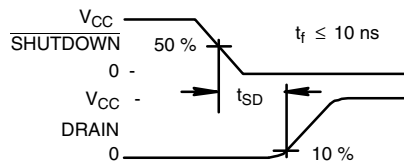


Figure 2.

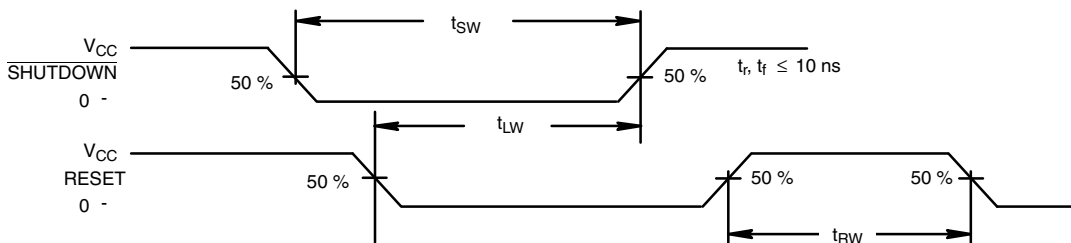


Figure 3.

TYPICAL CHARACTERISTICS

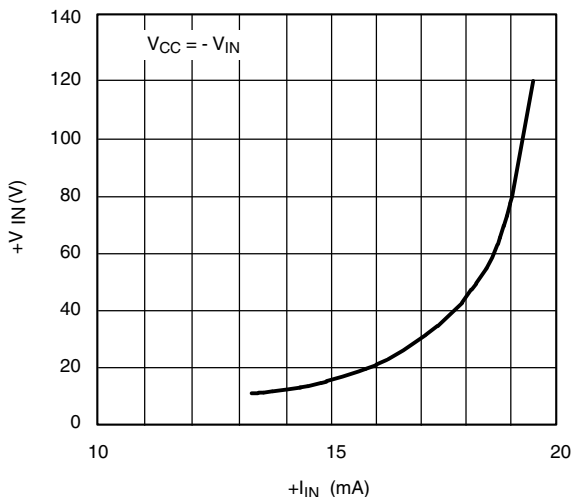


Figure 4. +VIN vs. +IIN at Start-Up

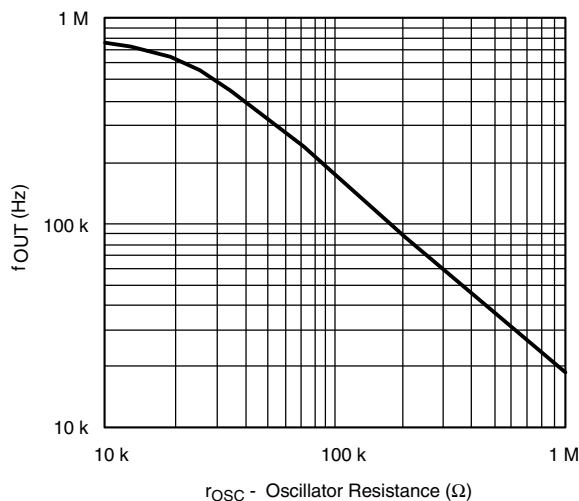
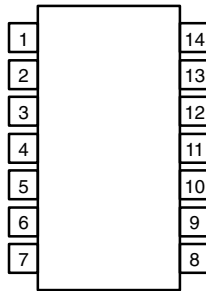


Figure 5. Output Switching Frequency vs. Oscillator Resistance

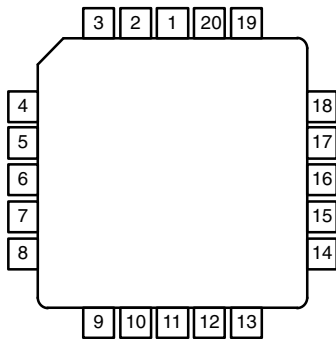
PIN CONFIGURATIONS

PDIP-14



Top View

PLCC-20



Top View

PIN DESCRIPTION

| Function | Pin | |
|-------------------|------------|--------------|
| | 14-Pin DIP | 20-Pin PLCC* |
| BIAS | 1 | 2 |
| + V _{IN} | 2 | 3 |
| DRAIN | 3 | 5 |
| SOURCE | 4 | 7 |
| - V _{IN} | 5 | 8 |
| V _{CC} | 6 | 9 |
| OSC OUT | 7 | 10 |
| OSC IN | 8 | 11 |
| DISCHARGE | 9 | 12 |
| V _{REF} | 10 | 14 |
| SHUTDOWN | 11 | 16 |
| RESET | 12 | 17 |
| COMP | 13 | 18 |
| FB | 14 | 20 |

*Pins 1, 4, 6, 13, 15, and 19 = N/C

ORDERING INFORMATION

| Standard Part Number | Lead (Pb)-free Part Number | Temperature Range | Package |
|---------------------------------------|--|-------------------|---------|
| Si9102DJ02 | Si9102DJ02-E3 | - 40 to 85 °C | PDIP-14 |
| Si9102DN02 | Si9102DN02-E3 | | PLCC-20 |
| Si9102DN02-T1 (With Tape and Reel) | Si9102DN02-T1-E3 (With Tape and Reel) | | |

DETAIL DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, + V_{IN} will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between + V_{IN} and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4 V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

Si9102



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DETAIL DESCRIPTION

BIAS

To properly set the bias for the Si9102, a 390 k Ω resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA .

Reference Section

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within $\pm 1\%$ of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC in and OSC out pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq 50\%$ by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 k Ω to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

| $\overline{\text{SHUTDOWN}}$ | RESET | Output |
|------------------------------|-----------------------|------------------------------|
| H | H | Normal Operation |
| H | $\overline{\text{L}}$ | Normal Operation (No Change) |
| L | H | Off (Not Latched) |
| L | L | Off (Latched) |
| $\overline{\text{L}}$ | L | Off (Latched, No Change) |

Output Switch

The output switch is a 7 Ω , 200 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.



APPLICATIONS

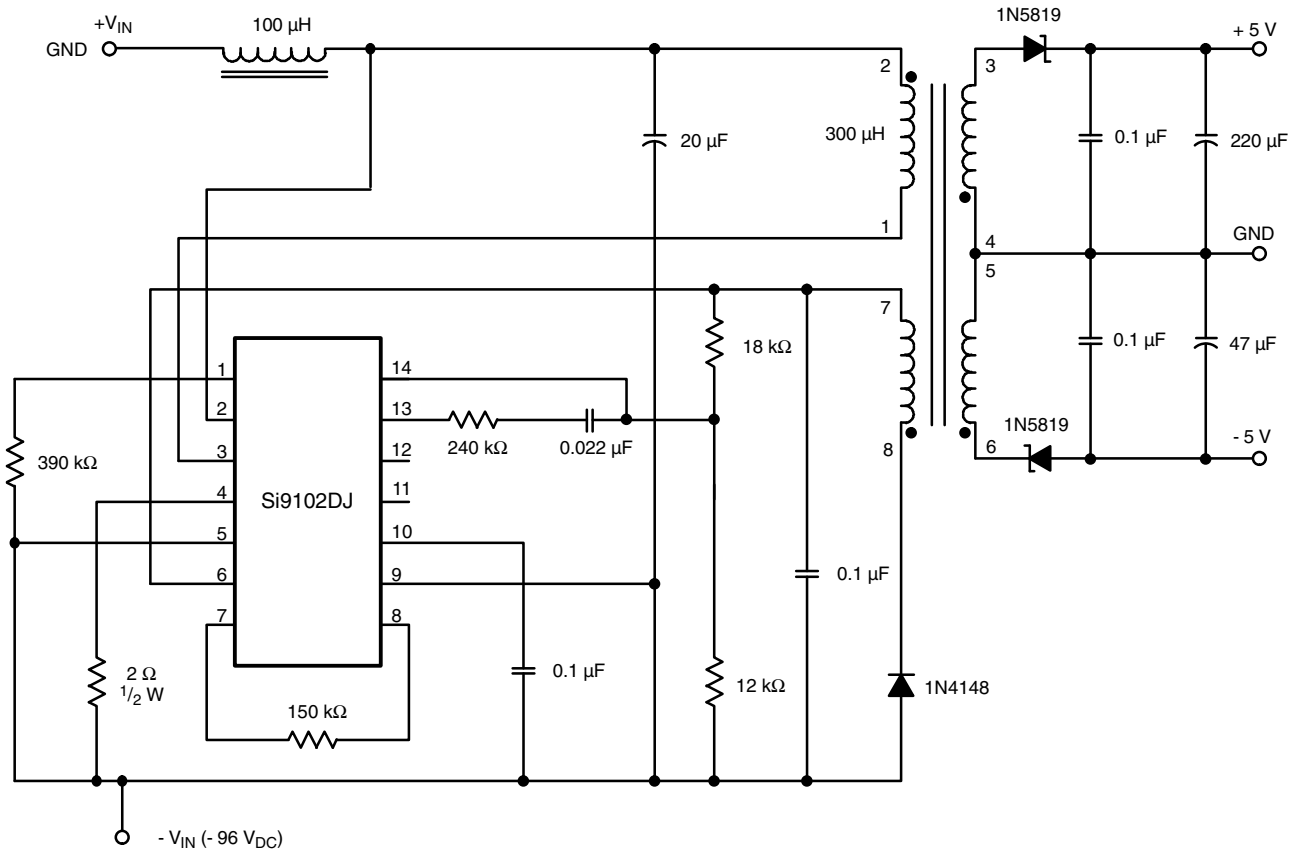
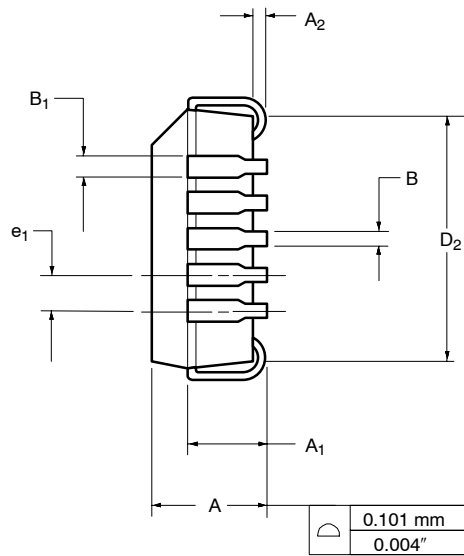
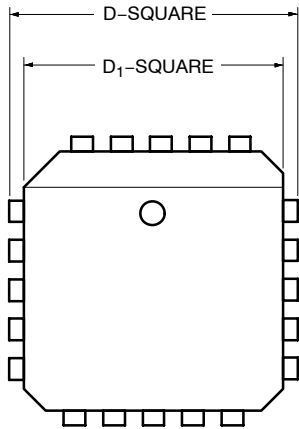


Figure 6. Flyback Converter for Double Battery Telecommunications Power Supplies

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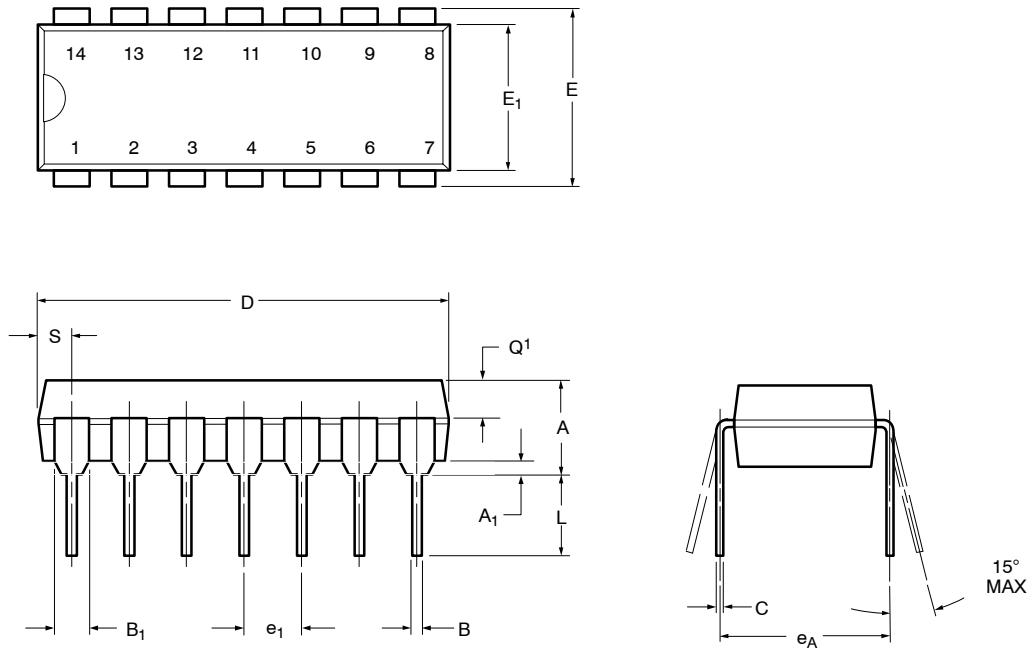
PLCC: 20-LEAD (POWER IC ONLY)



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 4.20 | 4.57 | 0.165 | 0.180 |
| A₁ | 2.29 | 3.04 | 0.090 | 0.120 |
| A₂ | 0.51 | - | 0.020 | - |
| B | 0.331 | 0.553 | 0.013 | 0.021 |
| B₁ | 0.661 | 0.812 | 0.026 | 0.032 |
| D | 9.78 | 10.03 | 0.385 | 0.395 |
| D₁ | 8.890 | 9.042 | 0.350 | 0.356 |
| D₂ | 7.37 | 8.38 | 0.290 | 0.330 |
| e₁ | 1.27 BSC | | 0.050 BSC | |

ECN: S-40081—Rev. A, 02-Feb-04
DWG: 5917

PDIP: 14-LEAD (POWER IC ONLY)



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 17.27 | 19.30 | 0.680 | 0.760 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 1.02 | 2.03 | 0.040 | 0.080 |

ECN: S-40081—Rev. A, 02-Feb-04
DWG: 5919



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