SiT6712EB Evaluation Board User Manual

Contents

1 Introduction

The SiT6712EB evaluation board (EVB) is designed for use with SiTime's In-system programmable oscillators (ISP-DCXO) that support the differential signaling outputs in the 5.0x3.2 mm 10-pin QFN package. It enables the user to evaluate all aspects of the ISP-DCXO devices including signal integrity, phase noise, phase jitter and the re-programming of the output frequency via I^2C/SPI interfaces.

EVB Features

- Support for SiT3521 (1 to 340 MHz) and SiT3522 (340.000001 to 725 MHz) ISP-DCXOs
- Probing points for output frequency measurements
  - Support for LVPECL, LVDS and HCSL output signal types
  - Support for waveform measurements
  - Support for phase noise and phase jitter measurements
- Connector access to I^2C and/or SPI interfaces
- Connector access for current consumption measurements

SiTime typically ships the EVB pre-configured with the ISP-DCXO device specified by the user. The end user can re-configure the EVB for an ISP-DCXO device of a different configuration.

Refer to Section **3** for details on EVB configuration and usage.

2 I/O Descriptions

Table 1 describes the input/output connectors of the board.

Table 1: SiT6712EB I/O

Designator	I/O	Description
P1	**Power**	A three-pin connector (P1) for DC power supply to the ISP-DCXO device. Pin's polarity is identified on the silkscreen pattern near the connector (see Figure A2). Third pin is used for VDD sensing.
P5	**VBIAS**	A three-pin connector (P5) intended for supplying bias voltage or supplying negative voltage to the ISP-DCXO device ground pin for split ground configuration. See Section 3.1 for detailed information on different termination schemes. Third pin is intended for Vbias sensing.
P1	**PIN 1**	A three-pin header (P2) provides access to pin 1 of the ISP-DCXO device
P3	**PIN 2**	A three-pin header (P3) provides access to pin 2 of the ISP-DCXO device
J1/J2	**OUT+ and OUT-**	OUT+ and OUT- are connected to the frequency output of the ISP-DCXO device. The output should be measured using either the hi-impedance, hi-bandwidth active probe or via the SMA connectors (J1 and J2). Section 3.1 describes in detail the recommended measurement configurations.
P4	**Current Measurement**	A two-pin connector (P4) enables the current consumption measurement of the ISP-DCXO device. To measure the current, remove zero-ohm resistors R1 and R19, and connect the DMM or other current measuring device across this connector. It is recommended to measure the voltage on VDD pin and adjust for any drop on the DMM to ensure known VDD voltage on the device.
P6	**Frequency control via I^2C/SPI**	A five-pin header (P6) provides access to I^2C (SDA, SCL) or SPI (MOSI, MISO, SCL) of the ISP-DCXO device.

Note: Pin 1 location of the ISP-DCXO device on EVB is indicated by a chamfer in the silkscreen pattern around the device footprint.

3 EVB Usage Descriptions

3.1 EVB Configurations

The SiT6712EB supports multiple configurations for different signaling types of SiTime differential oscillators by using different component loading options.

Refer to

- Figure A1 in Appendix A for the SiT6712EB schematics
- Figure A2 in Appendix A for the SiT6712EB layout top view

Note that not all components shown in the schematics are populated for all configurations of the EVB. Specifically,

- Any components with assigned nominal values are used in all configurations of the EVB
- Any components without assigned nominal values are populated only for specific configuration of EVB where these parts are needed
- Any components labeled “DNP” are not populated on the EVB and are reserved for SiTime internal use only

3.1.1 LVPECL, Standard Termination, Active Probe

In this configuration, the LVPECL outputs are terminated to Vbias = VDD – 2 V with 50 Ω resistors (R11 and R24). A high-speed active probe, as shown on Figure 1, is placed on the termination resistor’s pads which are on the OUT+ and OUT- traces. Figure 1 shows the termination scheme for this configuration.

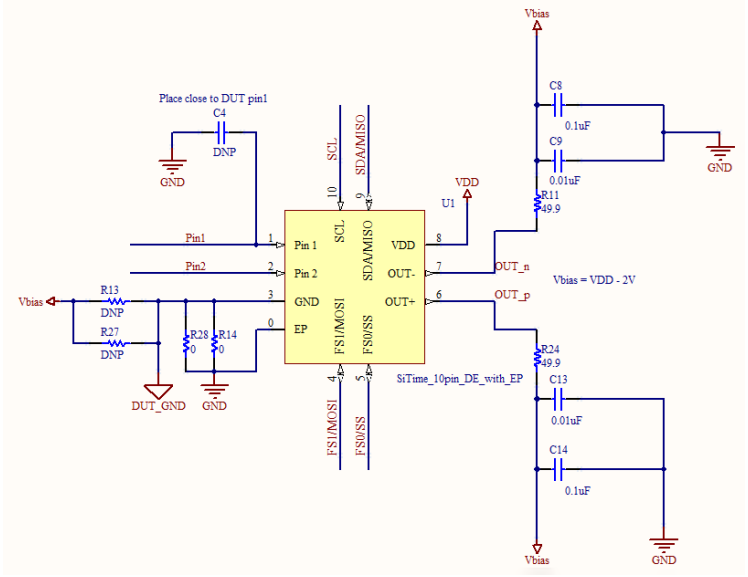

Figure 1: LVPECL output termination with 50 Ω to Vbias and measurement using high impedance and high bandwidth active probe

3.1.2 LVPECL, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVPECL devices.

This configuration allows LVPECL output connection to the measurement instrument using 50 Ω coaxial cables. Outputs are terminated with 150 Ω/120 Ω (R15 and R22; for 3.3 V and 2.5 V VDD respectively) to GND on the DUT side and connected to SMA connectors through 0.1 uF series capacitors (R16 and R23). Figure 2 shows the termination scheme for this configuration.

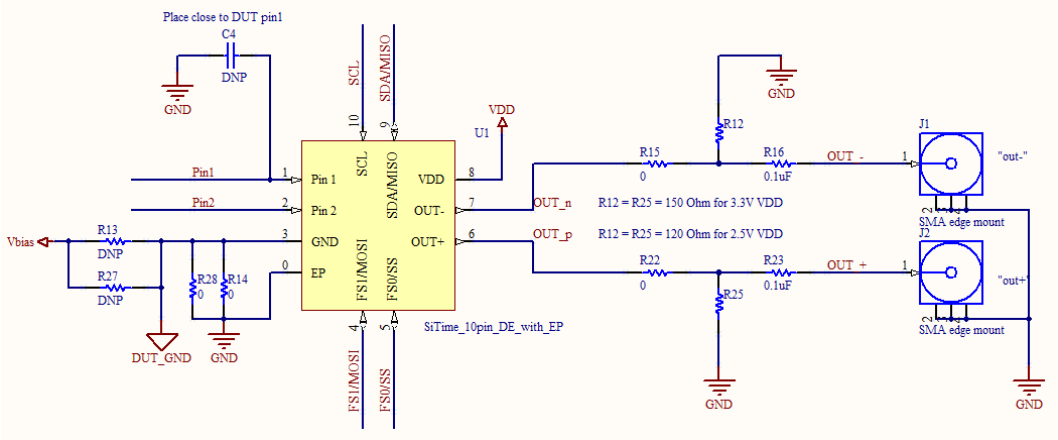

Figure 2: LVPECL output termination with 150 Ω/120 Ω to GND and measurement with AC-coupled connection to measurement instrument using 50 Ω SMA cables

3.1.3 LVPECL, Y-Termination, Active Probe

This configuration is intended for LVPECL output waveform parameters measurement using active probe.

Figure 3 shows termination scheme for this configuration. R26 is added to create DC voltage bias for OUT+ and OUT- with R24 (50 Ω) and R11 (50 Ω). R26 is 50 Ω for 3.3 V VDD and 18 Ω for 2.5 V VDD.

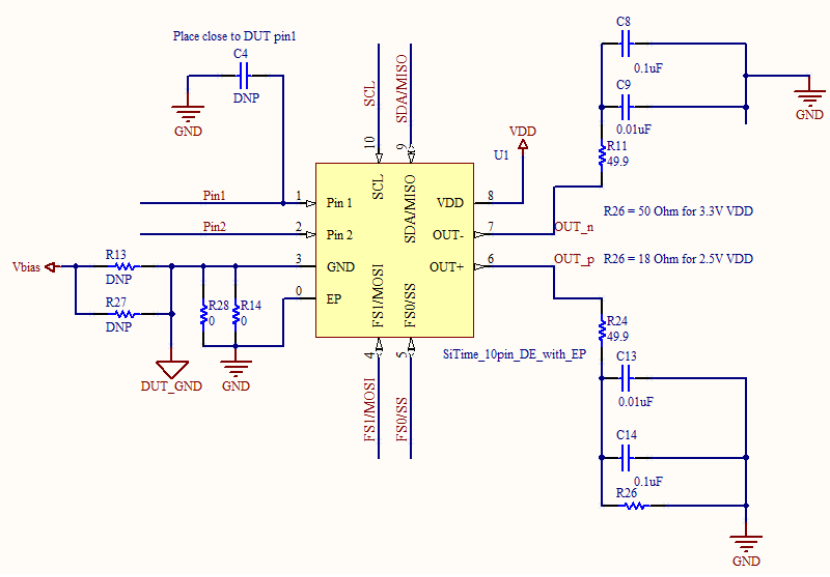

Figure 3: Y-termination scheme for LVPECL output termination for measurement using high impedance and high bandwidth active probe

3.1.4 LVDS, Standard Termination, Active Probe

This configuration is intended for LVDS output waveform parameters measurement using active probe. A high-speed active probe, as shown on Figure 4 is placed on the termination resistor's pads which are on the OUT+ and OUT- traces.

Figure 4 shows differential impedance of 100 Ω (R21) across OUT+ and OUT- for termination.

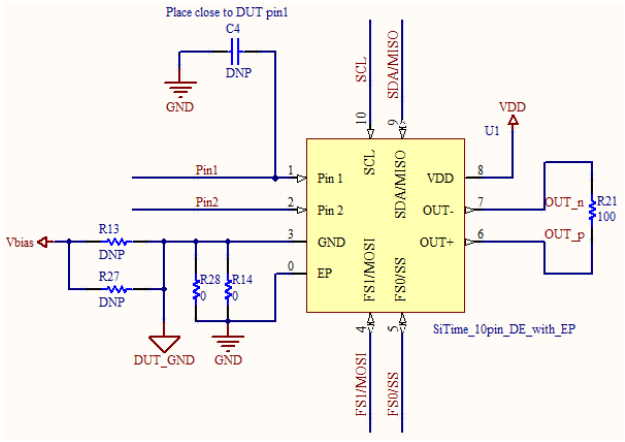

Figure 4: 100 Ω differential impedance across LVDS outputs for measurement using high impedance and high bandwidth active probe

3.1.5 LVDS, AC-coupling Configuration, Direct to Instrument

This is default shipment configuration for evaluation boards with LVDS devices.

This configuration is useful for connecting LVDS outputs to 50 Ω input channels of the measurement instrument. The AC-coupling capacitors (R16 and R23) block the DC common mode voltage from the LVDS outputs to avoid DC current draw to the 50 Ω inputs. Figure 5 shows termination scheme for this configuration.

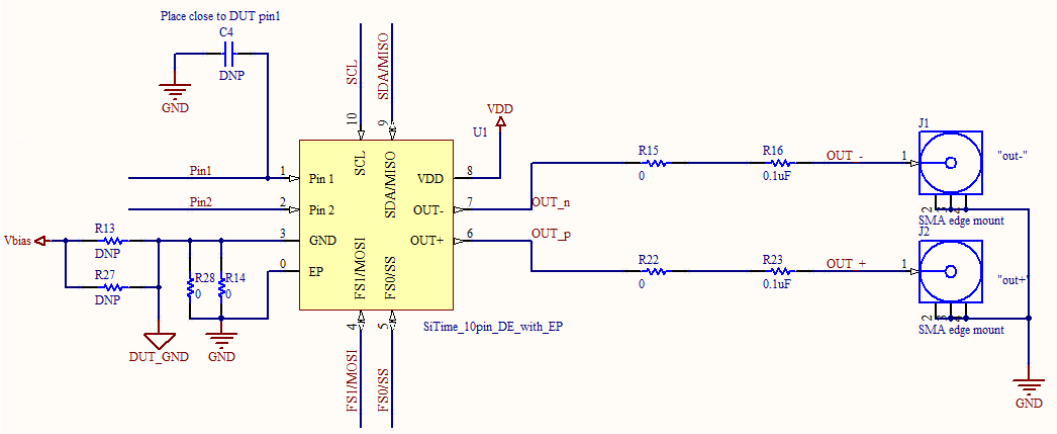

Figure 5: AC-coupled LVDS outputs are terminated by measurement instrument input 50 Ω impedance, equivalent 100 Ω across OUT+ and OUT-

3.1.6 HCSL, Standard Termination, Active Probe

This configuration is intended for HCSL output waveform parameters measurement using active probe. Output is terminated with 50 Ω (R12 and R25) to GND. Series resistors R15 and R22 are used as overshoot limiter and should be in range from 10 Ω to 30 Ω. A high speed active probe is placed on the termination resistor's pads which are on the OUT+ and OUT- traces. Figure 6 shows termination scheme for this configuration.

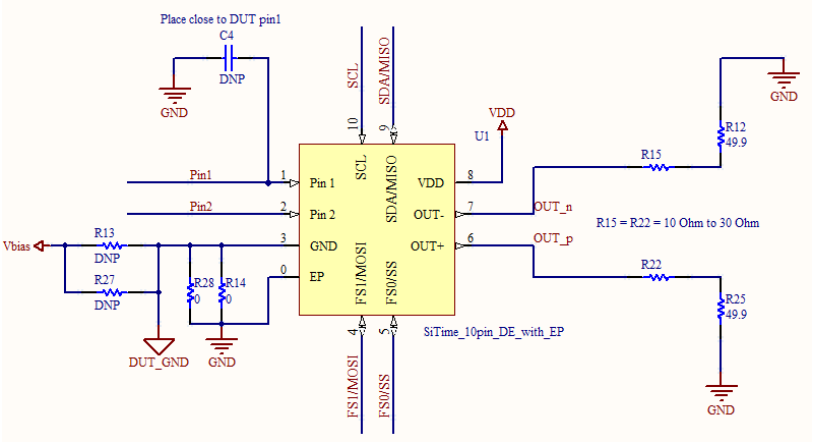

Figure 6: HCSL outputs terminated with 50 Ω to GND through 10 Ω to 30 Ω series resistors for measurement using high impedance and high bandwidth active probe

3.1.7 HCSL, Standard Termination, Direct to Instrument

This is default shipment configuration for evaluation boards with HCSL devices.

This configuration is intended for HCSL output waveform parameters measurement with direct connection to measurement instrument 50 Ω inputs.

Figure 7 shows termination scheme for this configuration. Series resistors R15 and R22 are used as overshoot limiter and should be in range of 10 Ω to 30 Ω.

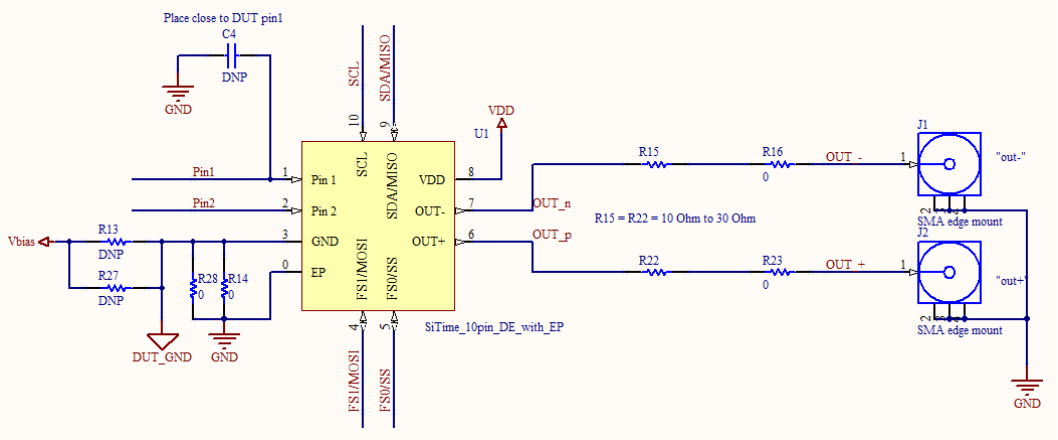

Figure 7: HCSL outputs terminated with 50 Ω to GND at measurement instrument side with 10 Ω to 30 Ω series resistors at source side

3.2 I²C and SPI Interfaces

Both I²C and SPI interfaces are supported via the P6 5-pin connector. Two pull up resistors – R20 (4.7 kΩ) and R30 (4.7 kΩ) – must be populated for the I²C support. SPI interface doesn't require these two resistors. The EVB ships preconfigured for either the I²C or the SPI support per user specification.

3.3 Waveform Measurement Using Active Probe

SiTime differential oscillators are high speed logic output devices with fast, sub-nanosecond rise/fall time. It is critical that the proper logic and high frequency measurement techniques are used along with the high-quality active probe to ensure best measurement results.

SiTime recommends the following equipment for proper measurement of a differential clock waveform:

1) Differential active probe with >4GHz bandwidth, <1pF load capacitance, such as an Agilent 1134A, with high-speed differential probe heads, such as:
    a. Agilent E2675B differential browser
    b. Agilent N5381B solder-down probe tip
    c. Agilent N5425B/N5426A ZIF probe tip
2) Oscilloscope with 4 GHz bandwidth or higher
3) Oscilloscope with 50 Ω inputs.

Please refer to Figure 8 for a probing example on the EVB using active probe.

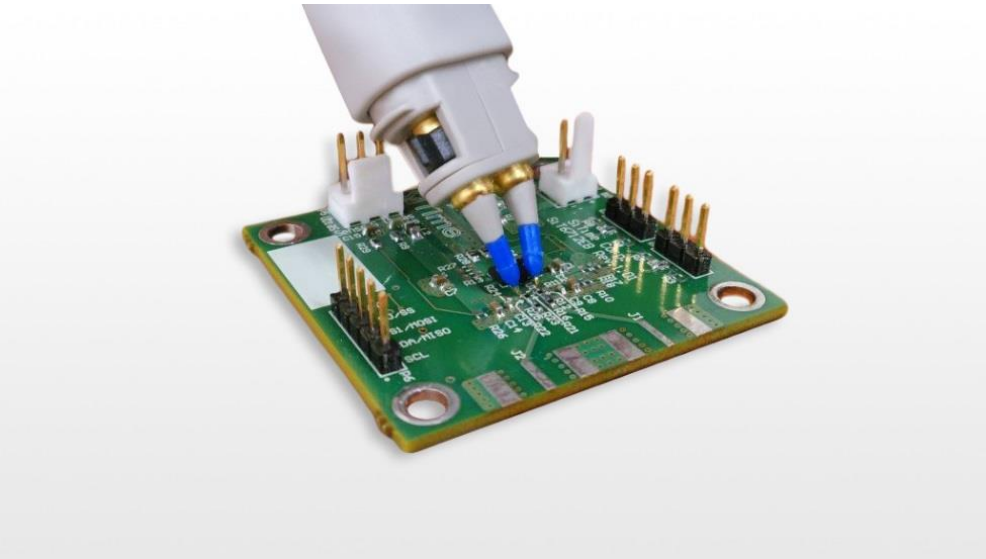

Figure 8: Differential browser (high impedance active probe) on test points for waveform capturing on the SiT6712EB EVB

3.4 Jitter Measurement

For jitter measurement, configurations described in 3.1.1 (LVPECL), 3.1.4 (LVDS) and 3.1.6 (HCSL) should be used. Jitter measurement technique is described in SiTime application note AN10007.

Appendix A – Schematic, BOM and Layout of SiT6712EB

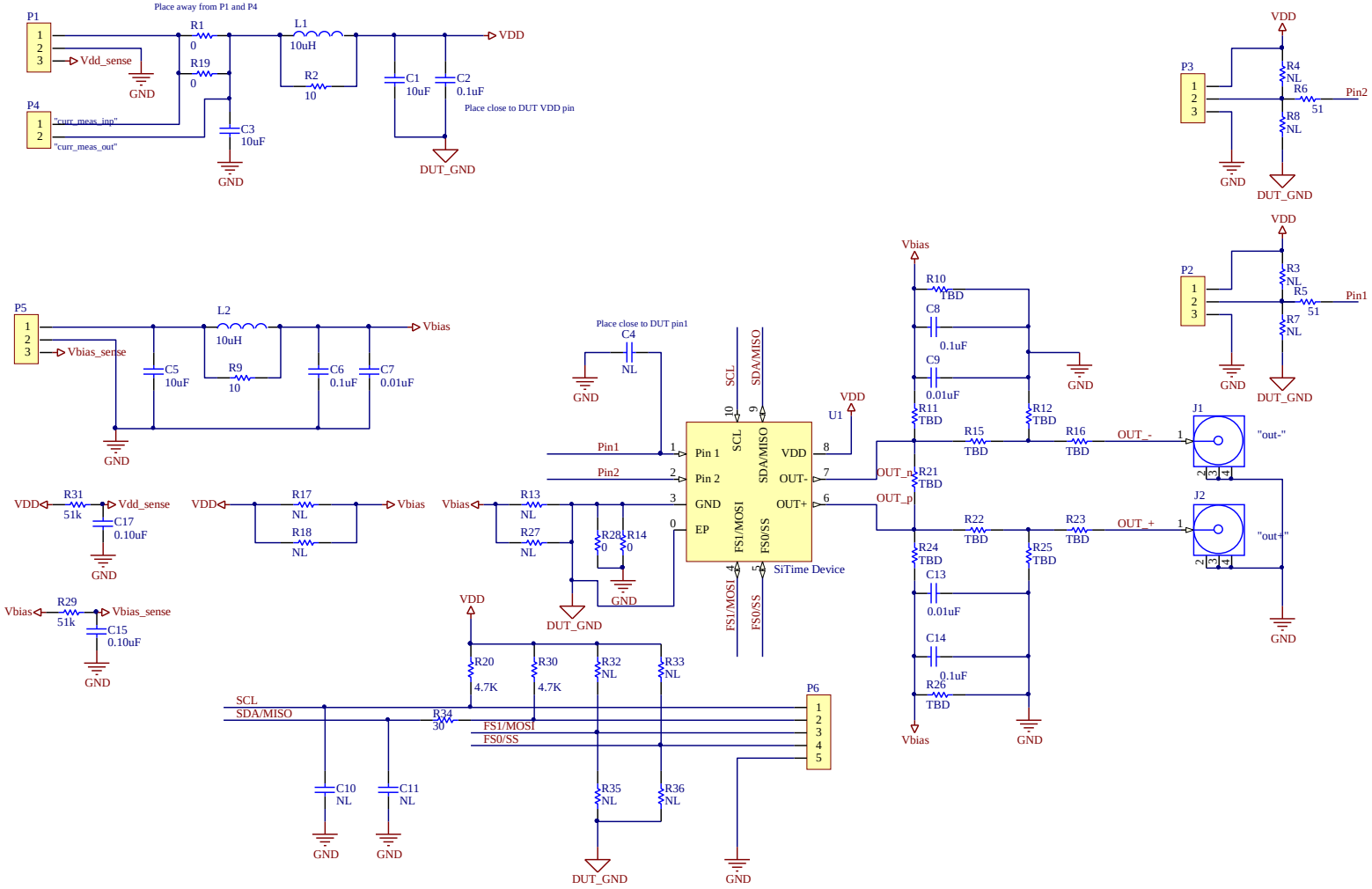

Figure A1: SiT6712EB rev. 2.01 schematic

Table A1: Bill of Materials (BOM)

#	Reference Designators	Description	Qty	SMD component size	Value
1	R1, R19	Resistor	2	0603	0 Ω
2	R14, R28	Resistor	2	0402	0 Ω
3	R2, R9,	Resistor	2	0603	10 Ω
4	R5, R6	Resistor	2	0603	51 Ω
5	R29, R31	Resistor	2	0603	51 kΩ
6	R20, R30	Resistor	2	0603	4.7 kΩ
7	R3, R4, R7, R8, R32, R33, R35, R36	Resistor	8	0603	Don't populated
8	R13, R27, R17, R18	Resistor	4	0402	Don't populated
9	R21	Resistor	1	0603	See Figure 1~8 for values
10	R10, R11, R12, R15, R16, R22, R23, R24, R25, R26	Resistor	10	0402	See Figure 1~8 for values
11	L1, L2	Inductor	2	0805	10 uH
12	C1, C3, C5	Ceramic capacitor	3	0603	10 uF
13	C2	Ceramic capacitor	1	0402	0.1 uF
14	C6, C8, C14, C15, C17	Ceramic capacitor	5	0603	0.1 uF
15	C7, C9, C13	Ceramic capacitor	4	0402	0.01 uF

16	C4	Ceramic capacitor	1	0603	Don't populated
17	C10, C11	Ceramic capacitor	2	0402	Don't populated
18	U1	SiTime Oscillator	1		
19	P1, P5	3-pin connector	2	Through hole, 2.54 mm pitch	
20	P2, P3	3-pin header	2	Through hole, 2.54 mm pitch	
21	P6	5-pin header	1	Through hole, 2.54 mm pitch	
22	P4	2-pin connector	1	Through hole, 2.54 mm pitch	
23	J1, J2	SMA connectors	2		See Figure 1~8 for values

Table A2: Connectors Digi-Key Part Number

Connectors	Digi-Key part number	Digi-Key part number for mating connector	Digi-Key part number for associated products
Power	WM2701-ND	WM2001-ND	WM1114-ND
Vbias	WM2701-ND	WM2001-ND	WM1114-ND
Pin 1	609-3461-ND	76341-303LF-ND	
Pin 2	609-3461-ND	76341-303LF-ND	
Frequency control via I^2C/SPI	609-3462-ND	76341-305LF-ND	
Output	WM5534-ND		
Power Supply Current Measurement	WM2744-ND	WM2011-ND	WM1114-ND

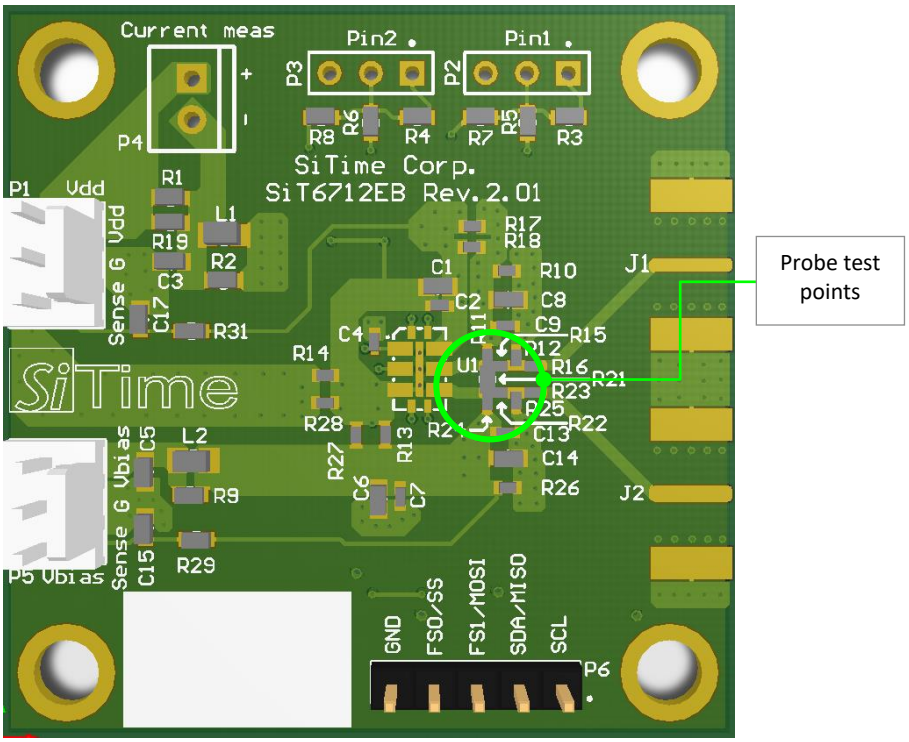

Figure A2: SiT6712EB rev.2.01 layout

Table 2: Revision History

Version	Release Date	Change Summary
1.01	24-Oct-2017	Initial Release
1.02	20-Jan-2023	Updated Appendix A for 2.01 board revision design.

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