
ML610Q793

8-bit Microcontroller for Sensor Control

■ General Description

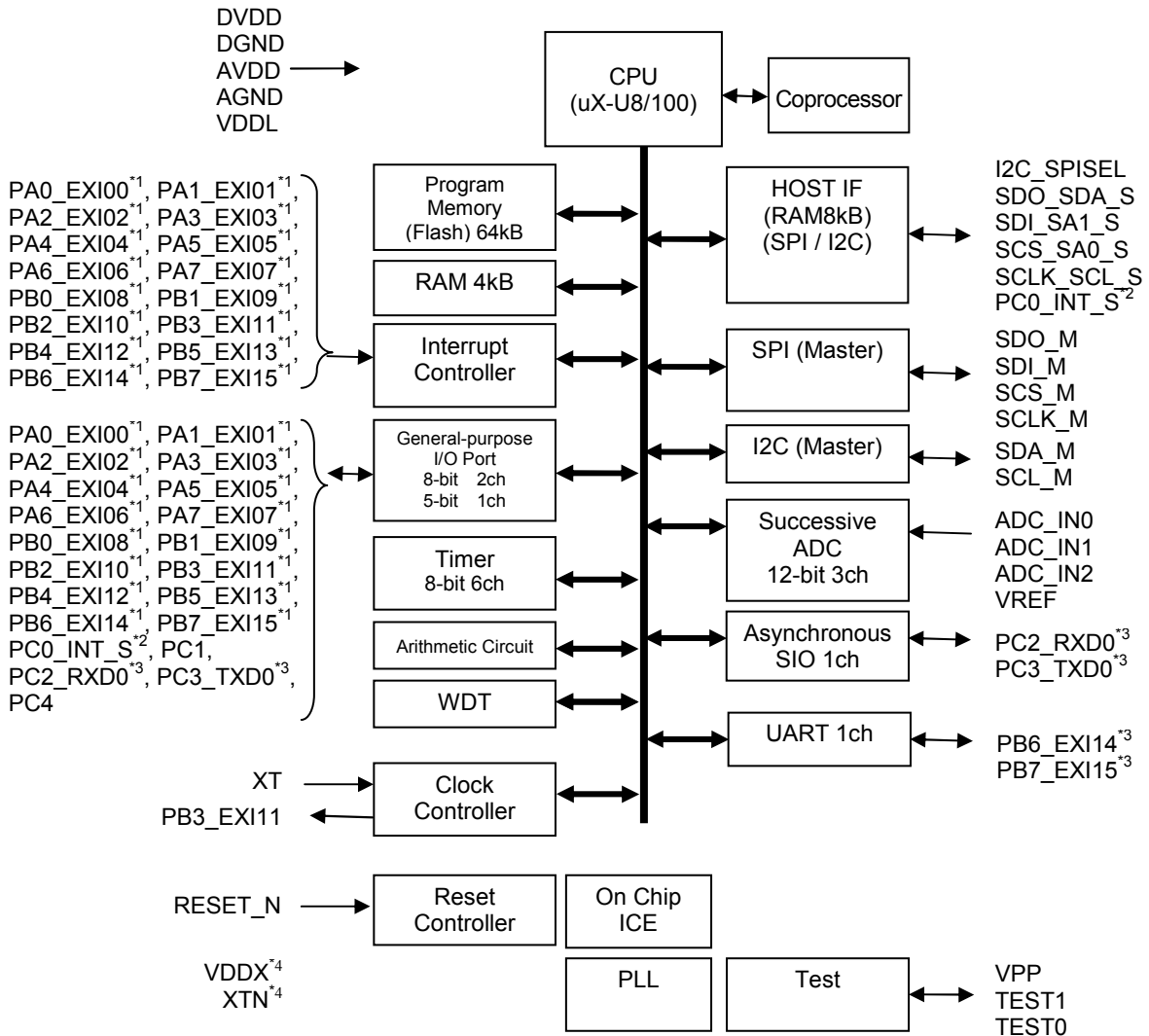
The ML610Q793 is a high-performance 8-bit low power microcontroller optimized for sensor hub, that integrates LAPIS Semiconductor's original high-performance 8-bit CPU core with a 16-bit multiplier/divider co-processor, 64 kByte flash memory, 4 kByte RAM, multiple interfaces for various sensors and host interfaces with 8kByte logging RAM in small footprint package. The ML610Q793 is an ideal sensor hub microcontroller for smart phone to separate various sensors off from its application processor and control them effectively for reducing total system power consumption.

■ Features

- CPU
 - 8-bit RISC CPU (CPU name: uX-U8/100)
 - 16-bit length instruction system
 - Minimum instruction execution time
 - 30.5 us (32.768 kHz system clock)
 - 0.25 us (4.096 MHz system clock)
 - Built-in coprocessor for multiplication, division, and multiply-accumulate operations
 - Multiplication (Input: 16-bit x 16-bit, Output: 32-bit)
 - Division (Input: 32-bit/16-bit, Output: 32-bit)
 - Multiply-accumulate (Input: 16-bit x 16-bit + 32-bit, Output: 32-bit)
- Internal memory
 - 64-kByte Flash ROM (32-kWord x 16-bit)
 - 4-kByte SRAM (4-kWord x 8-bit)
- Interrupt controller
 - Non-maskable interrupt: 1 source
 - Maskable interrupt: 29 sources
 - Number of internal sources: 13 (Timer: 6, ADC: 1, SPI: 1, I2C: 1, HOSTIF: 1, Arithmetic circuit: 1, UART: 1, SIO: 1)
 - Number of external sources: 16
- Timer
 - 8-bit auto-reload timer x 6ch
 - Watchdog timer (WDT) x 1ch
- Serial interface
 - SPI interface with master function x 1ch
 - I2C interface with master function x 1ch
 - UART interface (two-wire, full duplex communication) x 1ch
 - SIO interface (two-wire, half-duplex communication) x 1ch
- Host interface
 - Serial interface with slave function (SPI/I2C selectable) x 1ch
 - Outputs a host processor interrupt x 1ch (secondary function of general-purpose I/O port)
 - 8-kByte RAM for logging

- General-purpose I/O port
 - 8-bit input/output port x 2ch
 - 5-bit input/output port x 1ch
- A/D converter
 - 12-bit successive approximation type A/D converter x 3ch
- Arithmetic circuit
 - Root operation (Input: 18 bit, Output: 19 bit)
- Power consumption control function
 - CPU operation mode
 - Supports high frequency operation and low frequency operation
 - HALT mode Supports the HALT mode for stopping CPU only
Returning for HALT mode : 77usec
- Input clock
 - 32.768 kHz (External clock input)
- Power supply voltage
 - Analog section:(using ADC) 2.5V to 3.6V
(not using ADC) 1.7V to 1.9V
 - Digital I/O section: 1.7V to 1.9V
 - Digital core section: 1.7V to 1.9V
- Power consumption (Normal state)
 - High-speed operation (4.096MHz): 0.93mA
 - HALT Mode: 0.6uA
- Operating frequency
 - High-speed clock: 4.096 MHz
 - Low-speed clock: 32.768kHz
- Operating temperature
 - Ambient temperature: -30°C to +85°C (FLASH erase/programming -30°C to +60°C)
- Package
 - 48-pin WL-CSP (S-UFLGA48-3.06x2.96-0.40-W)

■ Block Diagram



*1 Shared by the interrupt pins and the general-purpose I/O port
 *2 Shared by the interrupt output pin of the host interface and the general-purpose I/O port
 *3 Shared by the UART/Asynchronous SIO transmit/receive pins and the general-purpose I/O port
 *4 Leave this pin open in ML610Q793

■ Pin Configuration (Top View)

| | | | | | | | |
|------------|---------|------------|-----------|-----------|-----------|-----------|---|
| DGND | DVDD | SDA_M | PA2_EXI02 | PA5_EXI05 | PB0_EXI08 | PB3_EXI11 | 7 |
| AVDD | VDDX | VDDL | PA1_EXI01 | PA4_EXI04 | PA7_EXI07 | PB2_EXI10 | 6 |
| ADC_IN1 | AGND | SCL_M | PA0_EXI00 | PA3_EXI03 | PB1_EXI09 | VPP | 5 |
| ADC_IN2 | VREF | ADC_IN0 | PC1 | PA6_EXI06 | PB7_EXI15 | PC2_RXD0 | 4 |
| XTN | TEST0 | PC4 | SCS_SA0_S | SDI_M | X | PB4_EXI12 | 3 |
| XT | TEST1 | SDO_SDA_S | SDI_SA1_S | SCS_M | PB6_EXI14 | PC3_TXD0 | 2 |
| I2C_SPISEL | RESET_N | SCLK_SCL_S | SDO_M | SCLK_M | PC0_INT_S | PB5_EXI13 | 1 |
| G | F | E | D | C | B | A | |

48-pin WL-CSP Package(S-UFLGA48-3.06x2.96-0.40-W)
(Bottom View)

■ List of Pins

| PIN No. | Symbol | Input/output | Polarity | Function |
|---------|------------|--------------|----------|---|
| F5 | AGND | — | — | Analog GND |
| G6 | AVDD | — | — | Analog power supply |
| G7 | DGND | — | — | Digital IO/core GND |
| F7 | DVDD | — | — | Digital I/O power supply |
| E6 | VDDL | — | — | Digital core power supply |
| F6 | VDDX | — | — | Pins unused |
| G1 | I2C_SPISEL | I | — | Selects the interface with the host I2C interface when I2C_SPISEL = 1 SPI interface when I2C_SPISEL = 0 |
| E2 | SDO_SDA_S | IO | — | SDA of I2C slave interface when I2C_SPISEL = 1 |
| | | O | — | SDO of SPI slave interface when I2C_SPISEL = 0 (This signal status is Hi-Z except for output data.) |
| D2 | SDI_SA1_S | I | — | I2C slave address when I2C_SPISEL = 1 |
| | | I | — | SDI of SPI slave interface when I2C_SPISEL = 0 |
| D3 | SCS_SA0_S | I | — | I2C slave address when I2C_SPISEL = 1 |
| | | I | Positive | SCS of SPI slave interface when I2C_SPISEL = 0 |
| E1 | SCLK_SCL_S | I | — | SCL of I2C slave interface when I2C_SPISEL = 1 |
| | | I | — | SCLK of SPI slave interface when I2C_SPISEL = 0 |
| E7 | SDA_M | IO | — | SDA of I2C master interface |
| E5 | SCL_M | O | — | SCL of I2C master interface |
| D1 | SDO_M | O | — | SDO of SPI master interface |
| C3 | SDI_M | I | — | SDI of SPI master interface |
| C2 | SCS_M | O | Positive | SCS of SPI master interface |
| C1 | SCLK_M | O | — | SCLK of SPI master interface |
| G4 | ADC_IN2 | — | — | Successive ADC input 2 |
| G5 | ADC_IN1 | — | — | Successive ADC input 1 |
| E4 | ADC_IN0 | — | — | Successive ADC input 0 |
| F4 | VREF | — | — | Successive ADC reference voltage input |
| B1 | PC0_INT_S | IO | — | General-purpose input/output port for the primary function |
| | | O | Negative | Interrupt output for host interface for the secondary function |
| D4 | PC1 | IO | — | General-purpose input/output port |
| A4 | PC2_RXD0 | IO | — | General-purpose input/output port for the primary function |
| | | I | — | Asynchronous SIO receive data for the secondary function |
| A2 | PC3_TXD0 | IO | — | General-purpose input/output port for the primary function |
| | | O | — | Asynchronous SIO transmit data for the secondary function |
| E3 | PC4 | IO | — | General-purpose input/output port |
| D5 | PA0_EXI00 | IO | — | General-purpose input/output port/external interrupt input |
| D6 | PA1_EXI01 | IO | — | General-purpose input/output port/external interrupt input |
| D7 | PA2_EXI02 | IO | — | General-purpose input/output port/external interrupt input |
| C5 | PA3_EXI03 | IO | — | General-purpose input/output port/external interrupt input |
| C6 | PA4_EXI04 | IO | — | General-purpose input/output port/external interrupt input |
| C7 | PA5_EXI05 | IO | — | General-purpose input/output port/external interrupt input |
| C4 | PA6_EXI06 | IO | — | General-purpose input/output port/external interrupt input |
| B6 | PA7_EXI07 | IO | — | General-purpose input/output port/external interrupt input |
| B7 | PB0_EXI08 | IO | — | General-purpose input/output port/external interrupt input |
| B5 | PB1_EXI09 | IO | — | General-purpose input/output port/external interrupt input |
| A6 | PB2_EXI10 | IO | — | General-purpose input/output port/external interrupt input |

| | | | | |
|----|-----------|----|----------|---|
| A7 | PB3_EXI11 | IO | — | General-purpose input/output port/external interrupt input |
| | | O | — | 32.768kHz clock for output |
| A3 | PB4_EXI12 | IO | — | General-purpose input/output port/external interrupt input |
| A1 | PB5_EXI13 | IO | — | General-purpose input/output port/external interrupt input |
| B2 | PB6_EXI14 | IO | — | General-purpose input/output port/external interrupt input for the primary function |
| | | I | — | UART receive data for the secondary function |
| B4 | PB7_EXI15 | IO | — | General-purpose input/output port/external interrupt input for the primary function |
| | | O | — | UART transmit data for the secondary function |
| F1 | RESET_N | I | Negative | System reset input |
| G2 | XT | I | — | External clock input |
| G3 | XTN | IO | — | Unused pin (Leave this pin open) |
| A5 | VPP | I | — | FLASH test pin |
| F2 | TEST1 | I | — | Test pin |
| F3 | TEST0 | I | — | Test pin/remap pin (for firmware update) |

■ Termination of Unused Pins

| Pin | Recommended pin termination |
|--|--|
| VPP | Leave this pin open. |
| VDDX | Leave this pin open. |
| XTN | Leave this pin open. |
| TEST0 | Leave this pin open. |
| TEST1 | Leave this pin open. |
| RESET_N | Leave this pin as open, or connect a pull-up resistor. |
| PA0~PA7 | Leave this pin open (refer to Note). |
| PB0~PB7 | Leave this pin open (refer to Note). |
| PC0~PC4 | Leave this pin open (refer to Note). |
| ADC_IN0~2 | Leave this pin open. |
| VREF | Leave this pin open. |
| SDA_M, SCL_M | Leave this pin open. |
| SDO_M, SCS_M, SCLK_M | Leave this pin open. |
| SDI_M | Connect this pin to a pull-down resistor. |
| SCLK_SCL_S, SCS_SA0_S, SDI_SA1_S, SDO_SDA_S | Apply low level to I2C_SPISEL pin, and connect these pins to a pull-down resistor. |

[Note:]

The supply current flow may become excessively large if the pins of unused input ports and input/output ports are left open with the high impedance input setting. It is recommended to set those ports to input mode with a pull-down resistor, input mode with a pull-up resistor, or output mode by setting the port control register.

■ Host Interface

The ML610Q793 controls various sensors via the host interface. The host interface provides selectable I2C/SPI interface and interrupt signals to the host processor, and includes an 8-bit and a 16-bit register address space and an 8-kByte FIFO.

● Register Map

| Address | | Name | Symbol (Byte) | R/W | Size | Initial Value |
|-------------|-------------|-------------------------------------|---------------|-----|------|---------------|
| Write | Read | | | | | |
| 00H | 80H | Configuration register | CFG | R/W | 8 | 00H |
| 01H | 81H | Sensor interrupt mask register 0 | INTMSK0 | R/W | 8 | FFH |
| 02H | 82H | Sensor interrupt mask register 1 | INTMSK1 | R/W | 8 | FFH |
| 03H~ 07H | 83H~ 87H | reserved | — | — | — | — |
| 08H | 88H | Operation status register | STATUS | R/— | 8 | FEH |
| 09H | 89H | Sensor interrupt request register 0 | INTREQ0 | R/— | 8 | 00H |
| 0AH | 8AH | Sensor interrupt request register 1 | INTREQ1 | R/— | 8 | 00H |
| 0BH | 8BH | Error code register 0 | ERROR0 | R/— | 8 | 00H |
| 0CH | 8CH | Error code register 1 | ERROR1 | R/— | 8 | 00H |
| 0DH~ 0FH | 8DH~ 8FH | reserved | — | — | — | — |
| 10H | 90H | Command register 0 | CMD0 | R/W | 8 | 00H |
| 11H | 91H | Command register 1 | CMD1 | R/W | 8 | 00H |
| 12H | 92H | Parameter register 0 | PRM0 | R/W | 8 | 00H |
| 13H | 93H | Parameter register 1 | PRM1 | R/W | 8 | 00H |
| 14H | 94H | Parameter register 2 | PRM2 | R/W | 8 | 00H |
| 15H | 95H | Parameter register 3 | PRM3 | R/W | 8 | 00H |
| 16H | 96H | Parameter register 4 | PRM4 | R/W | 8 | 00H |
| 17H | 97H | Parameter register 5 | PRM5 | R/W | 8 | 00H |
| 18H | 98H | Parameter register 6 | PRM6 | R/W | 8 | 00H |
| 19H | 99H | Parameter register 7 | PRM7 | R/W | 8 | 00H |
| 1AH | 9AH | Parameter register 8 | PRM8 | R/W | 8 | 00H |
| 1BH | 9BH | Parameter register 9 | PRM9 | R/W | 8 | 00H |
| 1CH | 9CH | Parameter register A | PRMA | R/W | 8 | 00H |
| 1DH | 9DH | Parameter register B | PRMB | R/W | 8 | 00H |
| 1EH | 9EH | Parameter register C | PRMC | R/W | 8 | 00H |
| 1FH | 9FH | Command entry register | ENT | R/W | 8 | 00H |
| 20H | A0H | Result register 00 | RSLT00 | R/— | 8/16 | 00H |
| 21H | A1H | Result register 01 | RSLT01 | R/— | 8 | 00H |
| 22H | A2H | Result register 02 | RSLT02 | R/— | 8/16 | 00H |
| 23H | A3H | Result register 03 | RSLT03 | R/— | 8 | 00H |
| 24H | A4H | Result register 04 | RSLT04 | R/— | 8/16 | 00H |
| 25H | A5H | Result register 05 | RSLT05 | R/— | 8 | 00H |
| 26H | A6H | Result register 06 | RSLT06 | R/— | 8/16 | 00H |
| 27H | A7H | Result register 07 | RSLT07 | R/— | 8 | 00H |
| 28H | A8H | Result register 08 | RSLT08 | R/— | 8/16 | 00H |
| 29H | A9H | Result register 09 | RSLT09 | R/— | 8 | 00H |
| 2AH | AAH | Result register 0A | RSLT0A | R/— | 8/16 | 00H |
| 2BH | ABH | Result register 0B | RSLT0B | R/— | 8 | 00H |
| 2CH | ACH | Result register 0C | RSLT0C | R/— | 8/16 | 00H |
| 2DH | ADH | Result register 0D | RSLT0D | R/— | 8 | 00H |

| | | | | | | |
|-------------|-------------|--------------------|--------|-----|------|-----------|
| 2EH | AEH | Result register 0E | RSLT0E | R/— | 8/16 | 00H |
| 2FH | AFH | Result register 0F | RSLT0F | R/— | 8 | 00H |
| 30H | B0H | Result register 10 | RSLT10 | R/— | 8/16 | 00H |
| 31H | B1H | Result register 11 | RSLT11 | R/— | 8 | 00H |
| 32H | B2H | Result register 12 | RSLT12 | R/— | 8/16 | 00H |
| 33H | B3H | Result register 13 | RSLT13 | R/— | 8 | 00H |
| 34H | B4H | Result register 14 | RSLT14 | R/— | 8/16 | 00H |
| 35H | B5H | Result register 15 | RSLT15 | R/— | 8 | 00H |
| 36H | B6H | Result register 16 | RSLT16 | R/— | 8/16 | 00H |
| 37H | B7H | Result register 17 | RSLT17 | R/— | 8 | 00H |
| 38H | B8H | Result register 18 | RSLT18 | R/— | 8/16 | 00H |
| 39H | B9H | Result register 19 | RSLT19 | R/— | 8 | 00H |
| 3AH | BAH | Result register 1A | RSLT1A | R/— | 8/16 | 00H |
| 3BH | BBH | Result register 1B | RSLT1B | R/— | 8 | 00H |
| 3CH | BCH | Result register 1C | RSLT1C | R/— | 8/16 | 00H |
| 3DH | BDH | Result register 1D | RSLT1D | R/— | 8 | 00H |
| 3EH | BEH | Result register 1E | RSLT1E | R/— | 8/16 | 00H |
| 3FH | BFH | Result register 1F | RSLT1F | R/— | 8 | 00H |
| 40H | C0H | Result register 20 | RSLT20 | R/W | 8 | Undefined |
| 41H~ 7FH | C1H~ FFH | reserved | — | — | — | — |

● Configuration Register CFG

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------|-------|-----|-----|-----|--------|-----|-----|
| CFG | REGMD | SPI3M | — | — | — | INTLVL | — | — |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REGMD:

Sets the access mode of the serial interface (I2C/SPI). Set to "0" to increment the internal address by 1 each time a 1-byte data is transmitted/received. Set to "1" to fix the address to the same address.

The Result register 20 is not intended. In addition, there is prohibition that set to "0" to this register and read successively for Result register "IF" to "20".

SPI3M:

If the host interface is set "SPI" (apply low level to I2C_SPISEL pin), sets the interface type(3-wires or 4-wires) of SPI communication. Set to "0" for 4-wires mode, or set to "1" for 3-wires mode.

INTLVL:

Sets the interrupt level. Set to "0" for pulse output, or set to "1" for level output.

● Sensor Interrupt Mask Register INTMSK0, INTMSK1

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| INTMSK0 | MSK0[7] | MSK0[6] | MSK0[5] | MSK0[4] | MSK0[3] | MSK0[2] | MSK0[1] | MSK0[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| INTMSK1 | MSK1[7] | MSK1[6] | MSK1[5] | MSK1[4] | MSK1[3] | MSK1[2] | MSK1[1] | MSK1[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

MSK0[7:0]:

Masks the interrupt notification to the host processor by the sensor interrupt request register (INTREQ0). Set to "0" to mask the interrupt notification by REQ0[n] bit of INTREQ0. Set to "1" not to mask the interrupt notification.

MSK1[7:0]:

Masks the interrupt notification to the host processor by the sensor interrupt request register (INTREQ1). Set to "0" to mask the interrupt notification by REQ1[n] bit of INTREQ1. Set to "1" not to mask the interrupt notification.

● Operation Status Register STATUS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| STATUS | ST[7] | ST[6] | ST[5] | ST[4] | ST[3] | ST[2] | ST[1] | ST[0] |
| R/W | R/— | R/— | R/— | R/— | R/— | R/— | R/— | R/— |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ST[n](N=7 to 0):

Indicates the status of sensor measurement.

Read successively for STAUS, INTREO0, INTERO1 by address increments mode.

● Sensor Interrupt Request Register INTREQ_n (n = 0, 1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| INTREQ _n | REQ _n [7] | REQ _n [6] | REQ _n [5] | REQ _n [4] | REQ _n [3] | REQ _n [2] | REQ _n [1] | REQ _n [0] |
| R/W | R/— | R/— | R/— | R/— | R/— | R/— | R/— | R/— |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REQ_n[7:0]:

Indicates the interrupt source to the host processor. Each bit of this register is cleared by being read by the host processor.

Read successively for INTREO0, INTERO1 by address increments mode.

* In competition clear by the reading from a host processor and write from the CPU occurs, Writing from the CPU may not be reflected in this register.

Therefore controls so that access of the CPU and access of the host processor do not compete.

In cases the competition is non avoidable, refer to [ML610Q793 SDK software manuals].

Provide Software avoiding competition for Software Development Kit [SDK].

● Error Code Register ERROR_n (n = 0, 1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| ERROR _n | ER _n [7] | ER _n [6] | ER _n [5] | ER _n [4] | ER _n [3] | ER _n [2] | ER _n [1] | ER _n [0] |
| R/W | R/— | R/— | R/— | R/— | R/— | R/— | R/— | R/— |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REQ_n[7:0]:

Indicates the ERROR Code of host processor.

● Command Register CMD_n (n = 0, 1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| CMD _n | CMD _n [7] | CMD _n [6] | CMD _n [5] | CMD _n [4] | CMD _n [3] | CMD _n [2] | CMD _n [1] | CMD _n [0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CMD_n[7:0]:

This register sets the measurement conditions of sensors and inputs commands such as measurement start/stop.

- Parameter Register PRM n ($n = 0$ to 9, A to C)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| PRM n | PRM n [7] | PRM n [6] | PRM n [5] | PRM n [4] | PRM n [3] | PRM n [2] | PRM n [1] | PRM n [0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PRM n [7:0]:

This register sets the parameters of commands.

- Command Entry Register ENT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| ENT | — | — | — | — | — | — | — | ENT |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ENT:

After a command is set, set this bit "1" to notify the CPU of the command. When the CPU receives the command, this bit is cleared.

- Result Register RSLT n ($n = 00$ to 1F)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| RSLT n | RSLT n [7] | RSLT n [6] | RSLT n [5] | RSLT n [4] | RSLT n [3] | RSLT n [2] | RSLT n [1] | RSLT n [0] |
| R/W | R/— | R/— | R/— | R/— | R/— | R/— | R/— | R/— |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSLT n [7:0]:

This register indicates the command processing result.

- Result Register RSLT20

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----------|------------|------------|------------|------------|------------|------------|------------|
| RSLT20 | RSLT20[7] | RSLT20 [6] | RSLT20 [5] | RSLT20 [4] | RSLT20 [3] | RSLT20 [2] | RSLT20 [1] | RSLT20 [0] |
| R/W | R/— | R/— | R/— | R/— | R/— | R/— | R/— | R/— |
| Initial Value | X | X | X | X | X | X | X | X |

RSLT20[7:0]:

This register indicates the command processing result. As this register has a FIFO structure, read data with the given size.

This register can be written from a host processor only when using firmware update software which SDK offers. For details, please refer to a [ML610Q793 SDK firm updates software manuals].

■ Absolute Maximum Ratings

(DGND=AGND=0V)

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------------|-----------|--------------------------|----------------------|------------------|
| Power supply voltage (Digital I/O) | V_{DD} | $T_a = 25^\circ\text{C}$ | -0.3 to +4.6 | V |
| Power supply voltage (Digital CORE) | V_{DDL} | $T_a = 25^\circ\text{C}$ | -0.3 to +3.6 | |
| Power supply voltage (Analog) | V_{DDA} | $T_a = 25^\circ\text{C}$ | -0.3 to +4.6 | |
| Input voltage | V_{IN} | $T_a = 25^\circ\text{C}$ | -0.3 to $V_{DD}+0.3$ | |
| Output current | I_{OUT} | $T_a = 25^\circ\text{C}$ | -12 to +11 | mA |
| Power dissipation | PD | $T_a = 25^\circ\text{C}$ | 0.9 | W |
| Storage temperature | T_{STG} | — | -55 to +150 | $^\circ\text{C}$ |

■ Recommended Operation Conditions

(DGND=AGND=0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|------------------|-----------------------------|--------|--------|-----------|------------------|
| Power supply voltage (Digital I/O) | V_{DD} | — | 1.7 | 1.8 | 1.9 | V |
| Power supply voltage (Digital CORE) | V_{DDL} | — | 1.7 | 1.8 | 1.9 | |
| Power supply voltage (Analog) | V_{DDA} | UsesADC | 2.5 | 3.3 | 3.6 | |
| | | Unuses ADC | 1.7 | 1.8 | 1.9 | |
| Analog reference voltage | V_{REF} | — | 2.2 | — | V_{DDA} | |
| Auto transient response (VDDL) | ΔV_{out} | — | — | — | ± 19 | mV |
| Clock input frequency | f_{CLK} | — | 32.441 | 32.768 | 33.095 | kHz |
| Ambient temperature | T_a | normal operation | -30 | 25 | +85 | $^\circ\text{C}$ |
| | | FLASH erase/write operation | -30 | 25 | +60 | |

■ Operating Conditions of Flash Memory

(DGND=AGND=0V)

| Parameter | Symbol | Condition | Range | Unit |
|-------------------------------|-----------|-----------------------|------------|------------------|
| Operating temperature | T_{OP} | read operation | -30 to +85 | $^\circ\text{C}$ |
| | | erase/write operation | -30 to +60 | |
| Power supply voltage | V_{DDL} | — | 1.7 to 1.9 | V |
| Rewrite count | C_{EP} | — | 100 | cycles |
| VDDL pin external capacitance | C_{LO} | — | 10 | years |

■ Electrical Characteristics

● DC Characteristics (1/2)

(DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|--------|-------------------------------|------|------|------|------|
| Power consumption (HALT) | IDD2 | CPU stop *1,*2 | - | 0.6 | 16.5 | μA |
| Power consumption (Low-speed operation) | IDD3 | CPU 32 kHz operation *1,*2 | - | 7.5 | 25 | μA |
| Power consumption (High-speed operation 1) | IDD4-1 | CPU 4 MHz operation *2 | - | 0.93 | 1.3 | mA |
| Power consumption (High-speed operation 2) | IDD4-2 | CPU 4 MHz operation | - | 1.5 | 2.3 | mA |

*1 The low-speed clock operates, and only the high-speed clock (PLL) stops

*2 The successive approximation type ADC stops

● DC Characteristics (2/2)

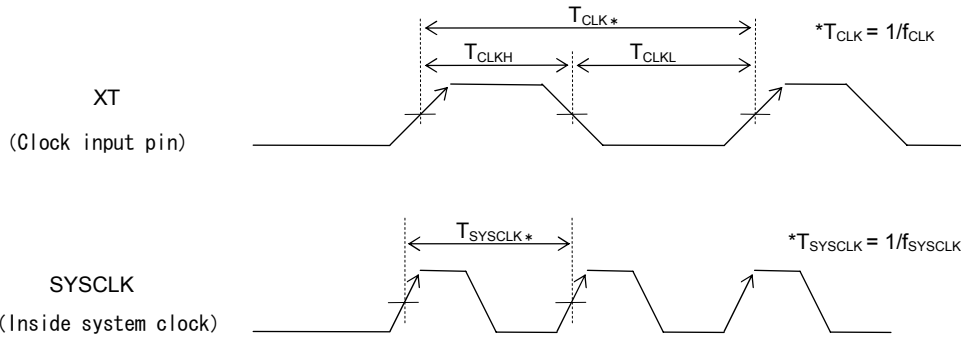
(DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|--------|---|---------------|------|---------------|------|
| Output voltage 1 (SDA_M,SCL_M) | VOH1 | - | - | - | - | V |
| | VOL1 | IOL1 = +0.5mA | - | - | 0.5 | |
| Output leakage 1 (SDA_M,SCL_M) | IOOH1 | - | - | - | - | μA |
| | IOOL1 | VOL=0V (in high-impedance state) | -1 | - | - | |
| Output voltage 2 (Excluding SDA_M and SCL_M) | VOH2 | IOH=-0.5mA | DVDD - 0.5 | - | - | V |
| | VOL2 | IOH= 0.5mA | - | - | 0.5 | |
| Output leakage 2 (Excluding SDA_M and SCL_M) | IOOH2 | VOH= V _{DD} (in high-impedance state) | - | - | 1 | μA |
| | IOOL2 | VOL= 0V (in high-impedance state) | -1 | - | - | |
| Input current 1 (RESET_N, TEST1) | IIH1 | VIH1=DVDD | 0 | - | 1 | μA |
| | IIL1 | VIL1 = V _{SS} | -600 | -300 | -2 | |
| Input current 2 (TEST0) | IIH2 | VIH1=DVDD | 2 | 300 | 600 | μA |
| | IIL2 | VIL1 = V _{SS} | -1 | - | 0 | |
| Input current 3 (Excluding RESET_N, TEST1, and TEST0) | IIH3 | VIH1 = DVDD(pull-down) | 2 | 30 | 200 | μA |
| | IIL3 | VIL1 = V _{SS} (pull-up) | -200 | -30 | -2 | |
| | IIH3Z | VIH1=0V (in high-impedance state) | - | - | 1 | |
| | IIL3Z | VIL1=DVDD (in high-impedance state) | -1 | - | - | |
| Input voltage | VIH1 | - | DVDD × 0.7 | - | - | V |
| | VIL1 | - | - | - | DVDD × 0.3 | |

●AC Characteristics (Clock)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

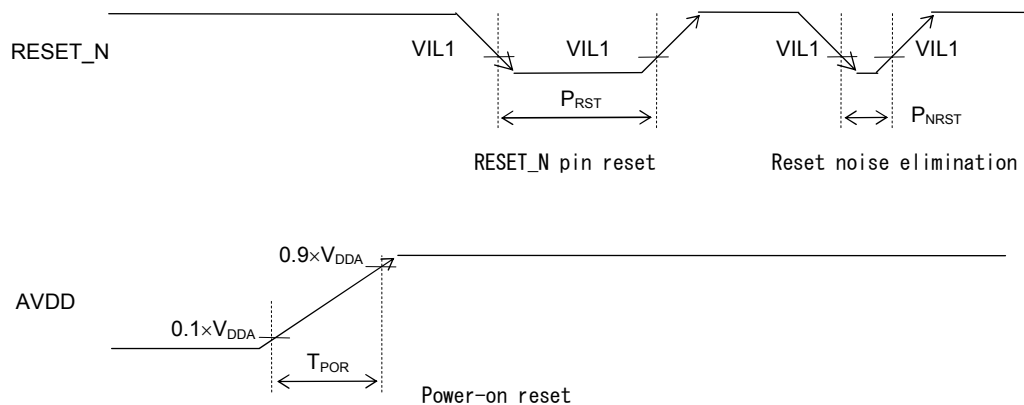
| Parameter | Symbol | Condition | Rating | | | Unit |
|------------------------------|--------------|--------------------------|--------|--------|--------|---------|
| | | | Min. | Typ. | Max. | |
| Input clock frequency | f_{CLK} | - | 32.441 | 32.768 | 33.095 | kHz |
| Input clock High pulse width | T_{CLKH} | - | 9.2 | 15.259 | 21.3 | μs |
| Input clock Low pulse width | T_{CLKL} | - | 9.2 | 15.259 | 21.3 | μs |
| System clock frequency | f_{SYSCLK} | No variable power supply | 3.99 | 4.096 | 4.20 | MHz |
| | | $V_{RPL} \leq 19mV$ | 3.89 | 4.096 | 4.30 | MHz |



●AC Characteristics (Reset)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

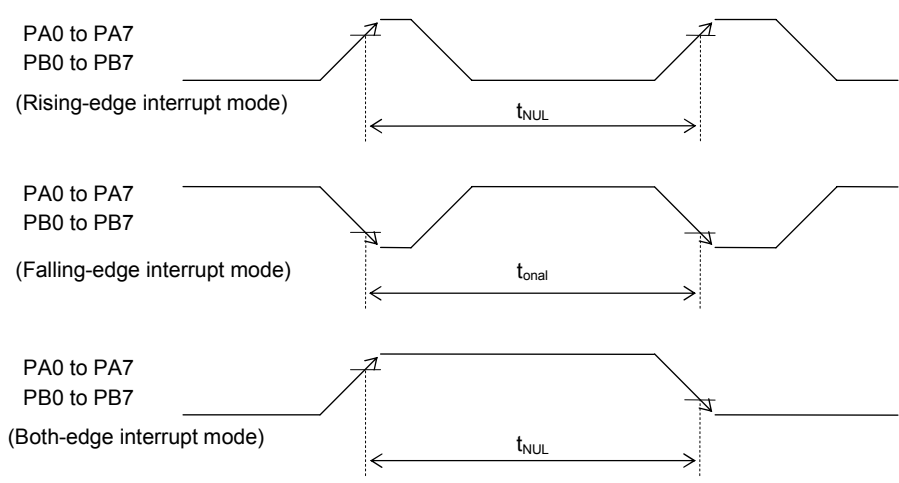
| Parameter | Symbol | Condition | Rating | | | Unit |
|--|------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Reset pulse width | P_{RST} | - | 200 | - | - | μs |
| Reset noise elimination pulse width | P_{NRST} | - | - | - | 0.3 | μs |
| Power on reset generated power rise time | T_{POR} | - | - | - | 10 | ms |



●AC Characteristics (External Interrupt)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|-----------------------------------|-----------|--|--------|------|-------|---------------|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | T_{NUL} | Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz | 76.8 | — | 106.8 | μs |



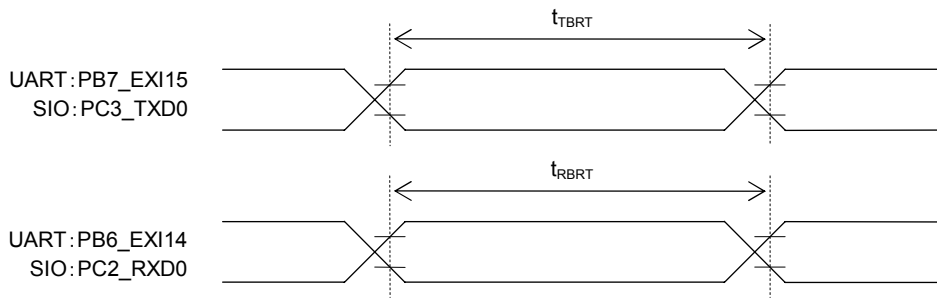
●AC Characteristics (UART/SIO)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9V, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--------------------|------------|-----------|-------------------|------------|-------------------|------|
| | | | Min. | Typ. | Max. | |
| Transmit baud rate | t_{TBRT} | — | — | BRT^{*1} | — | s |
| Receive baud rate | t_{RBRT} | — | BRT^{*1} -3% | BRT^{*1} | BRT^{*1} +3% | s |

*1: UART : Baud rate period set with the UART baud rate dividing register (LSB/MSB).

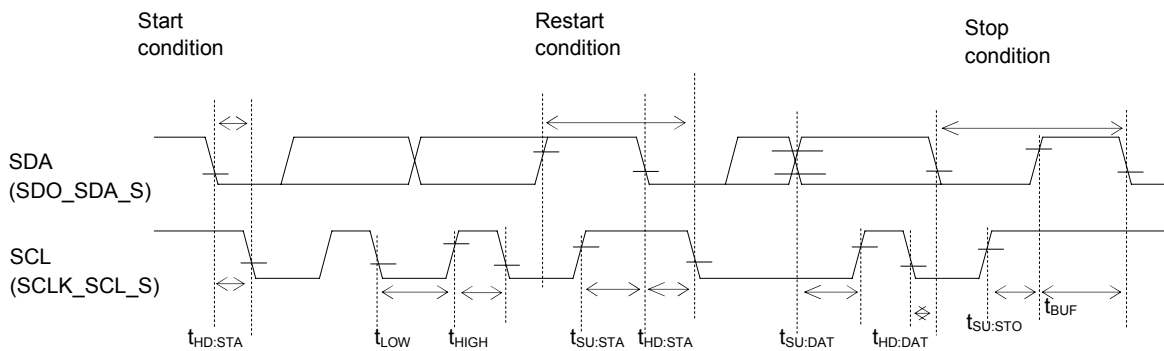
SIO : Baud rate period set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



● AC Characteristics (Host Interface: I2C Slave Interface)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

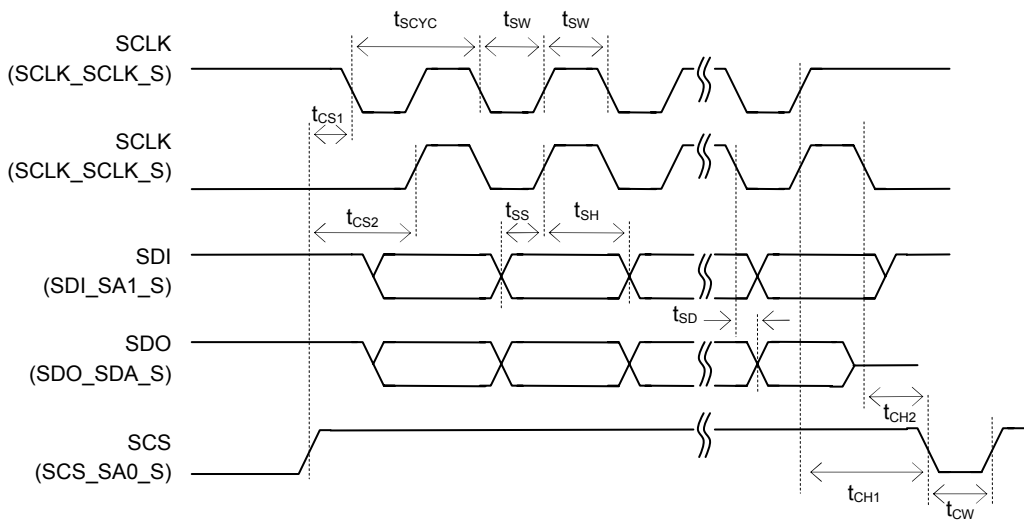
| Parameter | Symbol | Condition | Rating | | | Unit |
|---|--------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f_{SCL} | — | 0 | — | 400 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 0.6 | — | — | μs |
| SCL "L" level time | t_{LOW} | — | 1.3 | — | — | μs |
| SCL "H" level time | t_{HIGH} | — | 0.6 | — | — | μs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 0.6 | — | — | μs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | — | ns |
| SDA setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | μs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 0.6 | — | — | μs |
| Bus-free time | t_{BUF} | — | 1.3 | — | — | μs |



● AC Characteristics (Host Interface: SPI Slave Interface)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|------------------------|------------|-----------|--------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| SCLK input cycle | t_{SCYC} | — | 0.5 | — | — | μs |
| SCLK input pulse width | t_{SW} | — | 0.2 | — | — | μs |
| SCS setup time | t_{CS1} | — | 80 | — | — | ns |
| | t_{CS2} | — | 80 | — | — | ns |
| SCS hold time | t_{CH} | — | 80 | — | — | ns |
| SCS input pulse width | t_{CW} | — | 90 | — | — | ns |
| SDO output delay time | t_{SD} | — | — | — | 240 | ns |
| CLKI input setup time | t_{SS} | — | 80 | — | — | ns |
| SDI input hold time | t_{SH} | — | 80 | — | — | ns |

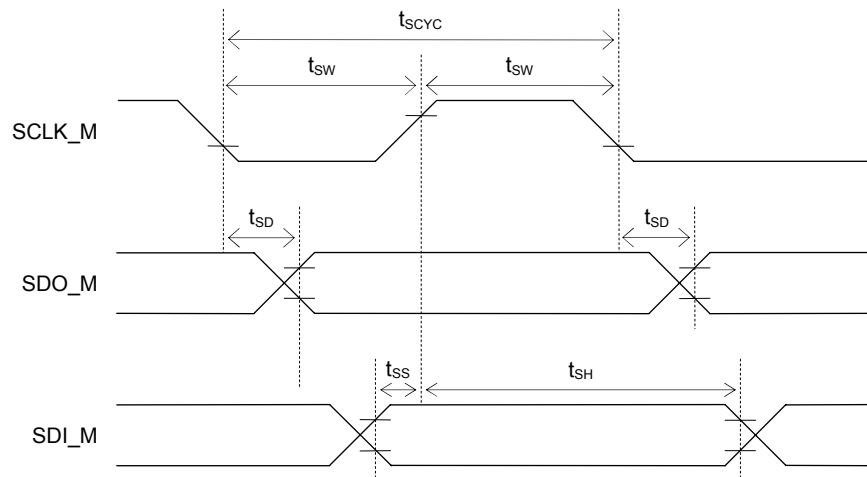


● AC Characteristics (SPI Master Interface)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---------------------------|------------|-----------|------------------------|------------------------|------------------------|------|
| | | | Min. | Typ. | Max. | |
| SCLK_M output cycle | t_{SCYC} | — | — | $SCLK^{*1}$ | — | s |
| SCLK_M output pulse width | t_{SW} | — | $SCLK^{*1} \times 0.4$ | $SCLK^{*1} \times 0.5$ | $SCLK^{*1} \times 0.6$ | s |
| SDO_M output delay time | t_{SD} | — | — | — | 240 | ns |
| SDI_M input setup time | t_{SS} | — | 240 | — | — | ns |
| SDI_M input hold time | t_{SH} | — | 80 | — | — | ns |

*¹: Internal clock cycle selected by the interface register



● AC Characteristics (I2C Master Interface: Standard Mode 100 kHz)

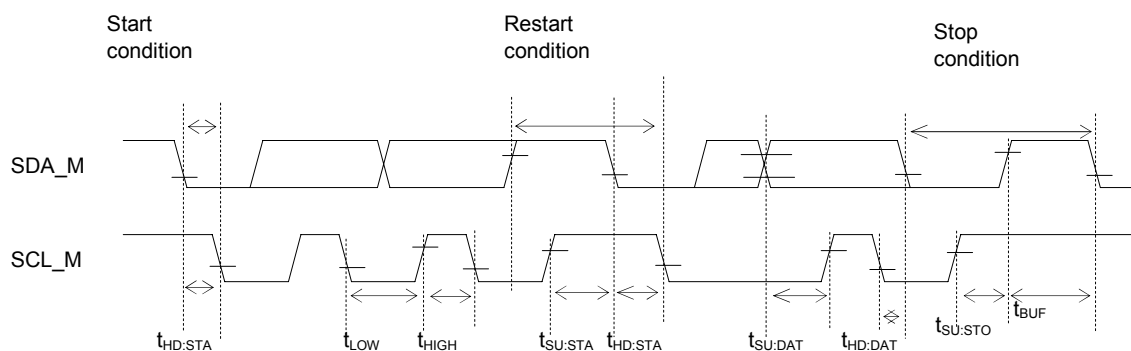
(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|--------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f_{SCL} | — | 0 | — | 100 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 4.0 | — | — | μ s |
| SCL "L" level time | t_{LOW} | — | 4.7 | — | — | μ s |
| SCL "H" level time | t_{HIGH} | — | 4.0 | — | — | μ s |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 4.7 | — | — | μ s |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | — | μ s |
| SDA setup time | $t_{SU:DAT}$ | — | 0.25 | — | — | μ s |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 4.0 | — | — | μ s |
| Bus-free time | t_{BUF} | — | 4.7 | — | — | μ s |

● AC Characteristics (I2C Master Interface: Fast Mode 400 kHz)

(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|--------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| SCL_M clock frequency | f_{SCL} | — | 0 | — | 400 | kHz |
| SCL_M hold time (start/restart condition) | $t_{HD:STA}$ | — | 0.6 | — | — | μ s |
| SCL_M "L" level time | t_{LOW} | — | 1.3 | — | — | μ s |
| SCL_M "H" level time | t_{HIGH} | — | 0.6 | — | — | μ s |
| SCL_M setup time (restart condition) | $t_{SU:STA}$ | — | 0.6 | — | — | μ s |
| SDA_M hold time | $t_{HD:DAT}$ | — | 0 | — | — | μ s |
| SDA_M setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | μ s |
| SDA_M setup time (stop condition) | $t_{SU:STO}$ | — | 0.6 | — | — | μ s |
| Bus-free time | t_{BUF} | — | 1.3 | — | — | μ s |



● Electrical Characteristics of Successive Approximation Type A/D Converter

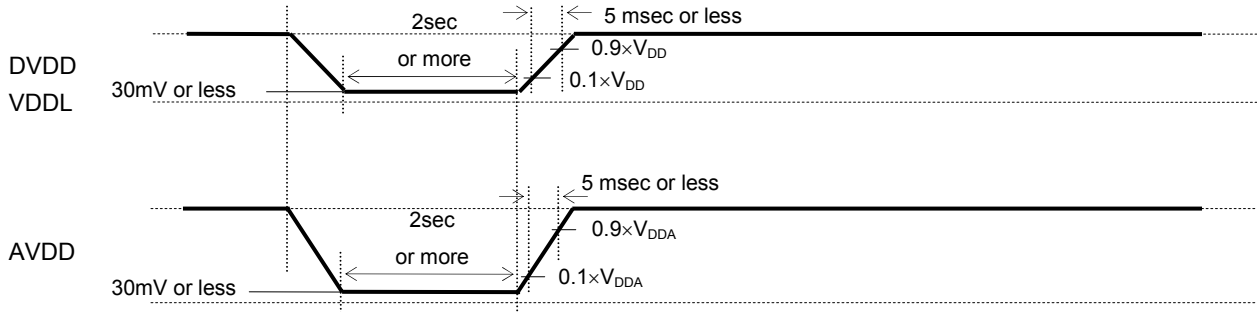
(Unless otherwise specified, DVDD = AVDD = 1.7 to 1.9, DGND = AGND = 0V, Ta = -30 to +85°C)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|-------------------|-------------------------------|--------|------|------------------|------|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | — | 12 | bit |
| Integral non-linearity error margin | INL | $2.7V \leq V_{REF} \leq 3.6V$ | -4 | — | +4 | LSB |
| | | $2.2V \leq V_{REF} \leq 2.7V$ | -6 | — | +6 | |
| Differential non-linearity error margin | DNL | $2.7V \leq V_{REF} \leq 3.6V$ | -3 | — | +3 | |
| | | $2.2V \leq V_{REF} \leq 2.7V$ | -5 | — | +5 | |
| Zero-scale error | V _{OFF} | — | -6 | — | +6 | |
| Full-scale error | FSE | — | -6 | — | +6 | |
| Reference voltage | V _{REF} | — | 2.2 | — | V _{DDA} | V |
| Conversion time | t _{CONV} | At high-speed operation | — | 112 | — | φ/CH |

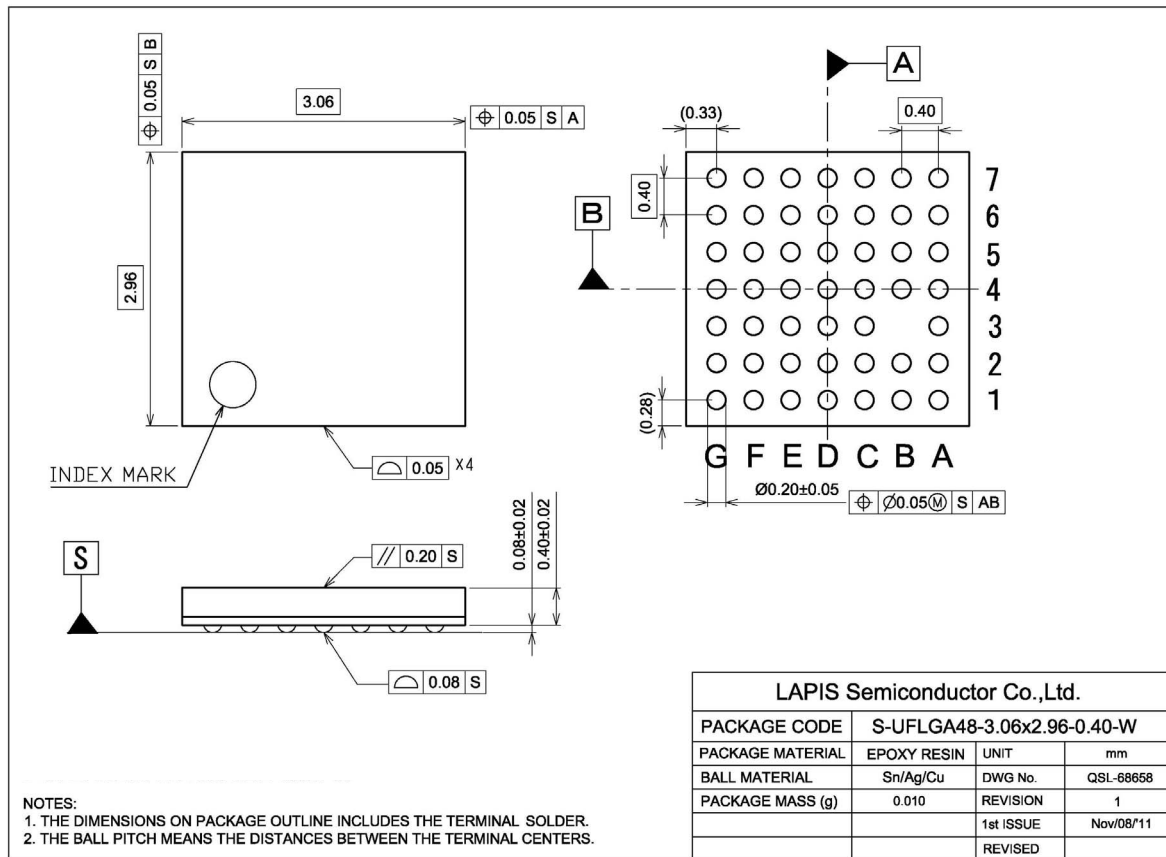
φ: Cycle of high-speed clock

■ Power-On / Power-Off Procedures

Keep the power-on and power-off procedures of DVDD, VDDL and AVDD supply at the same time.
 And DVDD, VDDL supply indetical voltage.
 The timing restrictions are shown as following.



■ Package Dimensions



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■ Revision History

| Document No. | Issue Date | Page | | Description |
|----------------|---------------|------------------|-------------|----------------------------------|
| | | Previous Edition | New Edition | |
| PEDL610Q793-00 | Oct. 20,2012 | — | — | Preliminary first edition issued |
| FEDL610Q793-01 | Jun. 12, 2013 | — | — | First edition issued |

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