



Click here for the 3D model.

Dimensions	
D	25.64mm +/-0.635mm
L	6.35mm MIN
Н	2.54mm NOM
F	1.397mm +/-0.25mm
А	8.13mm MAX
В	9.908mm MAX
С	11.43mm +/-0.635mm
E	12.7mm MAX
К	0.5mm NOM

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	16

General Information		
Series	KPS-MCC Indust COG HT200C	
Style	Leaded Stacked Chip	
Description	Low ESR, Stacked Ceramic Chips	
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance	
RoHS	With Exemptions	
REACH	SVHC (Pb – CAS 7439-92-1)	
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24	
Termination	Silver	
Lead	Straight Leads	
AEC-Q200	No	
Notes	Number of chips in this stack: 6.	

Specifications				
Capacitance	0.47 uF			
Capacitance Tolerance	10%			
Voltage DC	1000 VDC			
Dielectric Withstanding Voltage	1200 VDC			
Temperature Range	-55/+200°C			
Temperature Coefficient	COG			
Dissipation Factor	0.1% 1 kHz 25C			
Aging Rate	0% Loss/Decade Hour			
Insulation Resistance	2.13 GOhms			

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