Micro-stepping Motor Driver

NCV70516

Description

The NCV70516 is a micro−stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. The NCV70516 contains a current−translation table and takes the next micro−step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (= direction) register or input pin. The chip provides an error message if an electrical error, an under−voltage or an elevated junction temperature is detected. It is using a proprietary PWM algorithm for reliable current control.

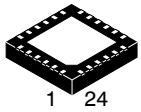
NCV70516 is fully compatible with the automotive voltage requirements and is ideally suited for general−purpose stepper motor applications in the automotive, industrial, medical, and marine environment.

Due to the technology, the device is especially suited for use in applications with fluctuating battery supplies.

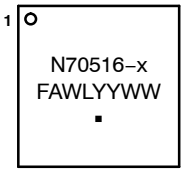
Features

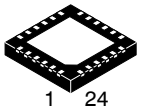
- Dual H−bridge for 2−phase Stepper Motors
- Programmable Peak−current up to 800 mA
- Low Temperature Boost Current up to 1100 mA
- On−chip Current Translator
- SPI Interface
- 5 Step Modes from Full−step up to 16 Micro−steps
- Fully Integrated Current−sensing and Current−regulation
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Fixed PWM Frequency
- Active Fly−back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 3.3 V Microcontrollers, 5 V Tolerant Inputs, 5 V Tolerant Open Drain Outputs
- Reset Function
- Overcurrent Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

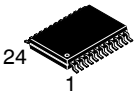


QFN24
CASE 485CS





QFNW24
CASE 484AF



SSOP24
CASE 940AK

N70516 or NV70516 = Specific Device Code
x = 0 or 1
F = Fab Indicator
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

TYPICAL APPLICATION SCHEMATIC

The application schematic below shows typical connections for applications with low axis counts and/or with software SPI implementation. For applications with many stepper motor drivers, some “minimal wiring” examples are shown at the last sections of this datasheet.

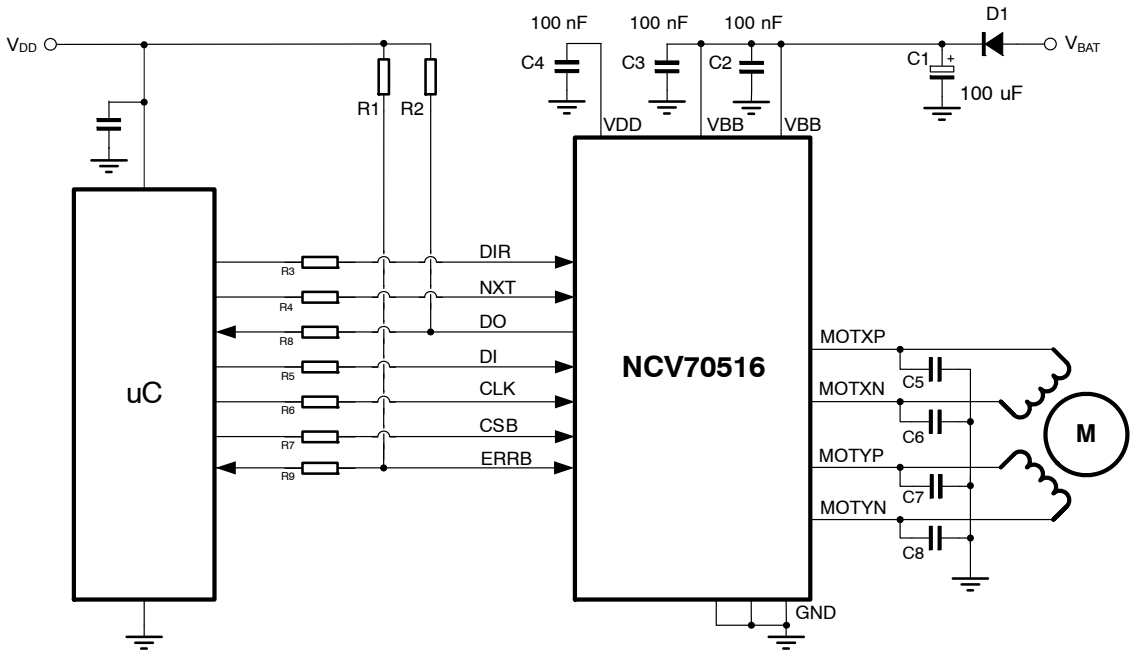


Figure 1. Typical Application Schematic

Table 1. EXTERNAL COMPONENTS

Component	Function	Typ. Value	Max Tolerance	Unit
C1	V_{BB} buffer capacitor (Note 1)	22 ... 100	±20%	μF
C2, C3	V_{BB} decoupling capacitor (Note 2)	100	±20%	nF
C4	V_{DD} decoupling capacitor (Note 3)	100	±20%	nF
C5, C6, C7, C8	Optional EMC filtering capacitor (Note 4)	1 ... 3.3 max	±20%	nF
R1, R2	Pull up resistor	1..5	±10%	kΩ
R3 – R7	Optional resistors	1	±10%	kΩ
R8, R9	Optional resistors (Note 5)	100	±10%	Ω
D1	Optional reverse protection diode	e.g. MURD530		

1. Low ESR < 4 Ω, mounted as close as possible to the NCV70516. Total decoupling capacitance value has to be chosen properly to reduce the supply voltage ripple and to avoid EM emission.
2. C2 and C3 must be close to pins VBB and coupled GND directly.
3. C4 must be a ceramic capacitor to assure low ESR.
4. Optional capacitors for improvement of EMC and system ESD performance. The slope times on motor pins can be longer than specified in the AC table.
5. Value depends on characteristics of μC inputs for DO and ERRB signals.

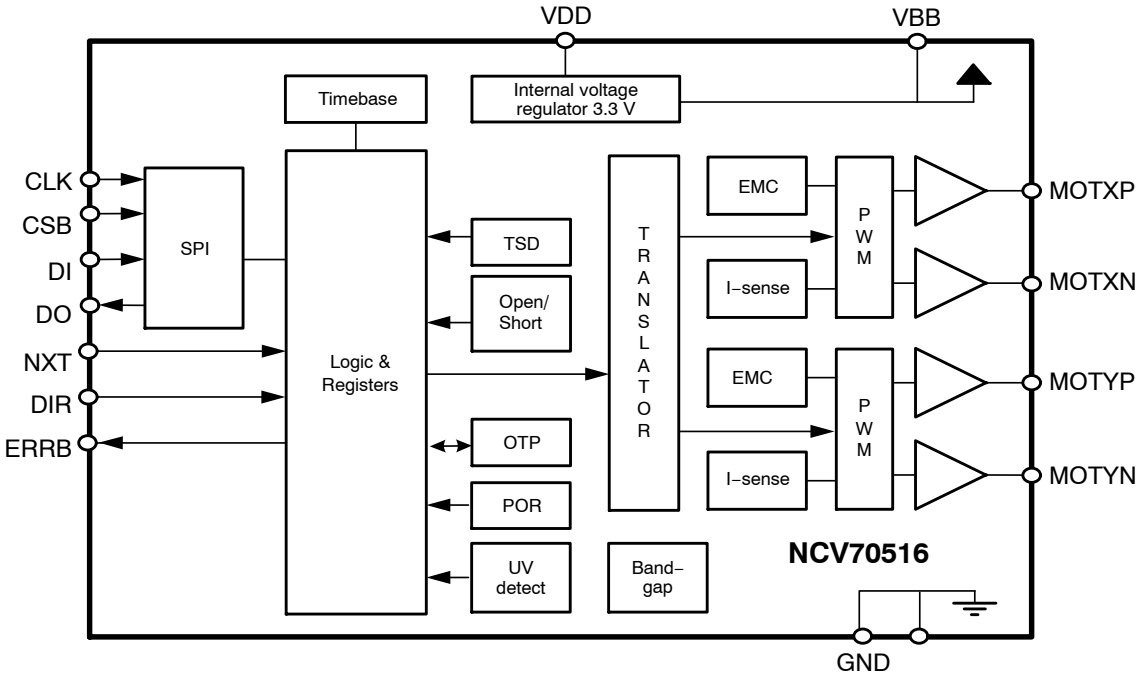


Figure 2. Block Diagram

PACKAGE AND PIN DESCRIPTION

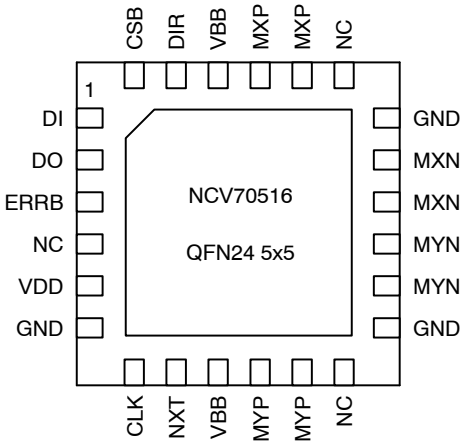


Figure 3. Pin Connections – QFN24

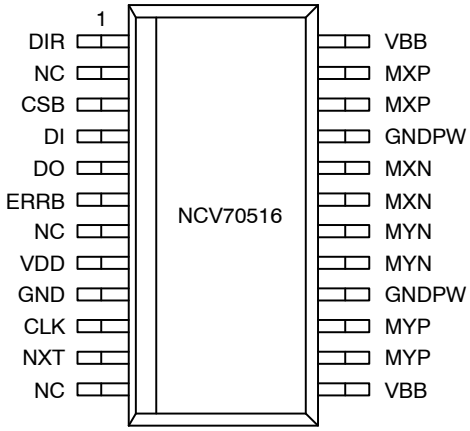


Figure 4. Pin Connections – SSOP24

Table 2. PIN DESCRIPTION

Pin No. QFN24 5x5	Pin No. SSOP24 NB EP	Pin Name	Description	I/O Type
1	4	DI	SPI data input	Digital Input
2	5	DO	SPI data output	Digital Output
3	6	ERRB	Error Output (Open Drain)	Digital Output
4, 12, 19	2, 7, 12	NC	Not connected	
5	8	VDD	Internal supply (needs external decoupling capacitor)	Supply
6	9	GND	Ground	Supply
7	10	CLK	SPI clock input	Digital Input
8	11	NXT	Next micro−step input	Digital Input
9, 22	13, 24	VBB	Battery voltage supply	Supply
10, 11	14, 15	MOTYP	Positive end of phase Y coil	Driver output
13, 18	16, 21	GNDPW	Ground	Supply
14, 15	17, 18	MOTYN	Negative end of phase Y coil	Driver output
16, 17	19, 20	MOTXN	Negative end of phase X coil	Driver output
20, 21	22, 23	MOTXP	Positive end of phase X coil	Driver output
23	1	DIR	Direction input	Digital Input
24	3	CSB	SPI chip select input	Digital Input

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Supply voltage (Note 6)	V_{BB}	−0.3	+40	V
Digital input/outputs voltage	V_{IO}	−0.3	+6.0	V
Junction temperature range (Note 7)	T_j	−50	+175	°C
Storage Temperature (Note 8)	T_{strg}	−55	+160	°C
HBM Electrostatic discharge voltage (Note 9)	V_{esd_hbm}	−2	+2	kV
System Electrostatic discharge voltage (Note 10)	V_{syst_esd}	−8	+8	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. V_{BB} Max is +43 V for limited time <0.5 s.
7. The circuit functionality is not guaranteed.
8. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.
9. HBM according to AEC−Q100: EIA−JESD22−A114−B (100 pF via 1.5 kΩ).
10. System ESD, 150 pF, 330 Ω, contact discharge on the connector pin (VBB, MXN, MXP, MYN and MYP), unpowered.

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 11) is a substantial part of the operation conditions; hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 4. RECOMMENDED OPERATING RANGES

Characteristic	Symbol	Min	Typ	Max	Unit
Battery Supply voltage	V_{BB}	+6		+29	V
Digital input/outputs voltage	V_{IO}	0		+5.5	V
Parametric operating junction temperature range (Note 12)	T_{jp}	−40		+145	°C
Functional operating junction temperature range (Note 13)	T_{jf}	−40		+160	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc. No more than 100 cumulated hours in life time above T_{tw}.
12. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.
13. The maximum functional operating temperature range can be limited by thermal shutdown T_{tsd}.

PACKAGE THERMAL CHARACTERISTIC

The NCV70516 is available in a thermally optimized SSOP24 and QFN24 5x5 packages. For the optimizations, the package has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

For precise thermal cooling calculations the major thermal resistances of the devices are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the device pins and exposed pad)

The major thermal resistances of the device are the Rth from the junction to the ambient (Rthja) and the Rth from the junction to the exposed pad (Rthjp).

Using an exposed die pad on the bottom surface of the package is mainly contributing to this performance. In order to take full advantage of the exposed pad, it is most important that the PCB has features to conduct heat away from the package. In the table below, one can find the values for the Rthja and Rthjp:

Table 5. THERMAL RESISTANCE

Package	Rth, Junction−to−Exposed Pad, Rthjp	Rth, Junction−to−Ambient, Rthja (Note 14)
SSOP24 NB EP	8.5 K/W	33.0 K/W
QFN24 5x5 0.65	5.9 K/W	32.2 K/W

14. The Rthja for 2S2P simulated for worst case power and following conditions:
    - A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
    - Board thickness is 1.46 mm (FR4 PCB material)
    - All four layers: 30 μm thick copper with an area of 2500 mm^2 where:
      - top signal layer has a conductivity of 40% = 64.5 W/mK
      - bottom signal layer has a conductivity of 90% = 355.5 W/mK
      - top plane has a conductivity of 70% = 276.5 W/mK
      - bottom plane has a conductivity of 90% = 355.5 W/mK
    - The 9 vias in Exposed Pad area, via diameter 0.45 mm for SSOP24 NB EP package
    - The 16 vias in Exposed Pad area, via diameter 0.25 mm for QFN24 5x5 package
    - Gap*filler max 400 μm between PCB and heat sink non conductive with worst case thermal conductivity of 1.5 W/mK

EQUIVALENT SCHEMATICS

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

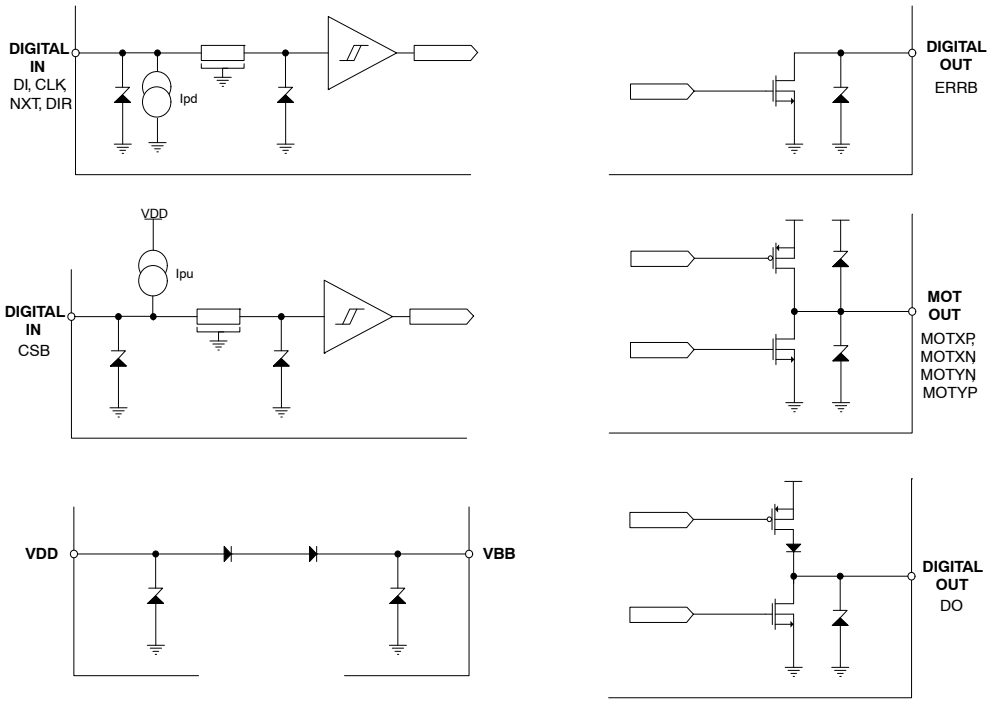


Figure 5. Input and Output Equivalent Diagrams

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

The DC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
MOTORDRIVER							
$I_{MS-max,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	V_{BB} = 14 V		800		mA
$I_{MS-boost,Peak}$		Max current during booster function	V_{BB} = 14 V, T_j = −45°C		1100		mA
I_{MSabs}		Absolute error on coil current	V_{BB} = 14 V, T_j = 145°C $I_{MSmax,Peak}$ = 800 mA and 100 mA	−10		10	%
I_{MSrel}		Matching of X & Y coil currents	V_{BB} = 14 V $I_{MSmax,Peak}$ = 800 mA and 100 mA	−7		7	%
$R_{DS(on)}$		On resistance of High side + Low side Driver at the highest current range	T_j = 145°C			2.4	Ω
LOGIC INPUTS							
V_{inL}	CSB	Logic low input level, max	T_j = 145°C			0.8	V
V_{inH}		Logic high input level, min	T_j = 145°C	2.4			V
I_{inL_pu}		Input pull up current for logic low level (Notes 15 and 16)	T_j = 145°C	−50	−25	−10	μA
I_{inH_pu}		Input leakage current for logic high level	T_j = 145°C			1	μA
V_{inL}	DI, CLK	Logic low input level, max	T_j = 145°C			0.8	V
V_{inH}		Logic high input level, min	T_j = 145°C	2.4			V
I_{inH_pd}		Input pull down current for logic high level (Note 16)	T_j = 145°C	1	2	5	μA
I_{inL_pd}		Input leakage current for logic low level	T_j = 145°C	−1			μA
V_{inL}	NXT, DIR	Logic low input level, max	T_j = 145°C			0.8	V
V_{inH}		Logic high input level, min	T_j = 145°C	2.4			V
I_{inH_pd}		Input pull down current for logic high level (Note 16)	T_j = 145°C	1	3	5	μA
I_{inL_pd}		Input leakage current for logic low level	T_j = 145°C	−1			μA
OPEN DRAIN LOGIC OUTPUT							
V_{OLmax}	ERRB	Output voltage	8 mA sink current			0.4	V
V_{OHmax}		Maximum drain voltage				5.5	V
I_{OLmax}		Maximum allowed drain current (Note 24)				12	mA

15. The CSB has a higher pull up current. It is expected that CSB is pulled high anyway in sleep mode, making this pull up current disappear.
16. All Pull−up and pull down currents stay activated during sleep to avoid floating input pins. Placing the pin in wrong state during sleep results in higher sleep currents in the application.
17. Thermal warning and low temperature level are derived from thermal shutdown ($T_{tw} = T_{tsd} - 20°C$, $T_{low} = T_{tsd} - 137°C$).
18. No more than 100 cumulated hours in life time above T_{tw}.
19. Parameter guaranteed by trimming relevant OTPs in production test at 160°C and VBB = 14 V.
20. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs.
21. All analog cells in power down. Logic powered, no clocks running. All outputs unloaded, no floating inputs.
22. Pin VDD must not be used for any external supply.
23. The SPI registers content will not be altered above this voltage.
24. Maximum allowed drain current that the output can withstand without getting damaged. Not tested in production.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
PUSH−PULL LOGIC OUTPUT WHEN CSB = 0 (Figure 5)							
V_{OLmax}	DO	Output voltage low	8 mA sink current			0.4	V
V_{OHmin}		Output voltage high without pull−up	4 mA source current	V_{DD} − 1.3			V
V_{OHmax}		Maximum pin voltage				5.5	V
I_{OLmax}		Maximum allowed pin current (Note 24)				12	mA
THERMAL WARNING & SHUTDOWN							
T_{tw}		Thermal warning (Notes 17 and 18)		135	145	155	°C
T_{tsd}		Thermal shutdown (Note 19)		155	165	175	°C
T_{low}		Low temperature level (Note17)		12	28	44	°C
SUPPLY AND VOLTAGE REGULATOR							
UV	V_{BB}	H−Bridge off voltage low threshold		5.7	6.0	6.3	V
$UV_{\_HYST}$		Under voltage hysteresis		100	250	600	mV
I_{bat}		Total current consumption (Note 20)	Unloaded outputs V_{BB} = 29 V		4	15	mA
I_{bat_s}		Sleep mode current consumption (Note 21)	V_{BB} = 5.5 V & 18 V	30	60	120	μA
V_{DD}	V_{DD}	Regulated internal supply (Note 22)	5.5 V < V_{BB} < 29 V Load = 0 mA, 15 mA	3.0	3.3	3.6	V
$V_{ddReset}$		Digital supply reset level @ power down (Note 23)				3.0	V
I_{ddLim}		Current limitation	Pin shorted to ground V_{BB} = 14 V			80	mA

15. The CSB has a higher pull up current. It is expected that CSB is pulled high anyway in sleep mode, making this pull up current disappear.
16. All Pull−up and pull down currents stay activated during sleep to avoid floating input pins. Placing the pin in wrong state during sleep results in higher sleep currents in the application.
17. Thermal warning and low temperature level are derived from thermal shutdown (T_{tw} = T_{tsd} − 20°C, T_{low} = T_{tsd} − 137°C).
18. No more than 100 cumulated hours in life time above T_{tw}.
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20. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs.
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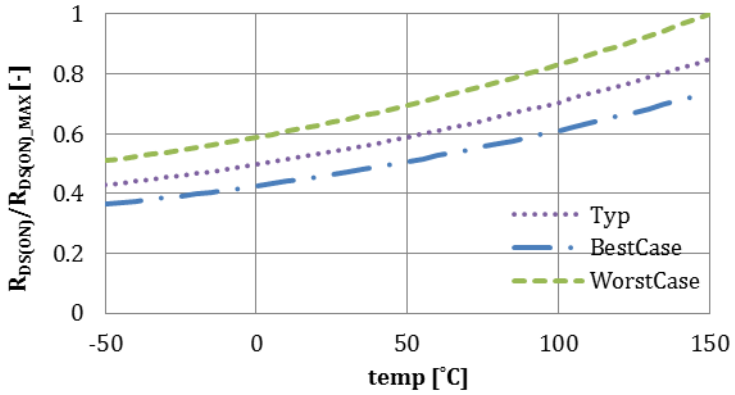


Figure 6. ON Resistance of High Side + Low Side Driver at the Highest Current Range

AC PARAMETERS

The AC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified.

Table 7. AC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL OSCILLATOR							
f_{osc}		Frequency of internal oscillator	V_{BB} = 14 V	9	10	11	MHz
MOTORDRIVER							
f_{pwm}	MOTxx	PWM frequency	(Note 25)		28.4		kHz
f_{jit_depth}		PWM jitter modulation depth	SPI bit PWMJen = 1 (Note 25)			20	%
t_{OCdet}		Open coil detection with PWM=100% (Note 25)	SPI bit OpenDet[1:0] = 00		5		ms
			SPI bit OpenDet [1:0] = 01		25		
			SPI bit OpenDet [1:0] = 10		50		
			SPI bit OpenDet [1:0] = 11		200		
t_{brise}		Turn−on transient time, between 10% and 90%, I_{MD} = 200 mA, V_{BB} = 14 V, 1 nF at motor pins			300		ns
t_{bfall}		Turn−off transient time, between 10% and 90%, I_{MD} = 200 mA, V_{BB} = 14 V, 1 nF at motor pins			300		ns
DIGITAL OUTPUTS							
t_{H2L}	DO, ERRB	Output fall−time (90% to 10%) from V_{InH} to V_{InL}	Capacitive load 200 pF and pull−up 1.5 kΩ			50	ns
HARD RESET FUNCTION							
t_{hr_trig}	DIR	Hard reset trigger time (Note 25)	See hard reset function	20			µs
t_{hr_dir}		Hard reset DIR pulse width	(Note 25)	2.5			µs
t_{hr_set}	NXT	NXT set−up time	(Note 25)	2.5			µs
t_{hr_err}	ERRB	Hard reset error indication	(Note 25)		50		µs
t_{csb_width}	CSB	CSB wake−up low pulse width	(Note 25)	2		150	µs
t_{wu}		Wake−up time	See Sleep Mode	250			µs
NXT/DIR INPUTS							
t_{NXT_HI}	NXT	NXT minimum, high pulse width		2			µs
t_{NXT_LO}		NXT minimum, low pulse width		2			µs
f_{NXT}		NXT max repetition rate				$f_{PWM}/2$	kHz
$t_{CSB\_LO\_WIDTH}$		NXT pin trigger after SPI NXT command		1			µs
t_{DIR_SET}	NXT, DIR	NXT set time, following change of DIR		25			µs
t_{DIR_HOLD}		NXT hold time, before change of DIR		25			µs

25. Derived from the internal oscillator

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. SPI INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB setup time (Note 26)	0.5			μs
t_{CSH}	CSB hold time	0.5			μs
t_{CS}	CSB high time	1			μs
t_{WL}	CLK low time	0.5			μs
t_{WH}	CLK high time	0.5			μs
t_{SU}	DI set up time, valid data before rising edge of CLK	0.25			μs
t_{H}	DI hold time, hold data after rising edge of CLK	0.275			μs
t_{CSDO}	CSB low to DO valid			0.23	μs
t_{DIS}	Output (DO) disable time (Note 27)	0.08		0.32	μs
$t_{V1\rightarrow0}$	Output (DO) valid (Note 27)			0.32	μs
$t_{V0\rightarrow1}$	Output (DO) valid (Note 28)			0.32 + t(RC)	μs

26. After leaving sleep mode an additional wait time of 250 μs is needed before pulling CSB low.
27. SDO low−side switch activation time.
28. Time depends on the SDO load and pull−up resistor.

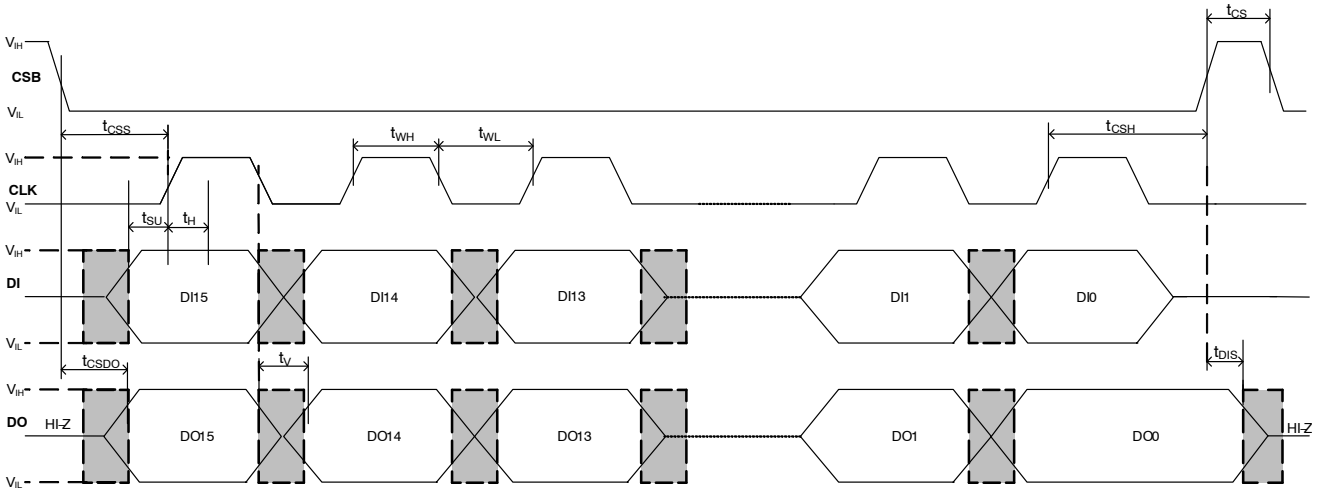


Figure 7. SPI Timing

DETAILED OPERATING DESCRIPTION

H−Bridge Drivers with PWM Control

Two H−bridges are integrated to drive a bipolar stepper motor. Each H−bridge consists of two low−side N−type MOSFET switches and two high−side P−type MOSFET switches. One PWM current control loop with on−chip current sensing is implemented for each H−bridge. Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted to maintain current−sense accuracy. A comparator compares continuously the actual winding current with the requested current and feeds back the information to generate a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock.

The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency. In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches.

A protection against shorts on motor lines is implemented. When excessive voltage is sensed across a MOSFET for a time longer than the required transition time, then the MOSFET is switched−off.

Motor Enable−Disable

The H−bridges and PWM control can be disabled (high−impedance state) by means of a bit <MOTEN> in the SPI control registers. <MOTEN>=0 will only disable the drivers and will not impact the functions of NXT, DIR, SPI bus, etc. The H−bridges will resume normal PWM operation by writing <MOTEN>=1 in the SPI register. PWM current control is then enabled again and will regulate current in both coils corresponding with the position given by the current translator.

Automatic Forward and Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. For transition to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

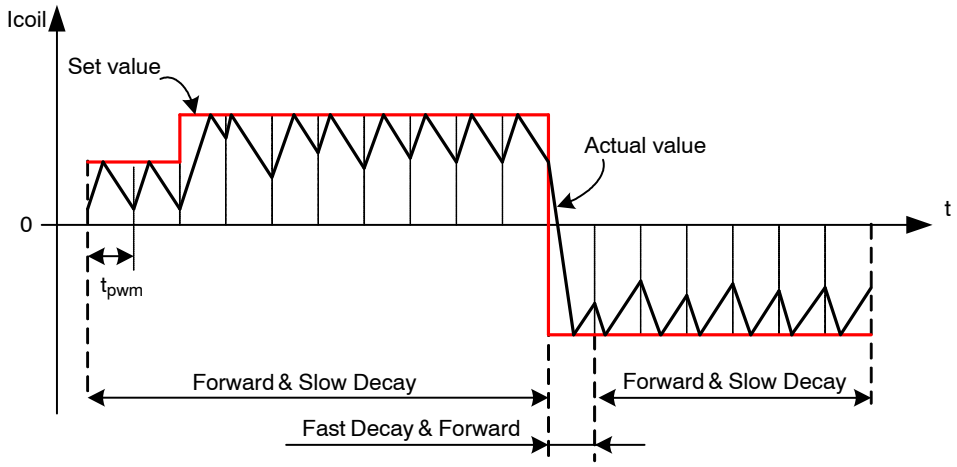


Figure 8. Forward and Slow/Fast Decay PWM

Automatic Duty Cycle Adaptation

If during regulation the set point current is not reached before 75% of t_{pwm}, the duty cycle of the PWM is adapted automatically to > 50% (top regulation) to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The state of the duty cycle adaptation mode is represented in the internal T/B bits for both motor windings X and Y. Figure 9 gives a representation of the duty cycle adaptation.

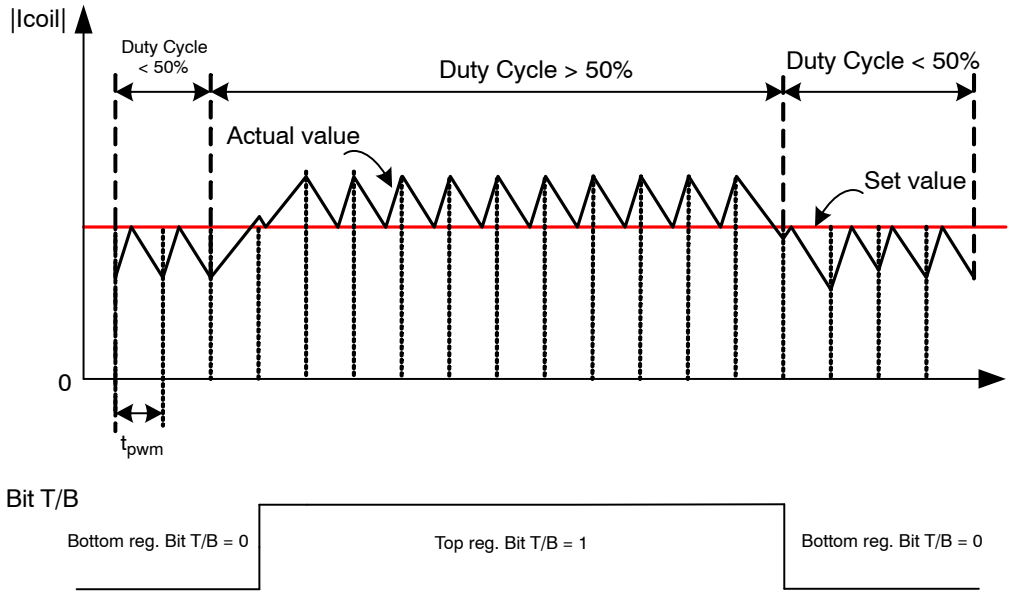


Figure 9. Automatic Duty Cycle Adaptation

Active Break

Whenever active break is activated (<ACTBR> bit is set), both bottom drivers of active H−bridge (based on actual MSP position) are switched on.

By this mean the position is frozen and current starts recirculating through the bottom drivers, causing faster stopping of the motor.

Step Translator

Step Mode

The step translator provides the control of the motor by means of step mode SPI register SM[2:0], SPI bits DIRP, NXTP and input pins DIR (direction of rotation) and NXT (next pulse). It is translating consecutive steps into corresponding currents in both motor coils for a given step mode.

One out of five possible stepping modes can be selected through SPI−bits SM[2:0]. After power−on or hard reset, the coil−current translator is set to the default to 1/16 micro−stepping at position '**8***'. When remaining in the default step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 9 lists the output current versus the translator position.

When the micro−step resolution is reduced, then the corresponding least−significant bits of the translator position are set to "0". This means that the position in the current table moves to the right and in the case that micro−step position of desired new resolution does not overlap the micro−step position of current resolution, the closest value up or down in required column is set depending on the direction of rotation.

When the micro−step resolution is increased, then the corresponding least−significant bits of the translator position are added as "0": the micro−step position moves to the left on the same row.

In general any change of <SM[2:0]> SPI bits have no effect on current micro−step position without consequent occurrence of NXT pulse or <NXTP> SPI command (see NXT input timing below). When NXT pulse or <NXTP> SPI command arrives, the motor moves into next micro−step position according to the current <SM[2:0]> SPI bits value.

Besides the micro−step modes, also full step mode is implemented. Full step mode activates always only one coil at a time.

Table 9. TRANSLATOR TABLE

MSP[5:0]	Step mode SM[2:0]					% of Imax		MSP[5:0]	Step mode SM[2:0]					% of Imax	
	000	001	010	011	100				000	001	010	011	100		
MSP[5:0]	1/16	1/8	1/4	1/2	FS	Coil Y	Coil X	MSP[5:0]	1/16	1/8	1/4	1/2	FS	Coil Y	Coil X
00 0000	0	0	0	0	0	0	100	**10 0000**	32	16	8	4	2	0	−100
00 0001	1	–	–	–	–	9,8	99,5	**10 0001**	33	–	–	–	–	−9,8	−99,5
00 0010	2	1	–	–	–	19,5	98,1	**10 0010**	34	17	–	–	–	−19,5	−98,1
00 0011	3	–	–	–	–	29	95,7	**10 0011**	35	–	–	–	–	−29	−95,7
00 0100	4	2	1	–	–	38,3	92,4	**10 0100**	36	18	9	–	–	−38,3	−92,4
00 0101	5	–	–	–	–	47,1	88,2	**10 0101**	37	–	–	–	–	−47,1	−88,2
00 0110	6	3	–	–	–	55,6	83,1	**10 0110**	38	19	–	–	–	−55,6	−83,1
00 0111	7	–	–	–	–	63,4	77,3	**10 0111**	39	–	–	–	–	−63,4	−77,3
00 1000	**8(*)**	4	2	1	–	70,7	70,7	**10 1000**	40	20	10	5	–	−70,7	−70,7
00 1001	9	–	–	–	–	77,3	63,4	**10 1001**	41	–	–	–	–	−77,3	−63,4
00 1010	10	5	–	–	–	83,1	55,6	**10 1010**	42	21	–	–	–	−83,1	−55,6
00 1011	11	–	–	–	–	88,2	47,1	**10 1011**	43	–	–	–	–	−88,2	−47,1
00 1100	12	6	3	–	–	92,4	38,3	**10 1100**	44	22	11	–	–	−92,4	−38,3
00 1101	13	–	–	–	–	95,7	29	**10 1101**	45	–	–	–	–	−95,7	−29
00 1110	14	7	–	–	–	98,1	19,5	**10 1110**	46	23	–	–	–	−98,1	−19,5
00 1111	15	–	–	–	–	99,5	9,8	**10 1111**	47	–	–	–	–	−99,5	−9,8
01 0000	16	8	4	2	1	100	0	**11 0000**	48	24	12	6	3	−100	0
01 0001	17	–	–	–	–	99,5	−9,8	**11 0001**	49	–	–	–	–	−99,5	9,8
01 0010	18	9	–	–	–	98,1	−19,5	**11 0010**	50	25	–	–	–	−98,1	19,5
01 0011	19	–	–	–	–	95,7	−29	**11 0011**	51	–	–	–	–	−95,7	29
01 0100	20	10	5	–	–	92,4	−38,3	**11 0100**	52	26	13	–	–	−92,4	38,3
01 0101	21	–	–	–	–	88,2	−47,1	**11 0101**	53	–	–	–	–	−88,2	47,1
01 0110	22	11	–	–	–	83,1	−55,6	**11 0110**	54	27	–	–	–	−83,1	55,6
01 0111	23	–	–	–	–	77,3	−63,4	**11 0111**	55	–	–	–	–	−77,3	63,4
01 1000	24	12	6	3	–	70,7	−70,7	**11 1000**	56	28	14	7	–	−70,7	70,7
01 1001	25	–	–	–	–	63,4	−77,3	**11 1001**	57	–	–	–	–	−63,4	77,3
01 1010	26	13	–	–	–	55,6	−83,1	**11 1010**	58	29	–	–	–	−55,6	83,1
01 1011	27	–	–	–	–	47,1	−88,2	**11 1011**	59	–	–	–	–	−47,1	88,2
01 1100	28	14	7	–	–	38,3	−92,4	**11 1100**	60	30	15	–	–	−38,3	92,4
01 1101	29	–	–	–	–	29	−95,7	**11 1101**	61	–	–	–	–	−29	95,7
01 1110	30	15	–	–	–	19,5	−98,1	**11 1110**	62	31	–	–	–	−19,5	98,1
01 1111	31	–	–	–	–	9,8	−99,5	**11 1111**	63	–	–	–	–	−9,8	99,5

*Default position after reset of the translator position.

Translator Position

The translator position can be read and set by the SPI register <MSP[5:0]>. This is a 6−bit number equivalent to the 1/16th micro−step from Table 9: Translator Table. The translator position is updated immediately following a next micro−step trigger (see below).

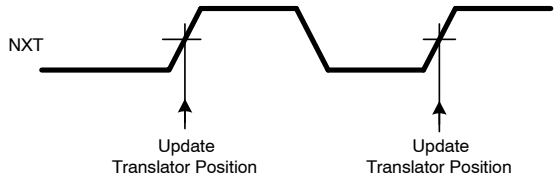


Figure 10. Translator Position Timing Diagram

Direction

The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP> (SPI register). The polarity bit <DIRP> allows changing the direction of rotation by means of only SPI commands instead of the dedicated input pin.

Direction = DIR−pin EXOR <DIRP>

Positive direction of rotation means counter−clockwise rotation of electrical vector Ix + Iy. Also when the motor is disabled (<MOTEN>=0), both the DIR pin and <DIRP> will have an effect on the positioner. The logic state of the DIR pin is visible as a flag in SPI status register.

Next Micro−Step Trigger

Positive edges on the NXT input − or activation of the “NXT pushbutton” <NXTP> in the SPI input register − will move the motor current one step up/down in the translator table. The <NXTP> bit in SPI is used to move positioner one (micro−)step by means of only SPI commands. If the bit is set to “1”, it is reset automatically to “0” after having advanced the positioner with one micro−step.

Trigger “Next micro−step” = (positive edge on NXT−pin) OR (<NXTP>=1)

- Also when the motor is disabled (<MOTEN>=0), NXT/DIR functions will move the positioner according to the logic.
- In order to be sure that both the NXT pin and the <NXTP> SPI command are individually attended, the following non overlapping zone has to be respected. In this case it is guaranteed that both triggers will have effect (2 steps are taken).

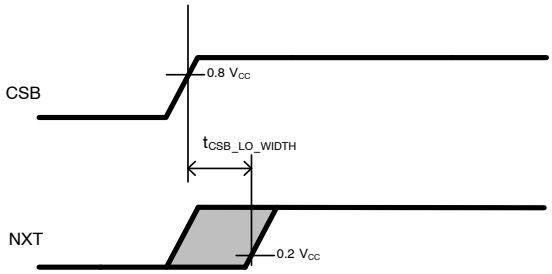


Figure 11. NXT Input Non Overlapping Zone with the <NXTP> SPI Command

For control by means of I/O’s, the NXT pin operation with respect to DIR pin should be in a non−overlapped way. See also the timing diagram below (refer to the AC table for the timing values). The <SM[2:0]> SPI bits setting, when changed, is accepted upon the consequent either NXT pin rising edge or <NXTP> SPI command write only. On the other hand, the SPI bits <DIRP>, <SM[2:0]> and <NXTP> can change state at the same time in the same SPI command: the next micro−step will be applied with the new settings. Writing to the SPI register <MSP[5:0]> is accepted and applied to translator table immediately, does not taking actual step mode into account.

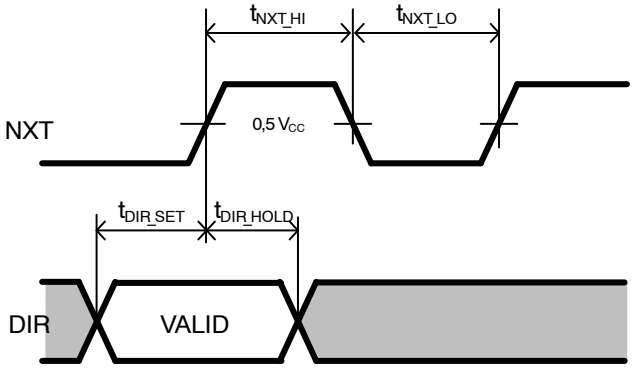


Figure 12. NXT input Timing Diagram

Motor Current

On cold temperatures below T_{low} (see Table 6 − DC Parameters) the current can be boosted to higher values by SPI bit <IBOOST>. After reaching temperature of thermal warning T_{tw}, current is automatically decreased to unboosted level. Status of the boost function can be read in SPI <IBOOST> bit. The motor current settings correspond to the following current levels:

Table 10. IMOT VALUES (4BIT)

Register Value	Peak Motor Current IMOT (mA)	Peak Boost Motor Current IMOT (mA)
0	59	81
1	71	98
2	84	116
3	100	138
4	119	164
5	141	194
6	168	231
7	200	275
8	238	327
9	283	389
A	336	462
B	400	550
C	476	655
D	566	778
E	673	925
F	800	1100

Whenever <IMOT[3:0]> is changed, the new coil currents will be updated immediately at the next PWM period.

In case the motor is disabled (<MOTEN>=0), the logic is functional and will have effect on NXT/DIR operation (not on the H−bridges). When the chip is in sleep mode, the logic is not functional and as a result, the NXT pin and DIR pin will have no effect.

Note: The hard−reset function is embedded by means of a special sequence on the DIR pin and NXT pin, see also Hard−Reset Function chapter.

Under−voltage Detection

The NCV70516 has one undervoltage threshold level UV (see Table 6 − DC Parameters).

UV level has its own flag readable via SPI. When supply voltage VBB drops under undervoltage level, this flag is set and ERRB pin is pulled down.

Only if the <UV>=0 the motor can be enabled again by writing <MOTEN>=1 in the control register.

Note: When Next pulse is applied (by means of NXT pin or <NXTP> bit via SPI) during undervoltage condition, the step loss bit <SL> is set.

Warning, Error Detection and Diagnostics Feedback

Open & Short Circuit Diagnostic

The NCV70516 stepper driver features an enhanced diagnostic detection and feedback, to be read by the external microcontroller unit (MCU). Among the main items of interest for the application and typical failures, are open coil and the short circuit condition, which may be to ground (chassis), or to supply (battery line).

When in normal mode, the device will continuously check upon errors with respect to the expected behavior.

The open load condition is determined by the fact that the PWM duty cycle keeps 100% value for a time longer than set by <OpenDet[1:0]> register. This is valid of course only for the X/Y coil where the current is supposed to circulate, meaning that in full step positions (MSP[5:0] = {0; 16; 32; 48} (dec)) the open load can be detected only for one of the coil at a time (respectively {X; Y; X; Y}). The same reasoning applies for the short circuits detection.

Due to the timeout value set by <OpenDet[1:0]>, the open coil detection is dependent on the motor speed. In more detail, there is a maximum speed at which it can be done. Table 11 specifies these maxima for the different step modes. For practical reasons, all values are given in full steps per second.

Table 11. MAXIMUM VELOCITIES FOR OPEN COIL DETECTION

Step Mode	Speed [FS/s] for given <OpenDet[1:0]>			
	00	01	10	11
Full Step	200	40	20	5
1/2	300	60	30	7.5
1/4	350	70	35	8.8
1/8	375	75	37.5	9.4
1/16	387.5	77.5	38.8	9.7

When Open coil condition is detected, the appropriate bit (<OPENX> or <OPENY>) together with <ELDEF> bit in the SPI status register are set. Reaction of the H−bridge to Open coil condition depends on the settings of <OpenHiZ> and <OpenDis> bits.

When both <OpenHiZ> and <OpenDis> bits are 0, <MOTEN> bit stays in 1 and only H−bridge where open coil is detected is disabled. When <OpenHiZ> bit is set, both H−bridges are disabled (<MOTEN>=0) in case of Open coil detection. When <OpenDis> bit is set, drivers remain active for both coils independently of <OpenHiZ> bit.

The short circuit detection monitors the load current in each activated output stage. The current is measured in terms of voltage drop over the MOSFETS' $R_{DS(ON)}$. If the load current exceeds the over−current detection threshold, the appropriate over−current flag <SHRTij> together with <ELDEF> bit are set and the drivers are switched off to protect the integrated circuit. Each driver stage has an individual detection bit for the N side and the P side.

When short circuit is detected, <MOTEN> is set to 0. The positioner, the NXT and DIR stay operational. The flag <ELDEF> (result of OR−ing the latched flags: <SHRTXPT> OR <SHRTXPB> OR <SHRTXNT> OR <SHRTYXNB> OR <SHRTYPT> OR <SHRTYPB> OR <SHRTYNT> OR <SHRTYNB> OR <OPENX> OR <OPENY>) is reset when the microcontroller reads out the short circuit or open coil status flags in status registers.

To enable the motor again after reading out of the status flags, <MOTEN>=1 has to be written.

Notes:

1. Successive reading of the <SHRTij> flags and re−enabling the motor in case of a short circuit condition may lead to damage of the drivers.
2. Example: SHRTXPT means: Short at X coil, Positive output pin, Top transistor.
3. In case of the short from any stepper motor pin to the top side during switching event from bottom to top on motor pin, the flag “short to bottom side” is set instead of the expected “short to top side” flag.

Step Loss Detection

When Next pulse is applied (by means of NXT pin or <NXTP> bit via SPI) or <MSP> register is written during error condition, the step loss bit <SL> is set.

<SL> = (<UV> OR <TSD> OR <ELDEF>) AND ((NXT OR <NXTP>) OR <MSP> write)

Step loss bit <SL> is cleared after read out.

Thermal Warning and Shutdown

When junction temperature is above T_{tw}, the thermal warning bit <TW> is set (SPI register) and the ERRB pin is pulled down (*). If junction temperature increases above thermal shutdown level, then also the <TSD> flag is set, the ERRB pin is pulled down, the motor is disabled (<MOTEN> = 0) and the hardware reset is disabled. If $T_j < T_{tw}$ level and <TSD> bit has been read−out, the status of <TSD> is cleared and the ERRB pin is released.

Only if the <TSD>=<TW>=0, the motor can be enabled again by writing <MOTEN>=1 in the control register 1.

During the over temperature condition the hardware reset will not work until $T_j < T_{tw}$ and the <TSD> readout is done.

In this way it is guaranteed that after a <TSD>=1 event, the die−temperature decreases back to the level of <TW>.

After reaching temperature of thermal warning T_{tw}, motor current is automatically decreased to unboosted level.

Note (*): During the <TW> situation the motor is not disabled while the ERRB is pulled down. To be informed about other error situations it is recommended to poll the status registers on a regular base (time base driven by application software in the millisecond domain).

Error Output

This is an open drain output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = (<SPI> OR <ELDEF> OR <TSD> OR <TW> OR <UV> OR (*)reset state) AND not (**)sleep mode

Note (*) reset state: After a power−on or a hard−reset, the ERRB is pulled low during t_{hr_err} (Table 7 − AC Parameters).

Note (**) sleep mode: In sleep mode the ERRB is always inactive (high).

Sleep Mode

The motor driver can be put in a low−power consumption mode (sleep mode). The sleep mode is entered automatically after a power−on or hard reset and can also be activated by means of SPI bit <SLP>. In sleep−mode, all analog circuits are suspended in low−power. SPI communication stays active. The motor driver is disabled (even if <MOTEN>=1), the content of all registers is maintained (including <MOTEN>, <TSD> and <TW>), logic output pin ERRB is disabled (ERRB has no function) and none of the input pins is functional with the exception of pin CSB and SPI pins. Only CSB pin can wake−up the chip to normal mode (i.e. clear bit <SLP>) by means of a low pulse with a specified width within t_{csb_with} time. After wake−up, time t_{wu} (see AC Table) is needed to restore all analog and digital circuits.

Notes:

- The hard−reset function is disabled in sleep mode.
- The thermal shutdown function will be “frozen” during sleep mode and re−activated at wake−up. This is important in case that bit <TSD>=1 was cleared already and <TW> was not “0” yet.
- The CSB low pulse width has to be within t_{csb_with}, (see AC Table) to guarantee a correct wake−up.

Power−on Reset, Hard−Reset Function

After a power−on or a hard−reset, a flag <HR> in the SPI status register is set and the ERRB is pulled low. The ERRB stays low during this reset state. The typical power−on reset time is given by t_{hr_err} (Table 7 − AC Parameters). After the reset state the device enters sleep mode and the ERRB pin goes high to indicate the motor controller is ready for operation.

By means of a specific pattern on the DIR pin and NXT pin, the complete digital part of driver can be reset without a power−cycle. This hard−reset function is activated when the input pin DIR changes logic state “0 → 1 → 0 → 1” in five consecutive patterns during NXT pin being at high level. See figure below and Table 7 − AC Parameters.

The operation of all analog circuits is suspended during the reset state of the digital. Similar as for a normal power−on, the flag <HR> is set in the SPI register after a hard−reset and the ERRB pin is pulled low during t_{hr_err} (Table 7 − AC Parameters).

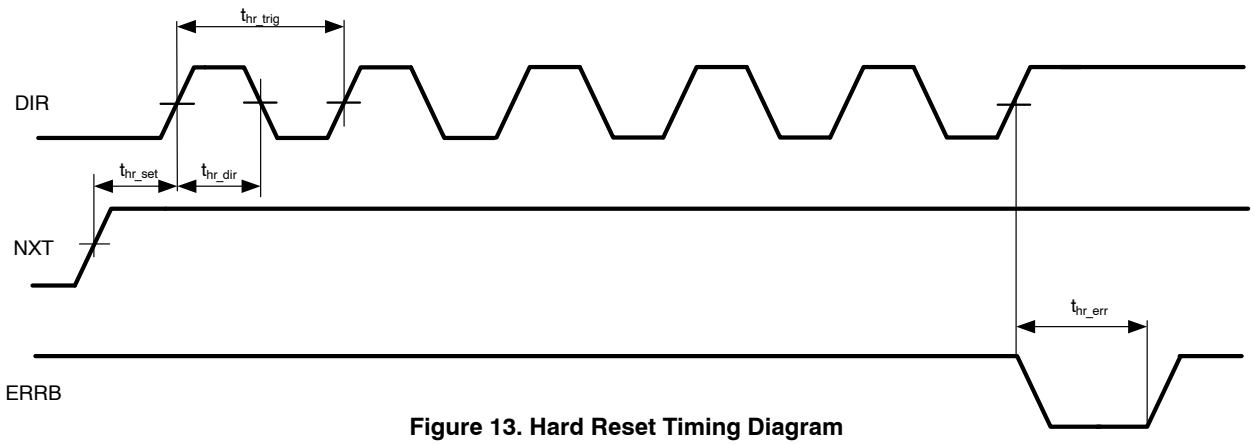


Figure 13. Hard Reset Timing Diagram

SPI INTERFACE

General

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV70516 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The NCV70516 SPI transfer size is 16 bits.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines: DO and DI. The DO signal is the output from the Slave (NCV70516), and the DI signal is the output from the Master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple−slave system.

The CSB line is active low. If an NCV70516 is not selected, DO is in high impedance state and it does not interfere with SPI bus activities. Since the NCV70516 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

The implemented SPI allows connection to multiple slaves by means of star connection (CSB per slave) or by means of daisy chain.

An SPI star connection requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 16 bits per communication.

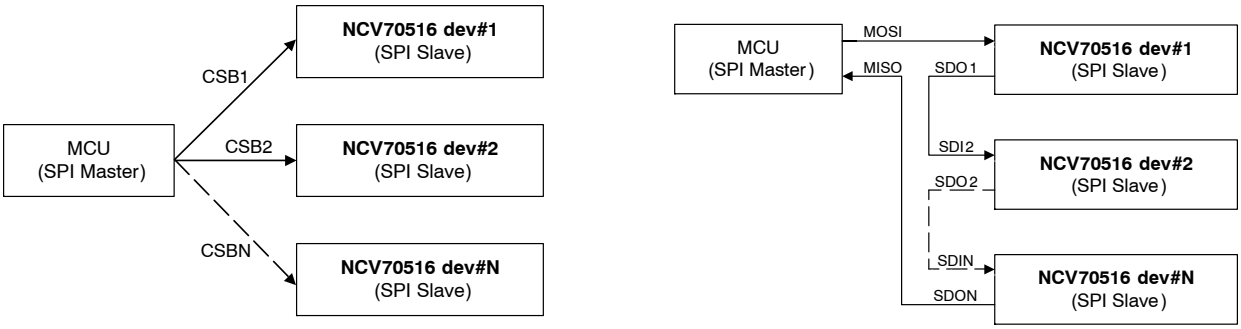


Figure 14. SPI Star vs. Daisy Chain Connection

SPI Daisy chain mode

SPI daisy chain connection bus width is always four lines independently on the number of slaves. However, the SPI transfer frame length will be a multiple of the base frame length so N x 16 bits per communication: the data will be interpreted and read in by the devices at the moment the CSB rises.

A diagram showing the data transfer between devices in daisy chain connection is given further: CMDx represents the 16−bit command frame on the data input line transmitted by the Master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

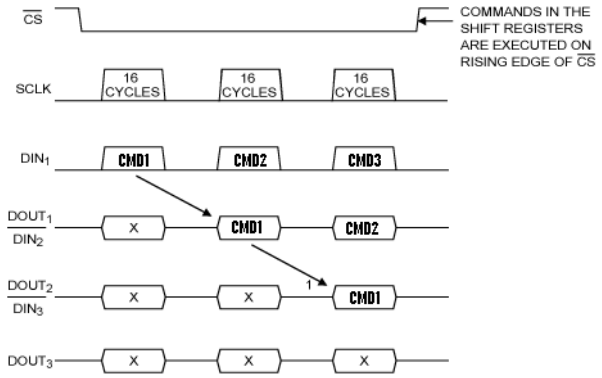


Figure 15. SPI Daisy Chain Data Shift Between Slaves. The symbol 'x' represents the previous content of the SPI shift register buffer.

The NCV70516 default power up communication mode is "star". In order to enable daisy chain mode, a multiple of 16 bits clock cycles must be sent to the devices, while the SDI line is left to zero.

Note: to come back to star mode the NOP register (address 0x0000) must be written with all ones, with the proper data parity bit and parity framing bit: see SPI protocol for details about parity and write operation.

SPI Transfer Format

Two types of SPI commands (to DI pin of NCV70516) from the micro controller can be distinguished: "Write to a control register" and "Read from register (control or status)".

The frame protocol for the *write operation*:

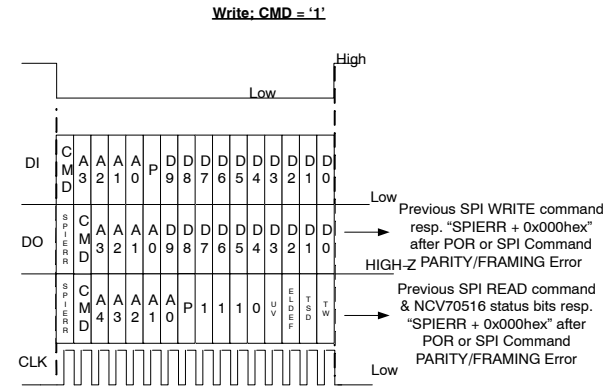


Figure 16. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the DI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 1 for write operation,
- Bits[14:11]: 4 bits WRITE ADDRESS field,
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame,
- Bits[9:0]: 10 bit DATA to write

Device in the same time replies to the master (on the DO):

- If the previous command was a write and no SPI error had occurred, a copy of the command, address and data written fields,
- If the previous command was a read, the response frame summarizes the address used and an overall diagnostic check (copy of the main detected errors, see Figure and Figure for details),
- In case of previous SPI error or after power−on−reset, only the MSB bit will be 1, followed by zeros.

If parity bit in the frame is wrong, device will not perform command and <SPI> flag will be set.

The frame protocol for the *read operation*:

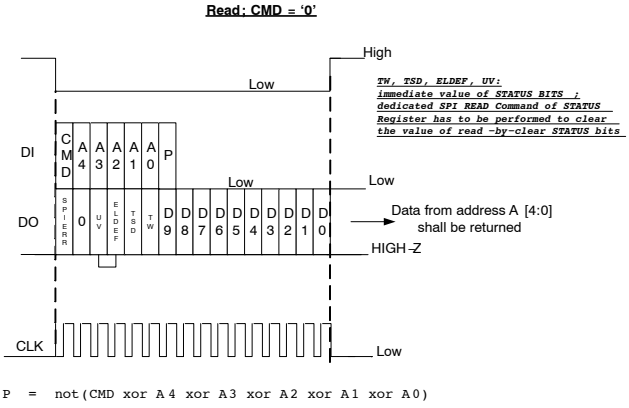


Figure 17. SPI Read Frame

Referring to the previous picture, the read frame coming from the master (into the DI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 0 for read operation,
- Bits[14:10]: 5 bits READ ADDRESS field,
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame,
- Bits [8:0]: 9 bits zeroes field.

Device in the same frame provides to the master (on the DO) data from the required address (in frame response), thus achieving the lowest communication latency.

SPI Framing and Parity Error

SPI communication framing error is detected by the NCV70516 in the following situations:

- Not an integer multiple of 16 CLK pulses are received during the active−low CSB signal;
- LSB bits (8..0) of a read command are not all zero;
- SPI parity errors, either on write or read operation.

Once an SPI error occurs, the <SPI> flag can be reset only by reading the status register in which it is contained (using in the read frame the right communication parity bit). This request will reset the SPI error bit and release the ERRB pin (high).

SPI Control Registers (CR)

All SPI control registers have Read/Write access.

Table 12. SPI CONTROL REGISTERS (CR)

5−bit Address	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default after Res.
00h	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	00 0000 0000
01h (CR1)	NotUsed	NXTP	MOTEN	DIRP	IBOOST	ACTBR	IMOT3	IMOT2	IMOT1	IMOT0	00 0000 0000
02h (CR2)	NotUsed	PWMJen	OpenDet1	OpenDet0	OpenDis	OpenHiZ	SLP	SM2	SM1	SM0	00 1000 1000
03h (CR3)	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	00 0000 0000
04h (CR4)	NotUsed	NotUsed	NotUsed	NotUsed	MSP5	MSP4	MSP3	MSP2	MSP1	MSP0	00 0000 1000

Table 13. BIT DEFINITION

Symbol	MAP position	Description
NOP	Bits [9:0] – ADDR_0x00	NOP register (read/write operation ignored)
NXTP	Bit 8 – ADDR_0x01 (CR1)	Push button pin, generating next step in position table
MOTEN	Bit 7 – ADDR_0x01 (CR1)	Enables the H−bridges (motor activated)
DIRP	Bit 6 – ADDR_0x01 (CR1)	Polarity of DIR pin, which controls direction status; DIRP = 1 inverts the logic polarity of the DIR pin)
IBOOST	Bit 5 – ADDR_0x01 (CR1)	Current boost function activation and status
ACTBR	Bit 4 – ADDR_0x01 (CR1)	Active break
IMOT[3:0]	Bits [3:0] – ADDR_0x01 (CR1)	Current amplitude
PWMJen	Bit 8 – ADDR_0x02 (CR2)	Enable PWM jittering function to spread spectrum of PWM modulation
OpenDet[1:0]	Bits [7:6] – ADDR_0x02 (CR2)	Open Coil detection time setting bits (see Table 7 – AC Parameters)
OpenDis	Bit 5 – ADDR_0x02 (CR2)	When bit is set, Open Coil detection status is flagged, but drivers control remain active for both coils, <OpenDis> bit setting has higher priority than <OpenHiZ> bit
OpenHiZ	Bit 4 – ADDR_0x02 (CR2)	When bit is set, during Open Coil detection both drivers are deactivated (MOTEN=0)
SLP	Bit 3 – ADDR_0x02 (CR2)	Places device in sleep mode with low current consumption (when 1)
SM[2:0]	Bits [2:0] – ADDR_0x02 (CR2)	Step mode selection
MSP[5:0]	Bit [5:0] – ADDR_0x04 (CR4)	Setting or status of translator micro−step position

SPI Status Registers (SR)

All SPI status registers have Read Only Access, with the odd parity on Bit8. Parity bit makes the numbers of 1 in the byte odd.

Table 14. SPI STATUS REGISTERS (SR)

5−bit Address	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default after Res.
05h (SR1)	0x0	PAR	SL, L	SPI,L	ELDEF, R*	TAMB, R	TSD,L	TW,R	UV, L	0x0	
06h (SR2)	0x0	PAR	0x0	0x0	HR,L	OPENX,L	SHRTXPB,L	SHRTXNB,L	SHRTXPT,L	SHRTXNT,L	
07h (SR3)	0x0	PAR	0x0	NXTpin, R	DIRpin, R	OPENY,L	SHRTYPB,L	SHRTYNB,L	SHRTYPT,L	SHRTYNT,L	
08h (SR4)	0x0	PAR	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0	REVID2	REVID1	REVID0	

Flags have ",L" for latched information or ",R" for real time information. All latched flags are "cleared upon read".
X = value after reset is defined during reset phase (diagnostics)
R* = real time read out of values of other latches. Reading out this R* value does not reset the bit, and does not reset the values of the latches this bit reads out.

Table 15. BIT DEFINITION

Symbol	MAP Position	Description
PAR	Bit 8 – ADDR_0x05 (SR1)	Parity bit for SR1
SL	Bit 7 – ADDR_0x05 (SR1)	Step loss register
SPI	Bit 6 – ADDR_0x05 (SR1)	SPI error: no multiple of 16 rising clock edges between falling and rising edge of CSB line
ELDEF	Bit 5 – ADDR_0x05 (SR1)	Eletrical defect: Short circuit was detected (at least one of the SHORTij individual bits is set) or Open Coil X or Y was detected
TAMB	Bit 4 – ADDR_0x05 (SR1)	Temperature below T_{low} level − Iboost function can be activated
TSD	Bit 3 – ADDR_0x05 (SR1)	Thermal shutdown
TW	Bit 2 – ADDR_0x05 (SR1)	Thermal warning
UV	Bit 1 – ADDR_0x05 (SR1)	Under voltage detection
PAR	Bit 8 – ADDR_0x06 (SR2)	Parity bit for SR2
HR	Bit 0 – ADDR_0x05 (SR1)	Hard reset flag: 1 indicates a hard reset has occurred
OPENX	Bit 4 – ADDR_0x06 (SR2)	Open Coil X detected
SHRTXPB	Bit 3 – ADDR_0x06 (SR2)	Short circuit detected at XP pin towards ground (Bottom)
SHRTXNB	Bit 2 – ADDR_0x06 (SR2)	Short circuit detected at XN pin towards ground (Bottom)
SHRTXPT	Bit 1 – ADDR_0x06 (SR2)	Short circuit detected at XP pin towards supply (Top)
SHRTXNT	Bit 0 – ADDR_0x06 (SR2)	Short circuit detected at XN pin towards supply (Top)
PAR	Bit 8 – ADDR_0x07 (SR3)	Parity bit for SR3
NXTpin	Bit 6 – ADDR_0x07 (SR3)	Read out of NXT pin logic status
DIRpin	Bit 5 – ADDR_0x07 (SR3)	Read out of DIR pin logic status
OPENY	Bit 4 – ADDR_0x07 (SR3)	Open Coil Y detected
SHRTYPB	Bit 3 – ADDR_0x07 (SR3)	Short circuit detected at YP pin towards ground (Bottom)
SHRTYNB	Bit 2 – ADDR_0x07 (SR3)	Short circuit detected at YN pin towards ground (Bottom)
SHRTYPT	Bit 1 – ADDR_0x07 (SR3)	Short circuit detected at YP pin towards supply (Top)
SHRTYNT	Bit 0 – ADDR_0x07 (SR3)	Short circuit detected at YN pin towards supply (Top)
PAR	Bit 8 – ADDR_0x08 (SR4)	Parity bit for SR4
DEVID[4:0]	Bits [7:3] – ADDR_0x08 (SR4)	Device ID
REVID[2:0]	Bits [2:0] – ADDR_0x08 (SR4)	Revision ID

For C516 device the DEVID [4:0] is $(16)_{dec}$. For N(V)70516−0 and N70516−1 versions the REVID[2:0] is $(1)_{dec}$.

APPLICATION EXAMPLES FOR MULTI−AXIS CONTROL

The wiring diagrams below show possible connections of multiple slaves to one microcontroller. In these examples, all movements of the motors are synchronized by means of a common NXT wire. The direction and Run/Hold activation is controlled by means of an SPI bus.

Further I/O reduction is accomplished in case the ERRB is not connected. This would mean that the microcontroller operates while polling the error flags of the slaves. Ultimately, one can operate multiple slaves by means of only 4 SPI connections: even the NXT pin can be avoided if the microcontroller operates the motors by means of the “NXTP” bit.

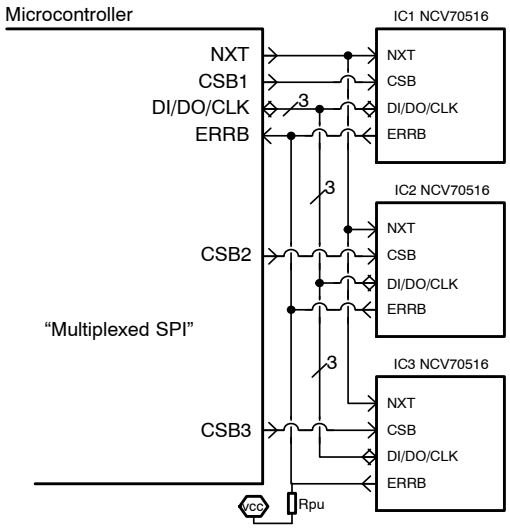


Figure 18. Examples of Wiring Diagrams for Multi−axis Control

ELECTRO MAGNETIC COMPATIBILITY

The NCV70516 has been developed using state−of−the−art design techniques for EMC. The overall system performance depends on multiple aspects of the system (IC design & lay−out, PCB design and layout...) of which some are not solely under control of the IC manufacturer. Therefore, meeting system EMC requirements can only happen in collaboration with all involved parties.

Special care has to be taken into account with long wiring to motors and inductors. A modern methodology to regulate the current in inductors and motor windings is based on controlling the motor voltage by PWM. This low frequency switching of the battery voltage is present at the wiring towards the motor or windings. To reduce possible radiated transmission, it is advised to use twisted pair cable and/or shielded cable.

ORDERING INFORMATION

Device	Peak Current	End Market/Version	Package*	Shipping†
NCV70516MW0R2G	800/1100 mA (Note 29)	Automotive High Temperature Version	QFN24 5x5 with wettable flank (Pb−Free)	5000 / Tape & Reel
NCV70516MW1BR2G			QFN24 5x5 non−wettable flank (Pb−Free)	5000 / Tape & Reel
NCV70516DQ0R2G			SSOP24 NB EP (Pb−Free)	3000 / Tape & Reel
NCV70516MW1AR2G**			QFNW24 5x5 with step−cut wettable flank (Pb−Free)	5000 / Tape & Reel

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

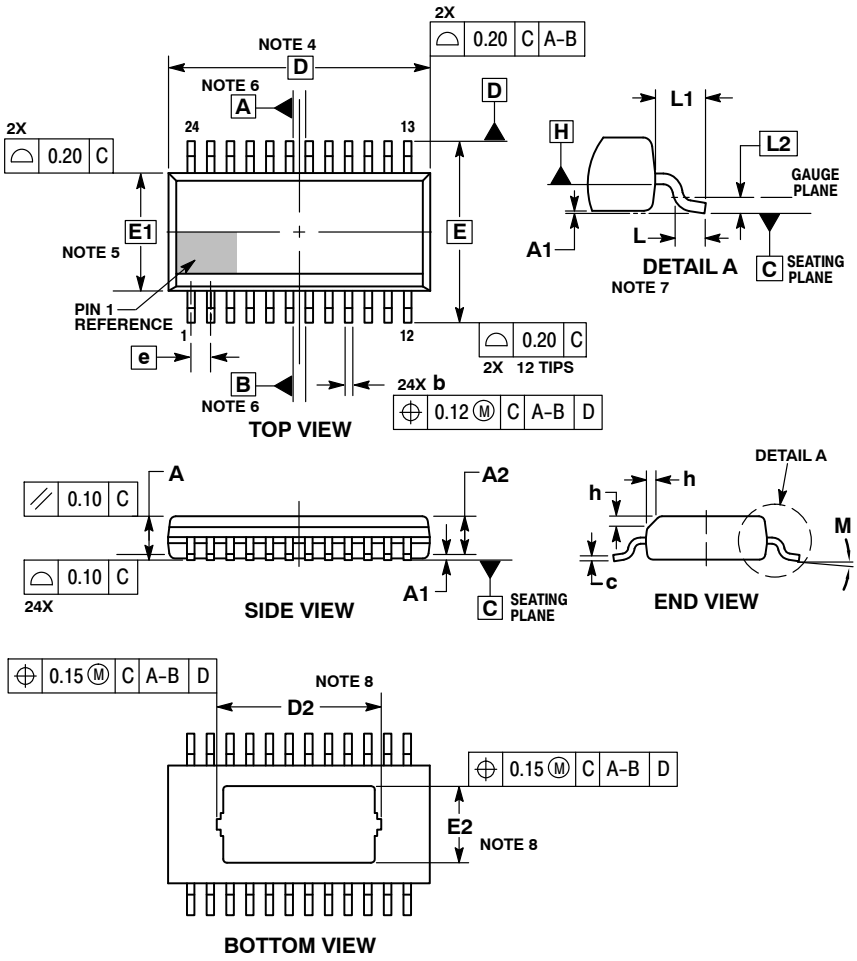
** NCV70516MW1AR2G is Dual Fab OPN. Please contact **onsemi** for technical details.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

29. The device boost current. This applies for operation under the thermal warning level only.

PACKAGE DIMENSIONS

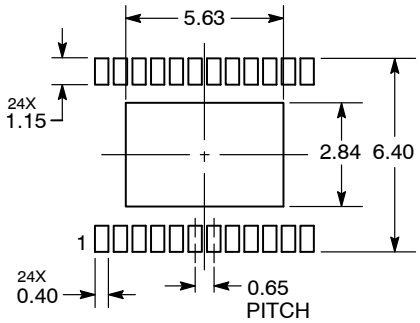
SSOP24 NB EP
CASE 940AK
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

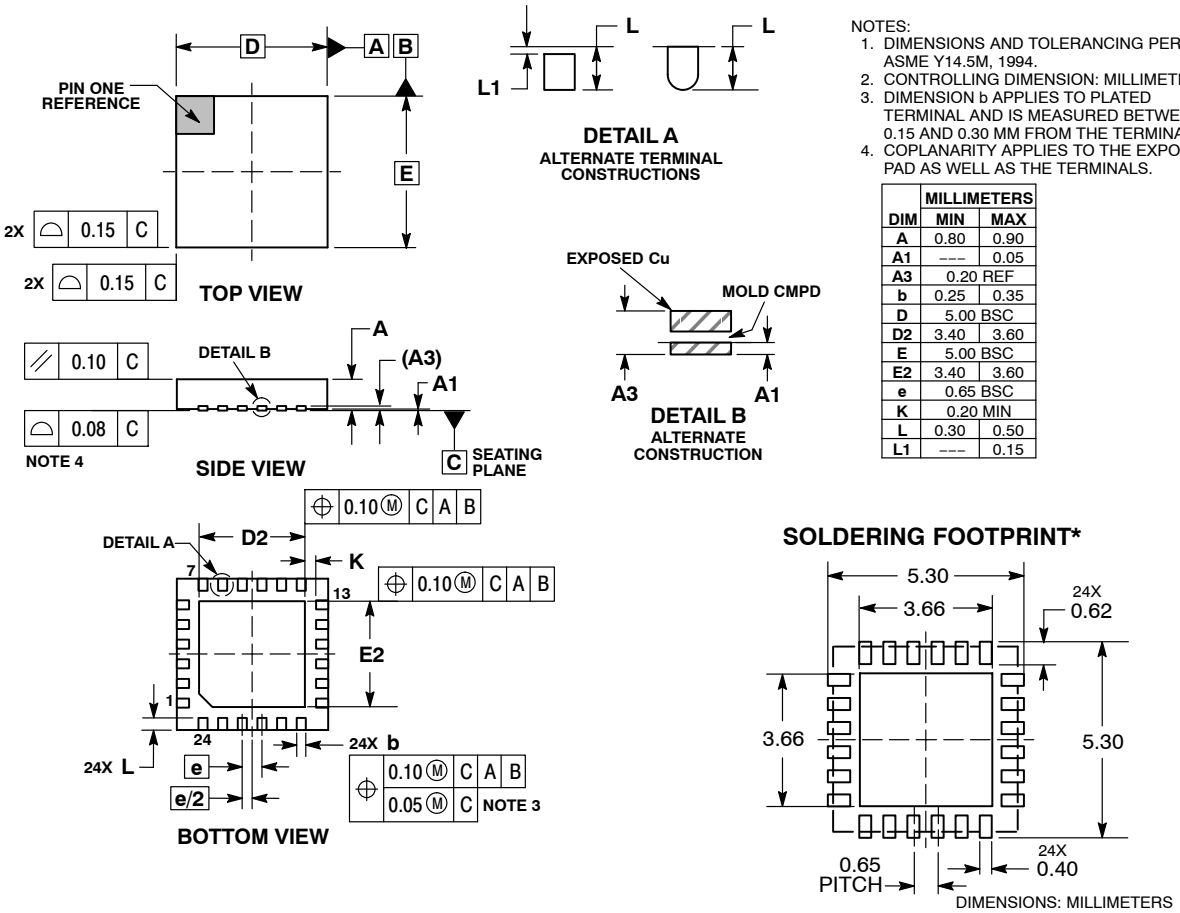
RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

QFN24 5x5, 0.65P
CASE 485CS
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	---	0.05
A3	0.20 REF	
b	0.25	0.35
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.65 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	---	0.15

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

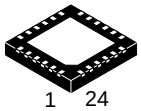
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

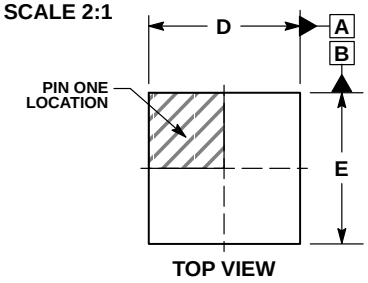
ON Semiconductor®

QFNW24 5x5, 0.65P
CASE 484AF
ISSUE A

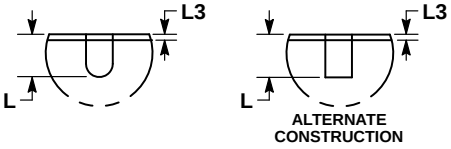
DATE 07 AUG 2018



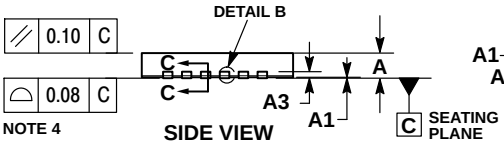
SCALE 2:1



TOP VIEW

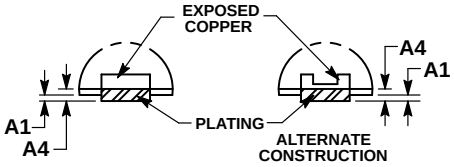


DETAIL A

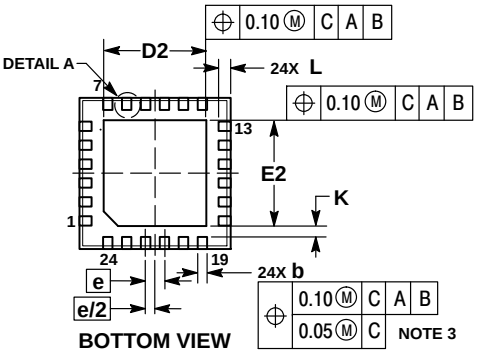


NOTE 4

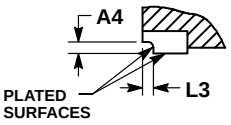
SIDE VIEW



DETAIL B



BOTTOM VIEW

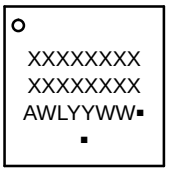


SECTION C−C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	–––	–––	0.05
A3		0.20 REF	
A4	0.10	–––	–––
b	0.25	0.30	0.35
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e		0.65 BSC	
K		0.35 REF	
L	0.30	0.40	0.50
L3		0.05 REF	

GENERIC MARKING DIAGRAM*

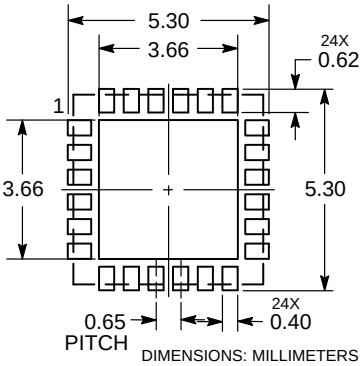


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	QFNW24 5x5, 0.65P	PAGE 1 OF 1

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