



N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a Q _g (Ty		
30	0.015 at V _{GS} = 10 V	12	16 nC	
	0.0175 at $V_{GS} = 4.5 \text{ V}$	12	10110	

FEATURES

- · Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] ChipFET[®] Package

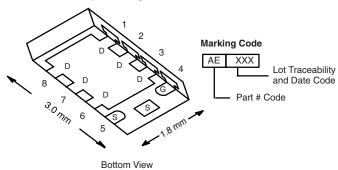


- Low On-Resistance
- Thin 0.8 mm Profile



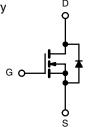
RoHS

PowerPAK ChipFET Single



APPLICATIONS

 Load Switch, PA Switch, and Battery for Portable Applications



N-Channel MOSFET

Ordering Information: Si5482DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25 ^{\circ}C$, unless Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30		
Gate-Source Voltage		V _{GS}	± 12	- V	
	T _C = 25 °C		12 ^a		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C		12 ^a		
Continuous Diam Current (1) = 130 C)	T _A = 25 °C	ID	11.1 ^{b, c}		
	T _A = 70 °C		8.8 ^{b, c}	А	
Pulsed Drain Current		I _{DM}	40		
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	12 ^a		
	T _A = 25 °C	I _S	2.6 ^{b, c}		
	T _C = 25 °C		31		
Maximum Power Dissipation	T _C = 70 °C	P _D	20	w	
	T _A = 25 °C	' b	3.1 ^{b, c}	7 "	
	T _A = 70 °C		2 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature		260	7 ~		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	34	40	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{th.IC}	3	4	C/VV	

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 90 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					I	I	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	30			٧	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	J 050 A		24.5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 4.3			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6		2	٧	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	ns	
Zero Gate Voltage Drain Current		V _{DS} = 30 V, V _{GS} = 0 V			1	1 10 μΑ	
	IDSS	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a		V _{GS} = 10 V, I _D = 7.4 A		0.0125	0.015	Ω	
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 6.8 \text{ A}$		0.0145	0.0175		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 7.4 A		35		S	
Dynamic ^b					L		
Input Capacitance	C _{iss}			1610		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		210			
Reverse Transfer Capacitance	C _{rss}			120			
Total Gate Charge	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 11.1 A		34	51	nC	
				16	24		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 11.1 \text{ A}$		3.6			
Gate-Drain Charge	Q _{gd}			3.7			
Gate Resistance	R_{g}	f = 1 MHz		5.1		Ω	
Turn-On Delay Time	t _{d(on)}			10	15	-	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.7 Ω		85	130		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 8.8 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		30	45		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			5	10	ns -	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.7 Ω		10	15		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 8.8$ A, V_{GEN} = 10 V, R_g = 1 Ω		35	55		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			12	A	
Pulse Diode Forward Current	I _{SM}				40	<u> </u>	
Body Diode Voltage	V _{SD}	I _S = 8.8 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			25	50	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 8.8 A, dl/dt = 100 A/μs, T _{.I} = 25 °C		18	27	nC	
Reverse Recovery Fall Time	t _a	$_{1F} = 0.0 \text{ A}$, $_{1J} = 25 \text{ C}$		14.5		20	
everse Recovery Rise Time t _b			10.5		ns		

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

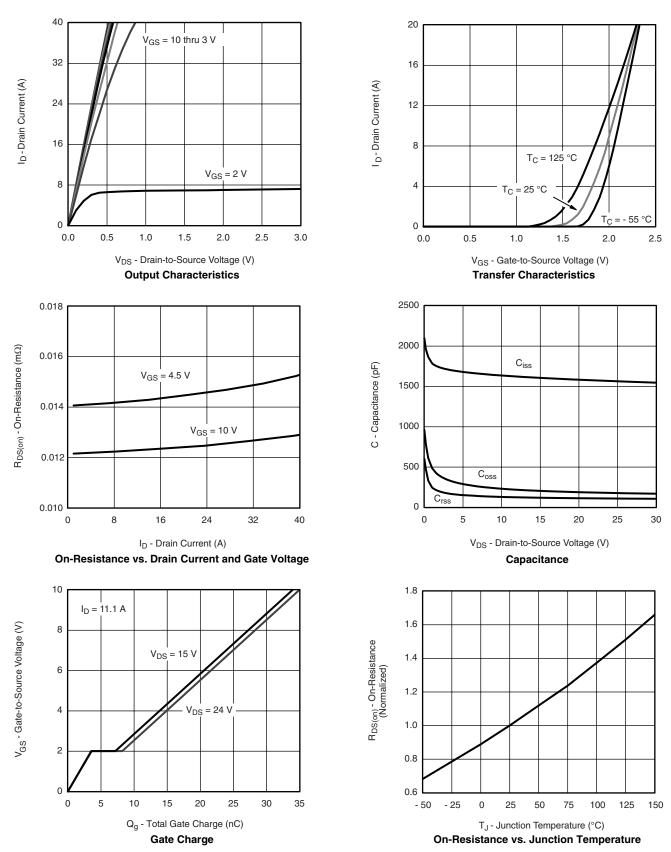
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







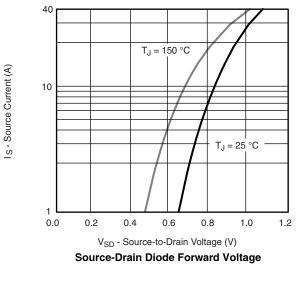
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

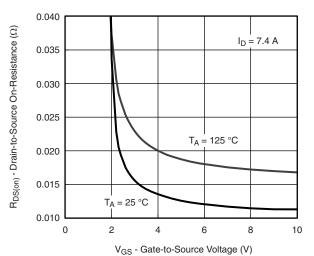


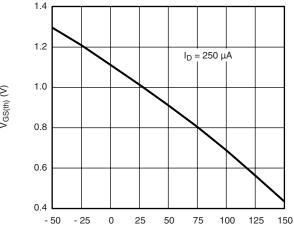
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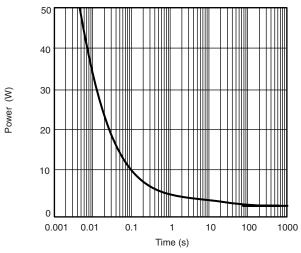
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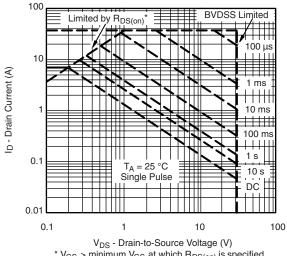
On-Resistance vs. Gate-to-Source Voltage



T_J - Temperature (°C)

Threshold Voltage





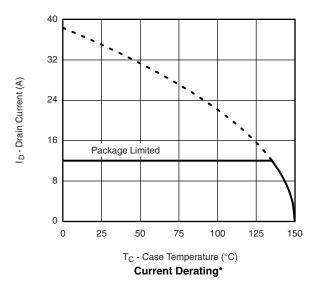
 V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified Safe Operating Area, Junction-to-Ambient

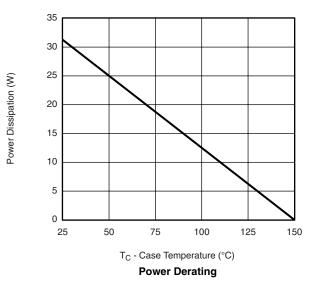






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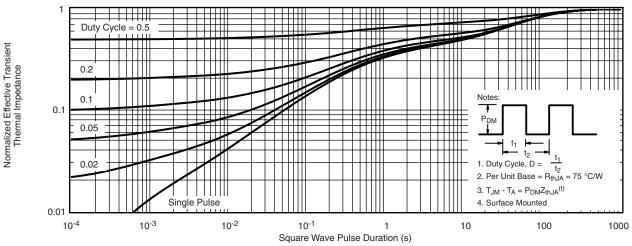
Document Number: 73594 S-81448-Rev. B, 23-Jun-08

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

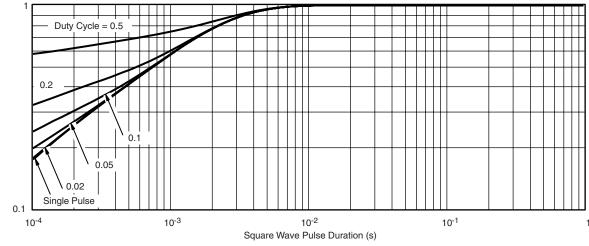
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73594.

Normalized Effective Transient Thermal Impedance



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