CHANGE NOTIFICATION

Linear Technology Corporation
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(408) 432-1900

February 06, 2015

Dear Sir/Madam: PCN# 020615

Subject: Notification of Change to LTC6091 Die and Datasheet

Please be advised that Linear Technology has made improvements to the ESD protection devices of the LTC6091. As these products now pass 4kV HBM ESD, the ESD Sensitivity Warning will be removed from page 2 of the data sheet. For informational purposes, CDM and MM ESD ratings are 1.0kV and 150V respectively. Also, internal resistor values were modified to simplify thermal shutdown functionality for single supply operation. The Thermal Shutdown application section of the datasheet will be modified to reflect this change as shown in attached mark-up pages of datasheet. This new revision silicon will ship with date codes 1514 and later. The data sheet specifications are unaffected by these changes.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@linear.com. If I do not hear from you by April 06, 2015, we will consider this change approved by your company.

Sincerely,

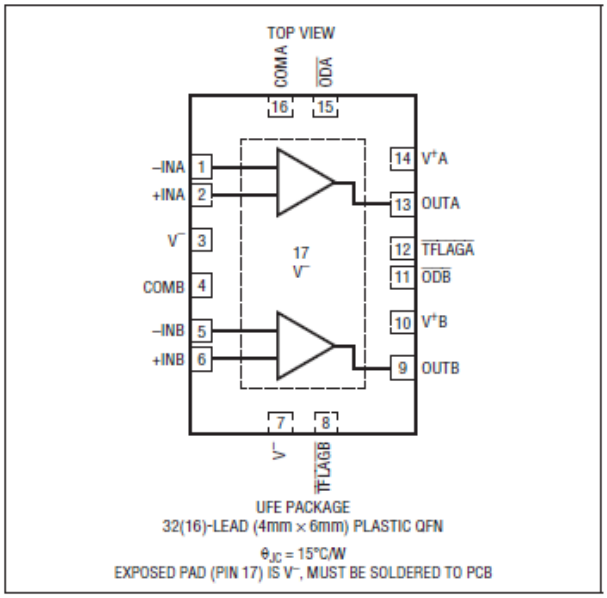
Jason Hu
Quality Assurance Engineer

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+A to V^-, or V^+B to V^-) 150V
COMA ..... V^- to V^+A
COMB ..... V^- to V^+B
Input Voltage
  $\overline{ODA}$ ..... V^- to V^+A + 0.3V
  $\overline{ODB}$ ..... V^- to V^+B + 0.3V
  +INA, –INA ..... V^- – 0.3V to V^+A + 0.3V
  +INB, –INB ..... V^- – 0.3V to V^+B + 0.3V
  $\overline{ODA}$ to COMA, $\overline{ODB}$ to COMB ..... –3V to 7V
Input Current
  +INA, –INA, +INB, -INB ..... ±10mA
$\overline{TFLAGA}$, $\overline{TFLAGB}$ Output
  $\overline{TFLAGA}$ ..... V^- – 0.3V to V^+A + 0.3V
  $\overline{TFLAGB}$ ..... V^- – 0.3V to V^+B + 0.3V
  $\overline{TFLAGA}$ to COMA ..... –3V to 7V
  $\overline{TFLAGB}$ to COMB ..... –3V to 7V
Continuous Output Current
  OUTA , OUTB (Note 2) ..... $50mA_{RMS}$
Operating Junction Temperature Range
  (Note 3) ..... –40°C to 125°C
Specified Junction Temperature Range (Note 4)
  LTC6091I ..... –40°C to 85°C
  LTC6091H ..... –40°C to 125°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10sec) ..... 300°C

PIN CONFIGURATION



UFE PACKAGE
32(16)-LEAD (4mm × 6mm) PLASTIC QFN

θ_{JC} = 15°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

~~ESD Sensitive: The output pins (OUTA and OUTB) are sensitve to ESD. Any ESD greater than 500V may cause permanent damage to the device.~~

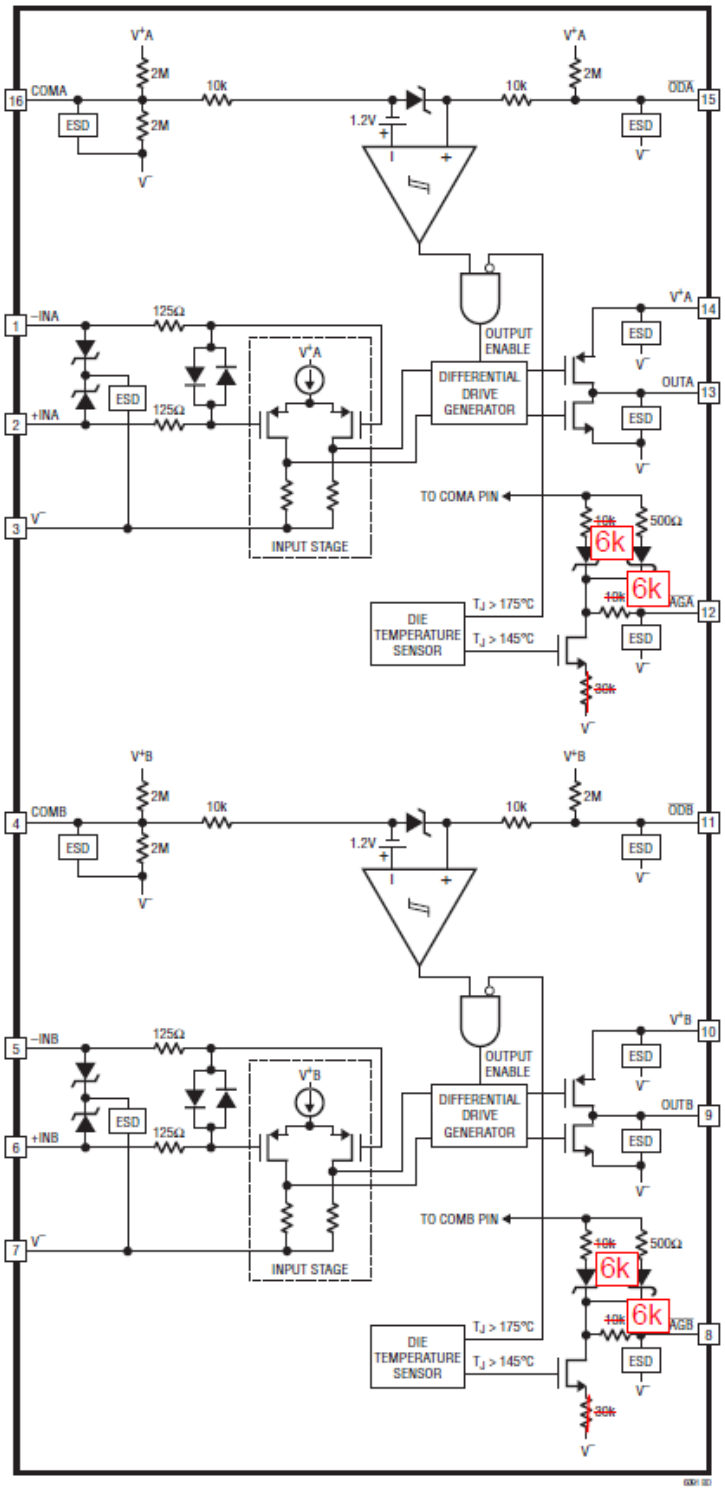
ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6091IUFE#PBF	LTC6091IUFE#TRPBF	6091	16-Lead Plastic QFN	–40°C to 85°C
LTC6091HUFE#PBF	LTC6091HUFE#TRPBF	6091	16-Lead Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

BLOCK DIAGRAM



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APPLICATIONS INFORMATION

General

The LTC6091 dual high voltage operational amplifier is designed in a Linear Technology proprietary CMOS process enabling a rail-to-rail output stage with a 140V supply while maintaining precision, low offset, low offset drift and low noise.

Power Supply

The LTC6091 consists of single monolithic die containing two LTC6090 amplifiers assembled in a single exposed-pad QFN package. Since both amplifiers share the same substrate, V^- pins (Pin 3 and Pin 7) must be tied together and to the exposed pad underneath. The V^+A (Pin 14) and V^+B (Pin 10) may be supplied independently. The LTC6091 works off single or split supplies. Split supplies can be balanced or unbalanced. For example, two ±70V supplies can be used, or a 100V and –40V supply can be used. The V+ and V– pins should be bypassed with high quality surface mount ceramic capacitors. See Board Layout section for recommendations. When using split supplies, supply sequencing does not cause problems.

Input Protection

As shown in the Block Diagram, the LTC6091 has a comprehensive protection network to prevent damage to the input devices. The current limiting resistors and back-to-back diodes are to keep the inputs from being driven apart. The voltage-current relationship is that of a resistor in series with a diode until the voltage difference between the pins reaches 12V. At that point the Zener diodes turn on. Any additional current into the pins will snap back the input differential voltage to 9V.

In the event of an ESD strike between an input and V^-, the voltage clamps and ESD device fire providing a current path to V^- protecting the input devices. The input pin protection is designed to protect against momentary ESD events. A repetitive large fast input swing (>5.5V and <20ns rise time) will cause repeated stress on the MOSFET input devices. When in such an application, anti-parallel diodes (1N4148) should be connected between the inputs to limit the swing.

Output Disable

Each amplifier of the LTC6091 has its own output disable ($\overline{OD}$) pin (Refer to Figure 1). The $\overline{OD}$ pin is an active low disable with an internal 2M resistor that will pull up the $\overline{OD}$ pin enabling the output stage. The $\overline{OD}$ pin voltage is limited by an internal Zener diode tied between COM and $\overline{OD}$. When the $\overline{OD}$ pin for a particular channel is asserted low with respect to its COM pin, the output stage for that channel is disabled, leaving its bias and input circuits enabled. This results in 580µA (typical) standby current for

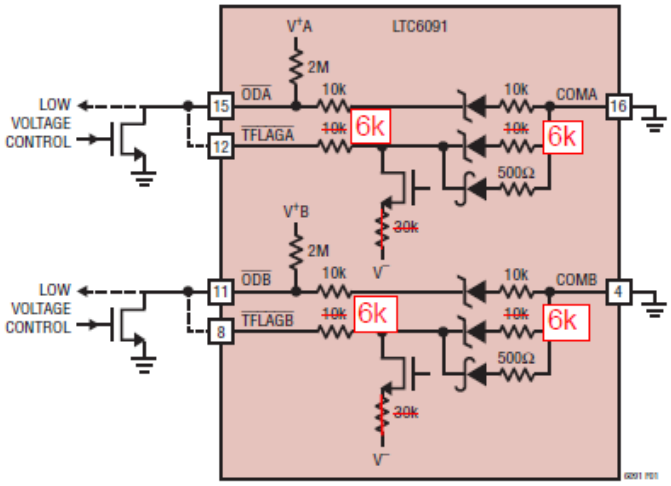

Figure 1. Low Voltage Interface Example for Output Disable

APPLICATIONS INFORMATION

the disabled channel. The $\overline{OD}$ pin can be directly connected to either an open drain NMOS device (as in Figure 1) or connected to low voltage logic circuitry.

Since the $\overline{OD}$ pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and $\overline{OD}$ pins. When coming out of shutdown the LTC6091 bias circuits and input stage are already powered up leaving only the output stage to turn on and drive to the proper output voltage. Figures 2 and 3 illustrate the part powering on and coming out of shutdown, respectively.

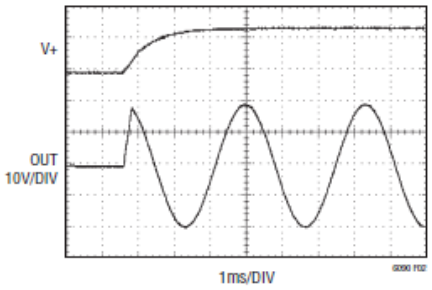

Figure 2. Starting Up

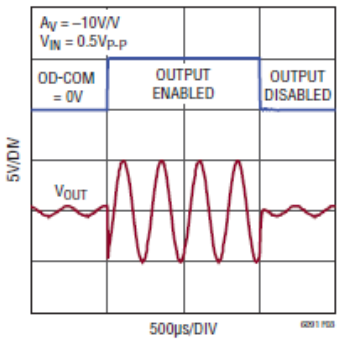

Figure 3. LTC6091 Output Disable Function

Thermal Shutdown

Each amplifier of the LTC6091 has its own trimmed temperature sensing circuit which senses die temperature in close proximity to their respective amplifier's output stage, where most of the on-chip power dissipation occurs. When one of the amplifiers's sensing circuit senses temperatures in excess of approximately 145°C, it will assert the $\overline{TFLAG}$ pin for that amplifier. The $\overline{TFLAG}$ pin is an open-drain output pin that sinks 200µA (typical) when asserted. The temperature sensor itself has approximately 5°C of hysteresis requiring the part to cool to approximately 140°C before disabling $\overline{TFLAG}$.

~~To guarantee proper operation of thermal shutdown, a few precautions must be followed when interfacing the output disable pin ($\overline{OD}$) to the $\overline{TFLAG}$ pin:~~

- For simplest operation, float both channel's COM pins (COMA and COMB), and connect $\overline{ODA}$ to $\overline{TFLAGA}$, and $\overline{ODB}$ to $\overline{TFLAGB}$ as shown in Figure 4. Both output stages will be safely disabled should the die temperature reach approximately 145°C. Both COM pins may be tied to ground ~~in this configuration so long as V^- is biased more negatively than –3V with respect to ground for proper thermal shutdown operation~~.
- ~~In the case where the COM pins are grounded, and the V^- supply is within 0V to –3V of ground, logic buffers must be used to force $\overline{ODA}$ or $\overline{ODB}$ to a logic low as shown in Figure 5. The pull-up resistor (R_{PULLUP}) of Figure 5 must be chosen large enough to guarantee a logic low for the logic buffer. For most CMOS, this requires at least 402k of pull-up resistance. Alternatively, the logic buffer is not needed if you float both COMA and COMB. With COM floating, you may simply tie the respective channel's $\overline{OD}$ directly to $\overline{TFLAG}$ for proper thermal shutdown operation.~~

Since both amplifiers share a common substrate, thermal cross coupling from one channel to the other will occur. Depending on the average die temperature, and temperature sensing accuracy, it is possible, however unlikely, for heat generated in Channel A's output stage to assert Channel B's $\overline{TFLAGB}$ or visa-versa. Should this condition occur, it should be understood that both amplifiers are operating close to their thermal shutdown limit.

Since the $\overline{TFLAG}$ pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and $\overline{TFLAG}$ pins.

For safety, a second overtemperature threshold shuts down the output stage if internal die temperatures rise to approximately 175°C. This second overtemperature indicator has approximately 7°C of hysteresis requiring the

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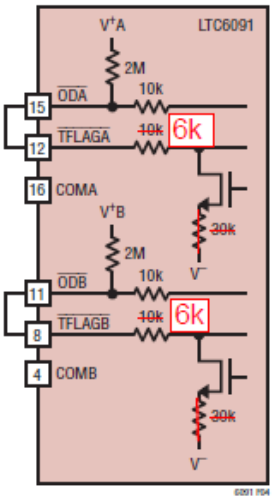

Figure 4. Automatic Thermal Output Disable Using the $\overline{\text{TFLAG}}$ Pins

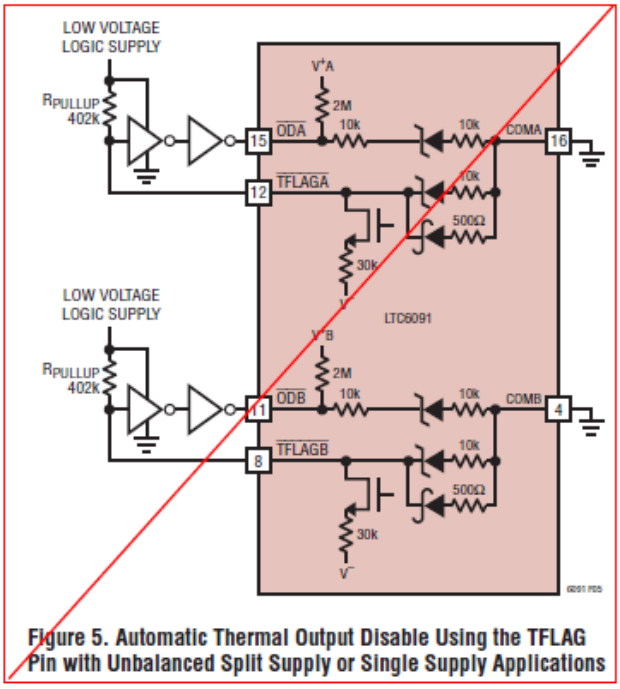

Figure 5. Automatic Thermal Output Disable Using the TFLAG Pin with Unbalanced Split Supply or Single Supply Applications

die temperature to cool 7°C. Once the device has cooled sufficiently, the output stage will enable. **Degradation can occur or reliability may be affected when the junction temperature of the device exceeds 150°C.**

Board Layout

Because the two amplifiers share a common substrate, a single bypass capacitor of 0.1µF can be used to bypass the V⁻ (as close to the pins as possible) to a low impedance ground plane. Additional bypass capacitance may be required for heavy loads. For the positive supplies, there are two independent positive supply pins (V⁺A, V⁺B): one for each amplifier. If these two supplies are tied together, they may be bypassed to a low impedance ground plane with a single capacitor (typically 0.1µF) as close to the supply pins as possible. Likewise, when driving heavy loads, additional bypass capacitance may be required.

There are other important considerations for high voltage and high power: trace spacing, humidity and dust. High voltage electric fields between adjacent conductors attract dust. Moisture absorbed by dust can contribute to PCB leakage and electrical breakdown. Vias biased to high voltage should have additional spacing to nearby ground plane.

PCB leakage related errors require special layout and cleaning practices. As little as 1000GΩ of PCB leakage between Pin 2 (+INA) and Pin 3 (V⁻) will generate 70pA of leakage with ±70V power supplies! It becomes important to clean the PCB after soldering down the part. Solder flux will accumulate dust and become a leakage hazard. It is recommended to clean the PCB with a solvent, or simply use soap and water to remove residue. Baking the PCB will remove leftover moisture. Depending on the application, a special low leakage board material may be considered. Also guarding sensitive traces as shown in Figures 6 and 7 to the greatest extent possible will also help to mitigate PCB leakage.

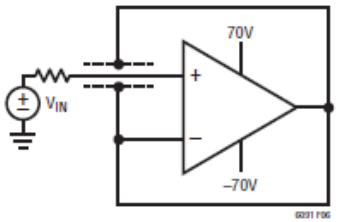

Figure 6. Example of a Noninverting Amplifier Guard Configuration