NX3P2902B

Logic controlled high-side power switch

Rev. 2 — 22 February 2018 **Product data sheet**

1. General description

The NX3P2902B is a high-side load switch which features a low ON resistance P-channel MOSFET. The MOSFET supports more than 500 mA of continuous current and an integrated output discharge resistor to discharge the output capacitance when disabled. Designed for operation from 1.1 V to 3.6 V, it is used in power domain isolation applications to reduce power dissipation and extend battery life. The enable logic includes integrated logic level translation making the device compatible with lower voltage processors and controllers. The NX3P2902B is ideal for portable, battery operated applications due to low ground current and OFF-state current.

2. Features and benefits

- Wide supply voltage range from 1.1 V to 3.6 V
- Very low ON resistance:
  - 95 mΩ at a supply voltage of 1.8 V
- High noise immunity
- Low OFF-state leakage current (600 nA maximum)
- 1.2 V control logic at a supply voltage of 3.6 V
- High current handling capability (500 mA continuous current)
- Internal output discharge resistor
- Turn-on slew rate limiting
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - CDM AEC-Q100-011 revision B exceeds 500 V
- Specified from –40 °C to +85 °C

3. Applications

- Cell phone
- Digital cameras and audio devices
- Portable and battery-powered equipment

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX3P2902BUK	x2	WLCSP4	wafer level chip-scale package; 4 bumps; 0.77 × 0.77 × 0.51 mm. (Backside coating included)	NX3P2902B

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX3P2902BUK	NX3P2902BUKZ	WLCSP4	Reel 7" Q1/T1 in Drypack	3000	T_{amb} = −40 °C to +85 °C

5. Functional diagram

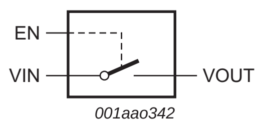


Fig 1. Logic symbol

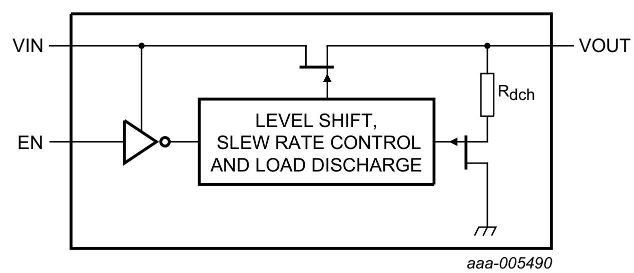


Fig 2. Logic diagram (simplified schematic)

6. Pinning information

6.1 Pinning

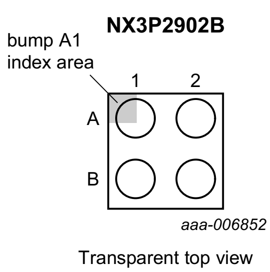


Fig 3. Pin configuration for WLCSP4

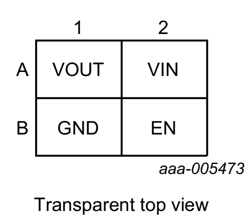


Fig 4. Ball mapping for WLCSP4

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VOUT	A1	output voltage
GND	B1	ground (0 V)
VIN	A2	input voltage
EN	B2	enable input (active HIGH)

7. Functional description

Table 4. Function table[1]

Input EN	Switch
L	switch OFF
H	switch ON

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	input EN [1]	–0.5	+4.0	V
		input VIN [2]	–0.5	+4.0	V
V_{SW}	switch voltage	output VOUT [2]	–0.5	$V_{I(VIN)}$	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V	–50	-	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V	–50	-	mA
		output VOUT: $V_{O(VOUT)} < -0.5$ V	–50	-	mA
		output VOUT: $V_{O(VOUT)} > V_{I(VIN)} + 0.5$ V	-	50	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V			
		T_{amb} = 25 °C	-	±1000	mA
		T_{amb} = 85 °C	-	±500	mA
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	[3]	-	300	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		1.1	3.6	V
T_{amb}	ambient temperature		–40	+85	°C

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1][2]	130	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Rely on the measurement data given for a rough estimation of the $R_{th(j-a)}$ in the application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts.

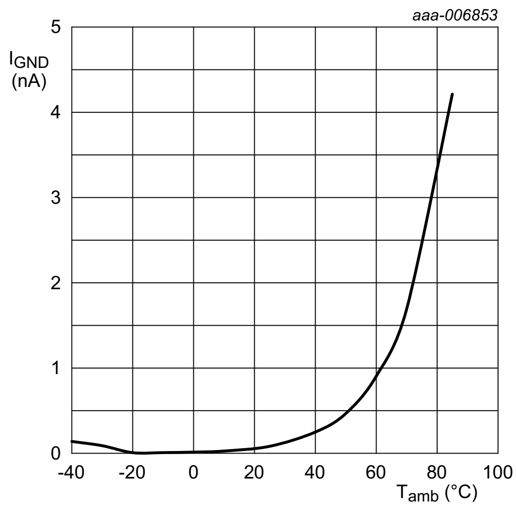
11. Static characteristics

Table 8. Static characteristics

$V_{I(VIN)}$ = 0.9 V to 3.6 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

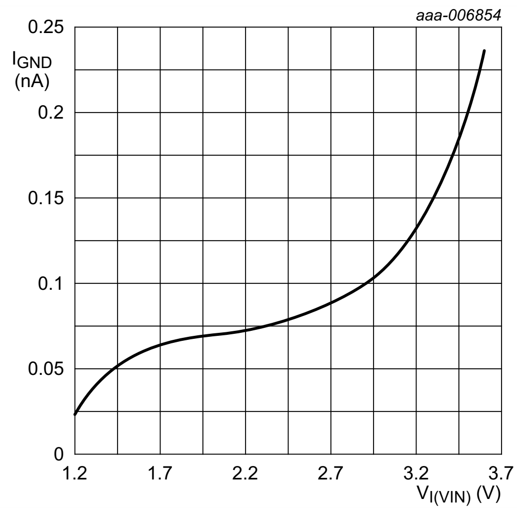
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN input						
		$V_{I(VIN)}$ = 1.1 V to 1.3 V	-	-	-	1.0	-	V
		$V_{I(VIN)}$ = 1.3 V to 1.8 V	-	-	-	1.2	-	V
		$V_{I(VIN)}$ = 1.8 V to 3.6 V	-	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	EN input						
		$V_{I(VIN)}$ = 1.1 V to 1.3 V	-	-	-	-	0.3	V
		$V_{I(VIN)}$ = 1.3 V to 1.8 V	-	-	-	-	0.4	V
		$V_{I(VIN)}$ = 1.8 V to 3.6 V	-	-	-	-	0.45	V
I_I	input leakage current	$V_{I(EN)}$ = 0 V or 3.6 V	-	0.1	-	-	500	nA
I_{GND}	ground current	$V_{I(EN)}$ = 0 V or 3.6 V; VOUT open; see Figure 5 and Figure 6	-	-	-	–2	-	µA
$I_{S(OFF)}$	OFF-state leakage current	$V_{I(VIN)}$ = 3.6 V; $V_{I(EN)}$ = GND; $V_{I(VOUT)}$ = GND; see Figure 8	-	10	-	-	600	nA
R_{dch}	discharge resistance	VOUT output; $V_{I(VIN)}$ = 3.3 V	-	90	-	-	120	Ω

11.1 Graphs



$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V; I_{LOAD} = 500 mA.

Fig 5. Ground current versus temperature



$V_{I(EN)}$ = $V_{I(VIN)}$; T_{amb} = 25 °C; I_{LOAD} = 500 mA.

Fig 6. Ground current versus input voltage on pin VIN

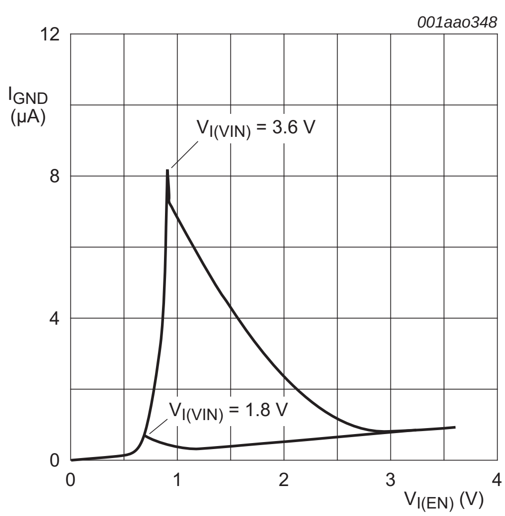
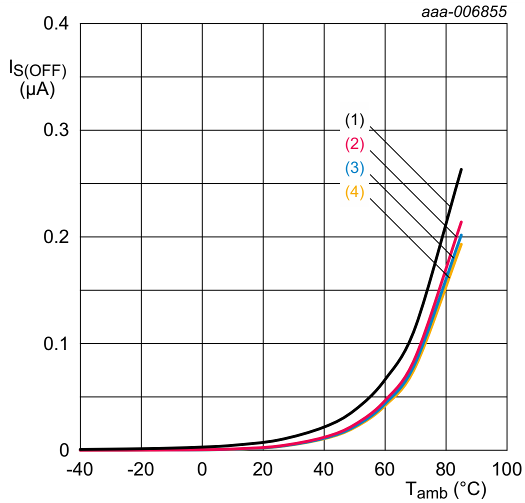


Fig 7. Additional ground current versus input voltage



$V_{I(EN)}$ = GND.

(1) $V_{I(VIN)}$ = 3.6 V.

(2) $V_{I(VIN)}$ = 2.5 V.

(3) $V_{I(VIN)}$ = 1.8 V.

(4) $V_{I(VIN)}$ = 1.2 V.

Fig 8. OFF-state leakage current versus temperature

11.2 ON resistance

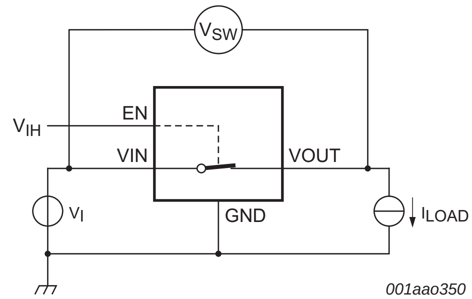
Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
R_{ON}	ON resistance	$V_{I(EN)}$ = 1.5 V; I_{LOAD} = 200 mA; see Figure 9, Figure 10 and Figure 11				
		$V_{I(VIN)}$ = 1.2 V	-	150	-	mΩ
		$V_{I(VIN)}$ = 1.5 V	-	110	-	mΩ
		$V_{I(VIN)}$ = 1.8 V	-	95	130	mΩ
		$V_{I(VIN)}$ = 2.5 V	-	75	-	mΩ
		$V_{I(VIN)}$ = 3.6 V	-	65	-	mΩ

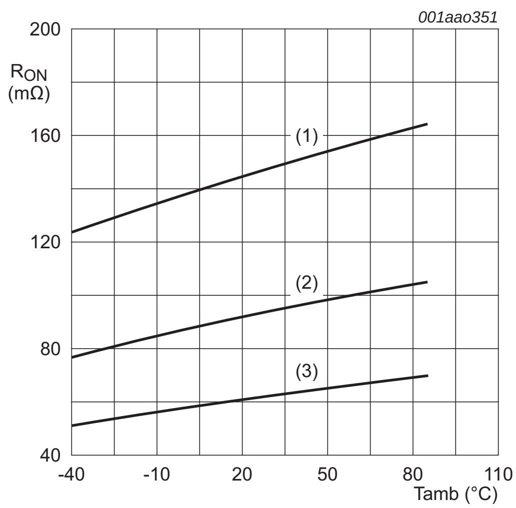
[1] Typical values are measured at T_{amb} = 25 °C.

11.3 ON resistance test circuit and waveforms



$R_{ON} = V_{SW} / I_{LOAD}$.

Fig 9. Test circuit for measuring ON resistance



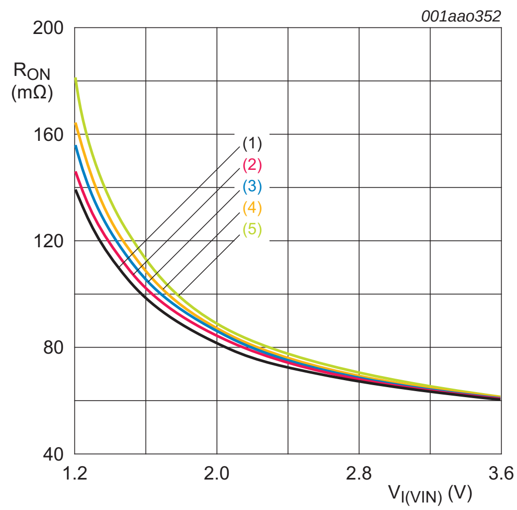
I_{LOAD} = 100 mA.

(1) $V_{I(VIN)}$ = 1.2 V.

(2) $V_{I(VIN)}$ = 1.8 V.

(3) $V_{I(VIN)}$ = 3.6 V.

Fig 10. ON resistance versus temperature



$V_{I(EN)} = V_{I(VIN)}$; T_{amb} = 25 °C.

(1) I_{LOAD} = 10 mA.

(2) I_{LOAD} = 100 mA.

(3) I_{LOAD} = 250 mA.

(4) I_{LOAD} = 350 mA.

(5) I_{LOAD} = 500 mA.

Fig 11. ON resistance versus input voltage

12. Dynamic characteristics

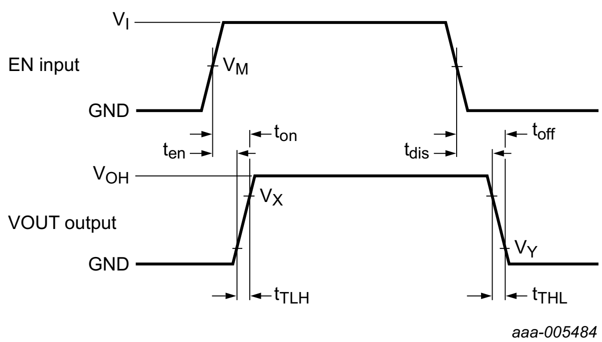
Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 12 and Figure 13.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{en}	enable time	EN to VOUT; see Figure 14				
		$V_{I(VIN)}$ = 1.8 V	175	310	-	µs
		$V_{I(VIN)}$ = 3.3 V	80	135	-	µs
t_{dis}	disable time	EN to VOUT; see Figure 14				
		$V_{I(VIN)}$ = 1.8 V	-	10	-	µs
		$V_{I(VIN)}$ = 3.3 V	-	8	-	µs
t_{on}	turn-on time	EN to VOUT; see Figure 14 and Figure 15				
		$V_{I(VIN)}$ = 1.8 V	285	570	-	µs
		$V_{I(VIN)}$ = 3.3 V	150	280	-	µs
t_{off}	turn-off time	EN to VOUT; see Figure 16 and Figure 17				
		$V_{I(VIN)}$ = 1.8 V	-	200	-	µs
		$V_{I(VIN)}$ = 3.3 V	-	180	-	µs
t_{TLH}	LOW to HIGH output transition time	VOUT				
		$V_{I(VIN)}$ = 1.8 V	110	265	-	µs
		$V_{I(VIN)}$ = 3.3 V	70	150	-	µs
t_{THL}	HIGH to LOW output transition time	VOUT				
		$V_{I(VIN)}$ = 1.8 V	-	190	-	µs
		$V_{I(VIN)}$ = 3.3 V	-	172	-	µs

[1] Typical values are measured at T_{amb} = 25 °C.

12.1 Waveforms and test circuits



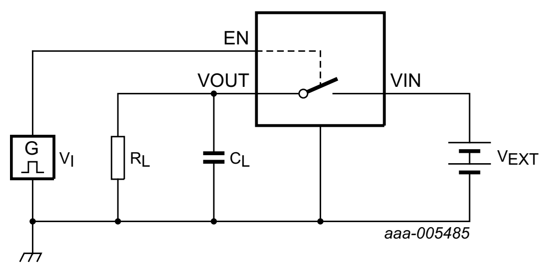
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 12. Switching times

Table 11. Measurement points

Supply voltage	EN Input		Output		
$V_{I(VIN)}$	V_M	t_r, t_f	V_M	V_X	V_Y
1.1 V to 3.6 V	0.5 × $V_{I(EN)}$	≤ 100 ns	0.5 × V_{OH}	0.9 × V_{OH}	0.1 × V_{OH}



Test data is given in Table 12.

Definitions test circuit:

R_L = Load resistance.

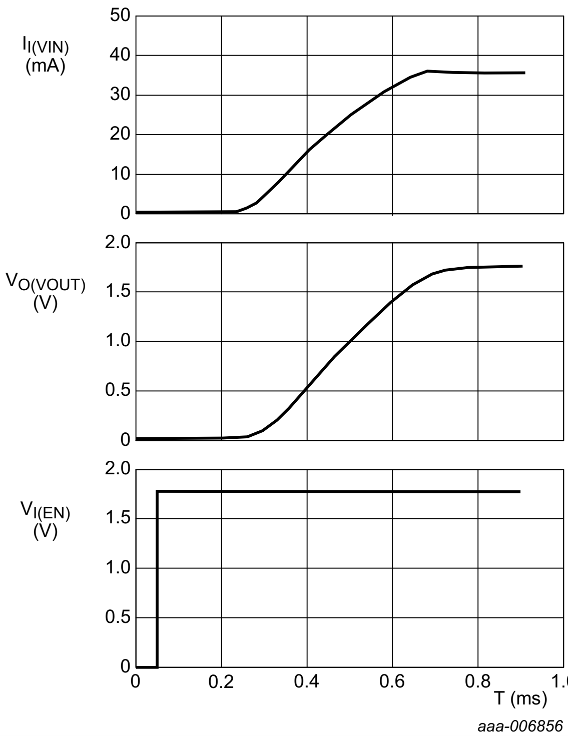
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

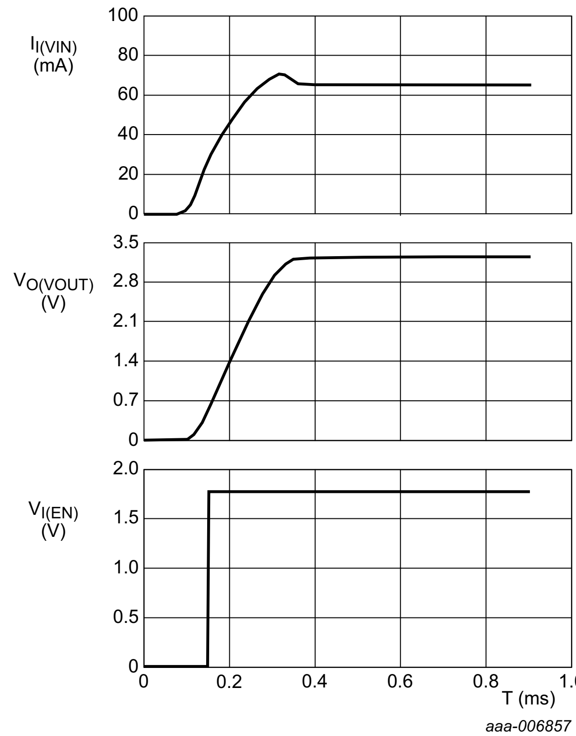
Table 12. Test data

Supply voltage	EN Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
1.1 V to 3.6 V	1.8 V	1 μF	500 Ω



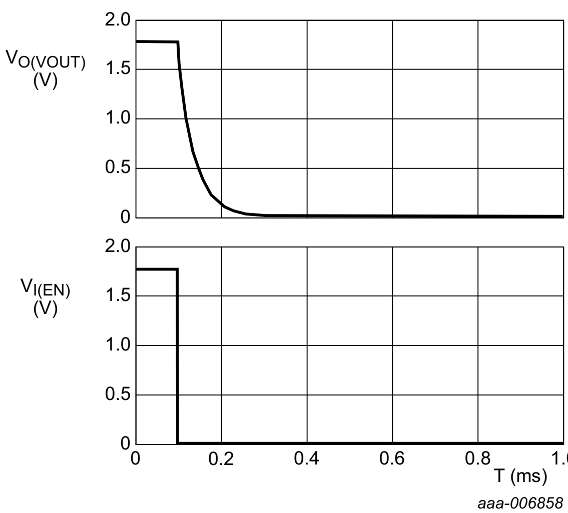
$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V; R_L = 50 Ω; C_L = 1 μF.

Fig 14. Turn-on time



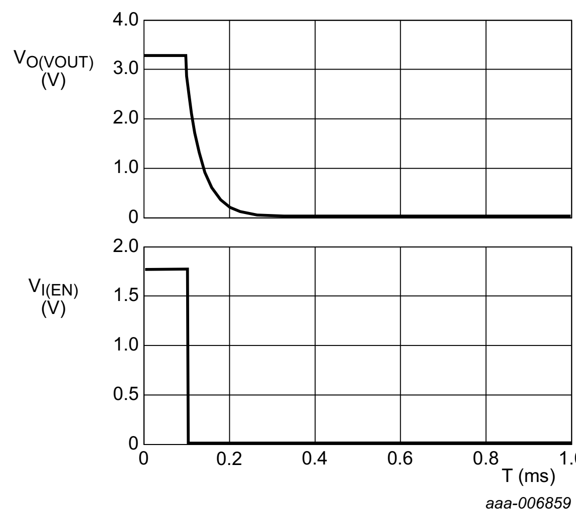
$V_{I(VIN)}$ = 3.3 V; $V_{I(EN)}$ = 1.8 V; R_L = 50 Ω; C_L = 1 μF.

Fig 15. Turn-on time



$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V; R_L = 50 Ω; C_L = 1 μF.

Fig 16. Turn-off time

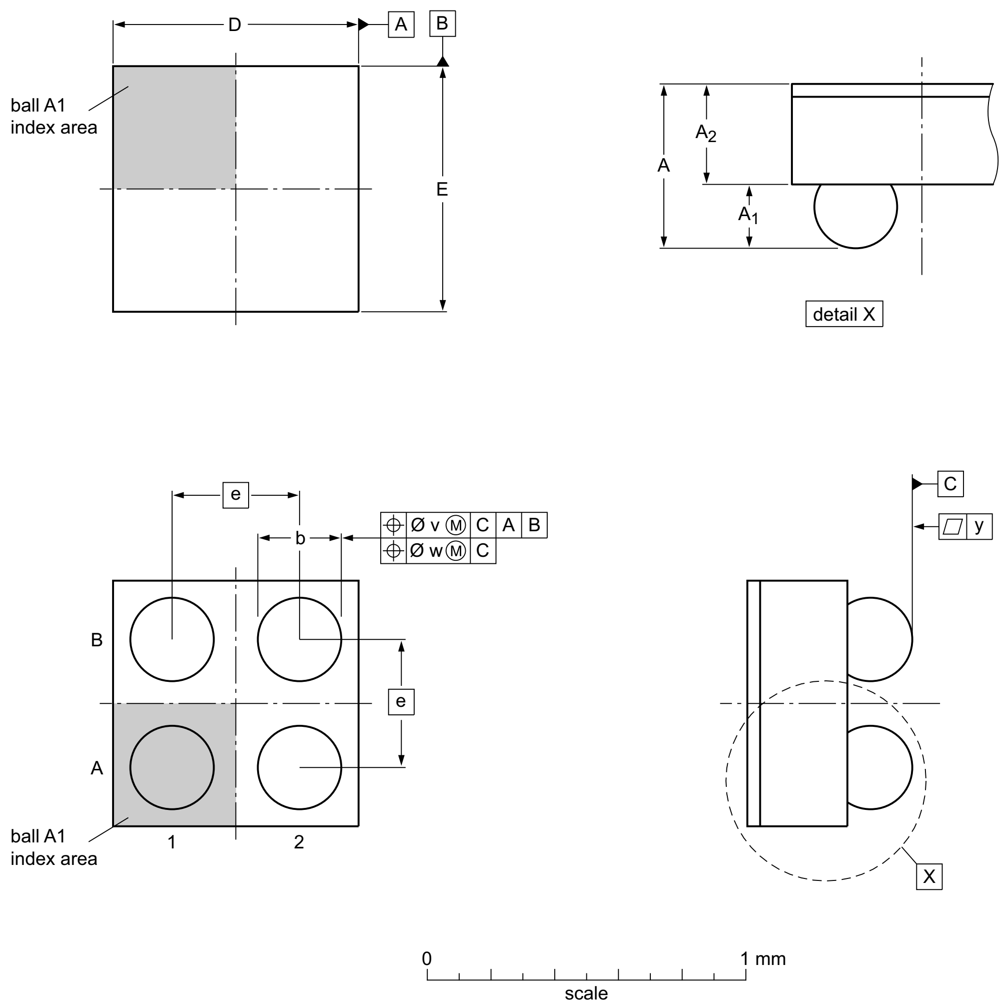


$V_{I(VIN)}$ = 3.3 V; $V_{I(EN)}$ = 1.8 V; R_L = 50 Ω; C_L = 1 μF.

Fig 17. Turn-off time

13. Package outline

WLCSP4: wafer level chip-scale package; 4 bumps; 0.77 x 0.77 x 0.51 mm (Backside coating included) **NX3P2902B**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	v	w	y
	max	0.54	0.22	0.33	0.29	0.80	0.80				
mm	nom	0.51	0.20	0.31	0.26	0.77	0.77	0.4	0.05	0.015	0.03
	min	0.48	0.18	0.29	0.23	0.74	0.74				

wlcsp4_nx3p2902b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX3P2902B						~~13-03-04~~ 13-04-02

Fig 18. Package outline WLCSP4 (NX3P2902B)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3P2902B v.2	20180222	Product data sheet	-	NX3P2902B v.1.1
Modifications:	• Updated Section 4 “Ordering information”			
NX3P2902B v.1.1	20161101	Product data sheet	-	NX3P2902B v.1
Modifications:	• Table 8: Updated OFF-state current specification			
NX3P2902B v.1	20130429	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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