

1

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U_B12
B12.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_PWR1
PWR1.SchDoc

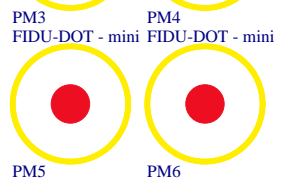
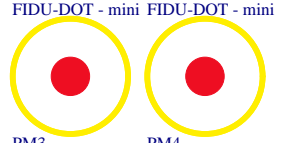
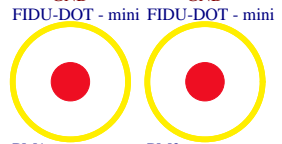
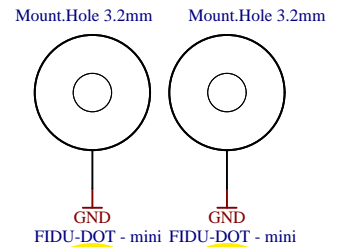
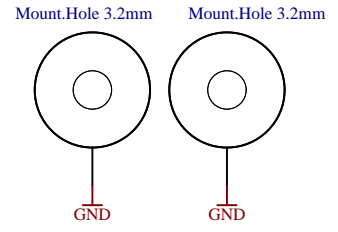
U_PWR2
PWR2.SchDoc

U_Clock
Clock.SchDoc

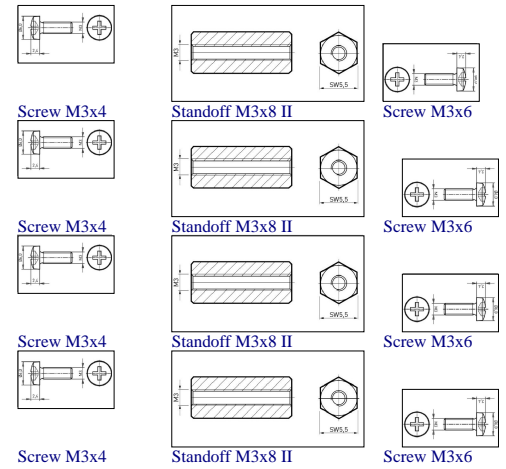
U_B2B-Connectors
B2B-Connectors.SchDoc

U_B33
B33.SchDoc

Serial
Serialnumber 6,3 x 6.3mm



Top of Board



Assembly variant	G21-1-A
Created by	VT
Modified by	VY
Modified at	2018-10-12
SVN Revision	12616



Title: TE0741		
A4	Number: TE0741 G21-1-A	Rev. 04
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1

2

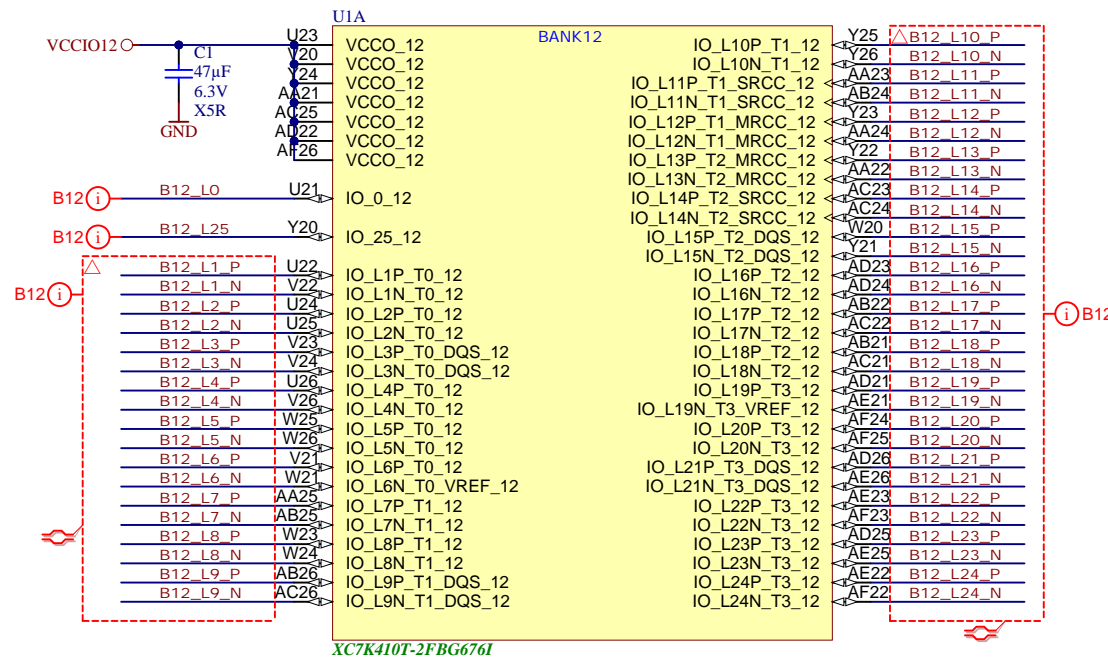
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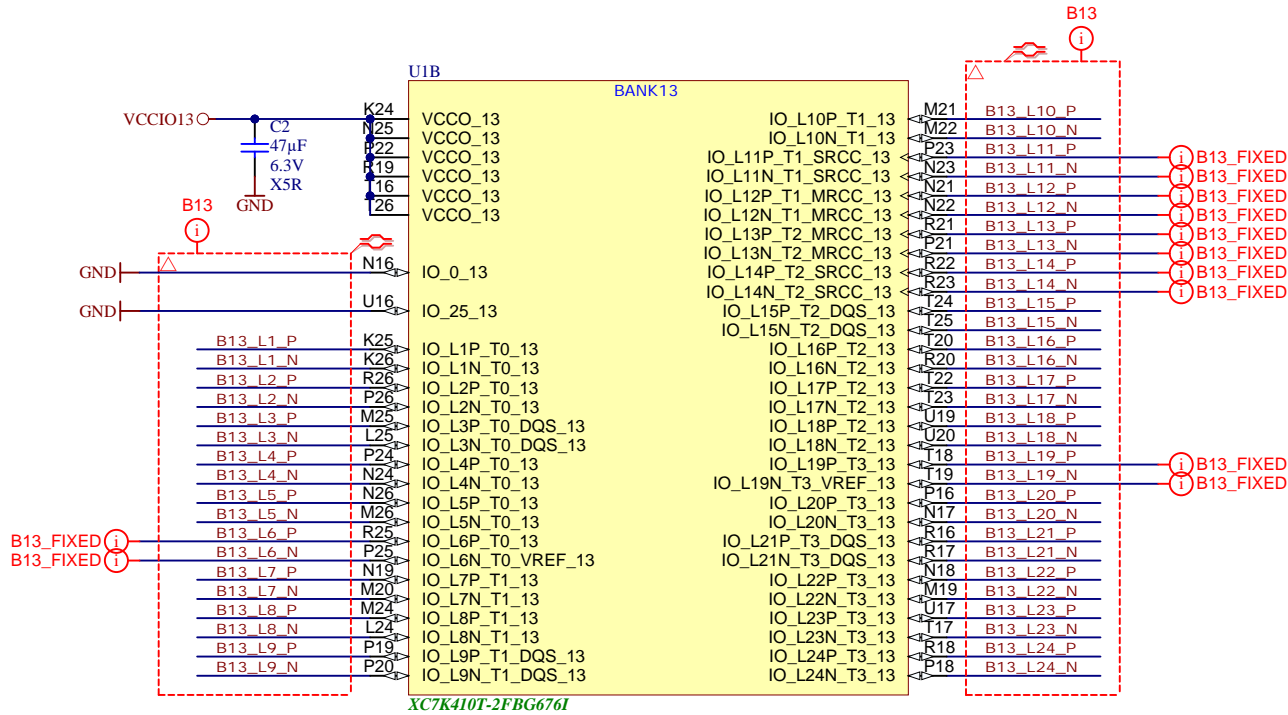
B12_FIXED ⓘ ▲

B12_L11_P
B12_L11_N
B12_L12_P
B12_L12_N
B12_L13_P
B12_L13_N
B12_L14_P
B12_L14_N
B12_L19_P
B12_L19_N
B12_L6_P
B12_L6_N

K70T version does not have this bank!



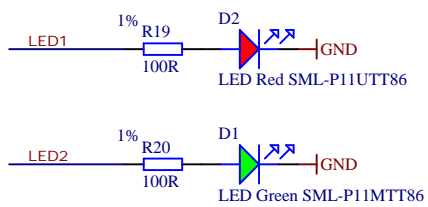
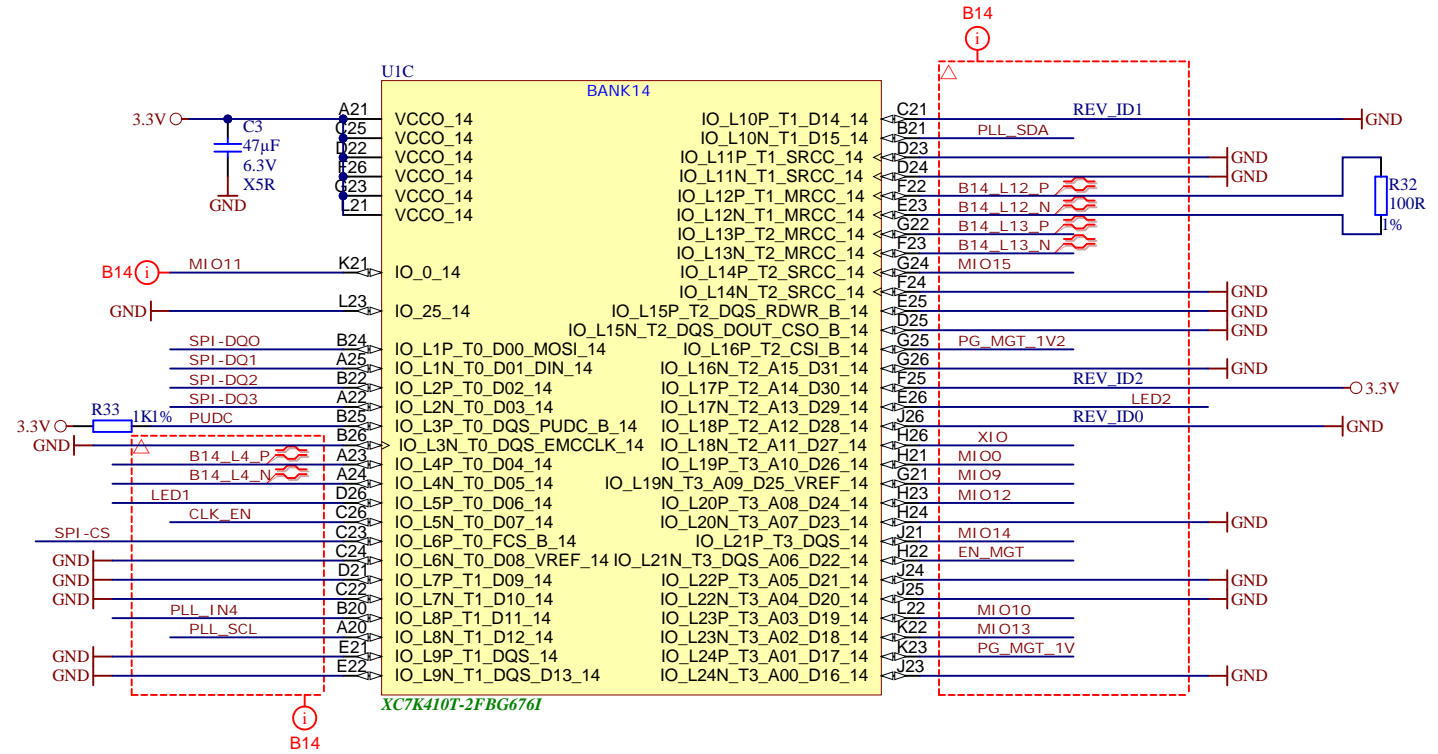
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Filename: B12.SchDoc		



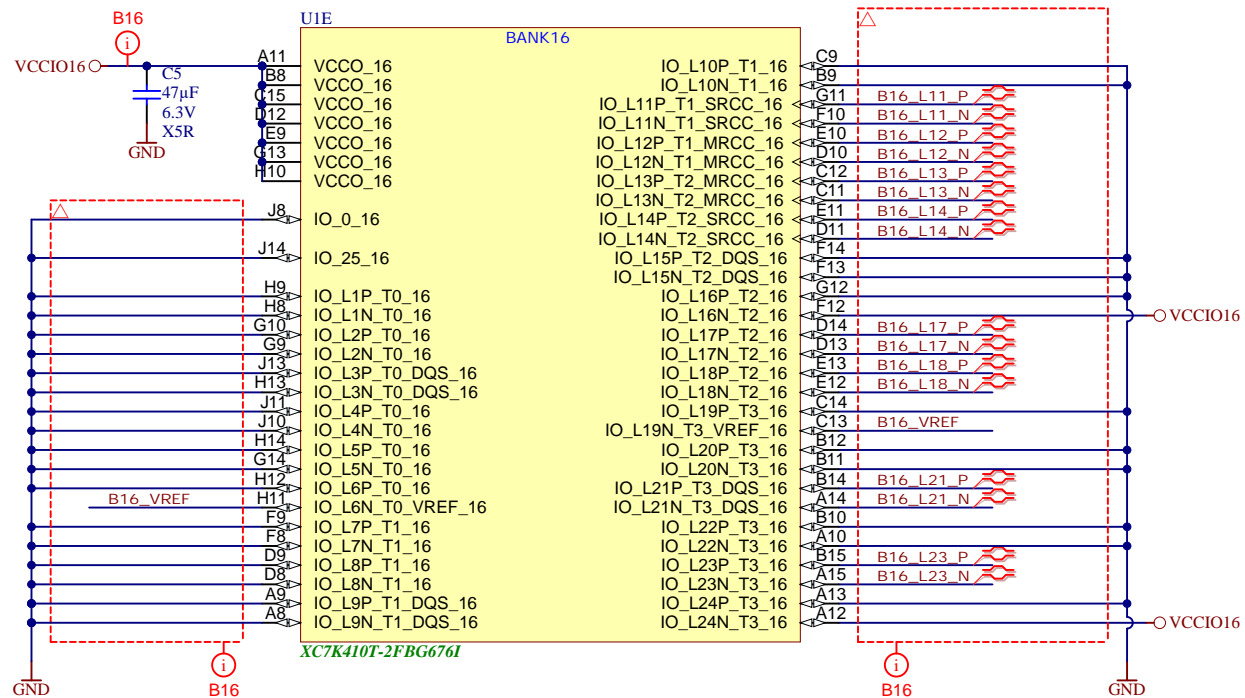
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	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 4 of 17
	Filename: B13.SchDoc		

Revision PCB Board:

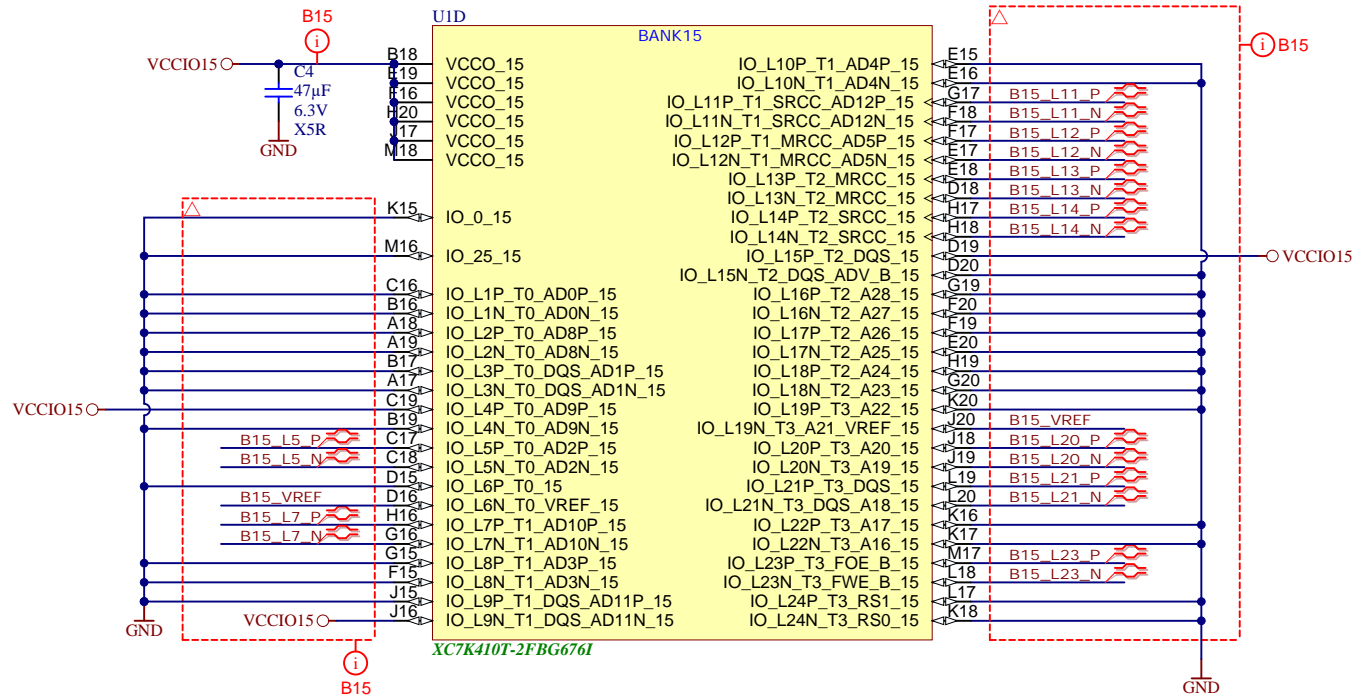
	"0"	"1"	"2"	"3"	"4"
REV_ID0	0	1	0	1	0
REV_ID1	0	0	1	1	0
REV_ID2	0	0	0	0	1




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A4	Number: TE0741 G2I-1-A	Rev. 04
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A4	Number: TE0741 G2I-1-A	Rev. 04
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		Title: TE0741	
		A4	Number: TE0741 G2I-1-A
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
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Filename: B15.SchDoc			

1

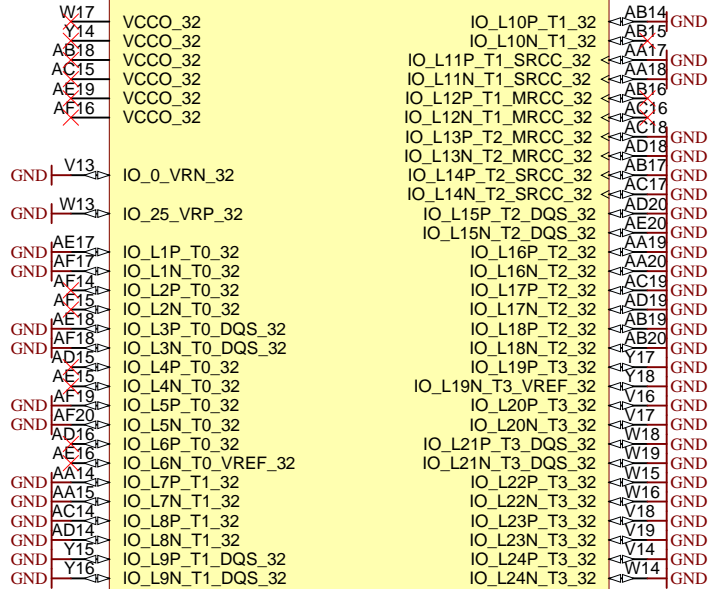
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UIF

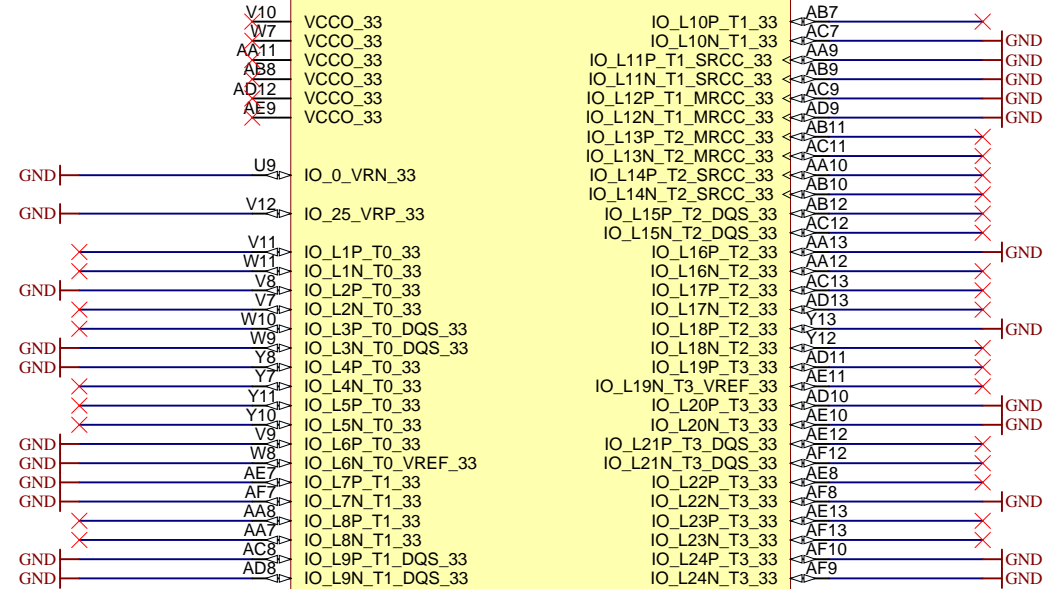
BANK32



XC7K410T-2FBG676I

UIG

BANK33



XC7K410T-2FBG676I



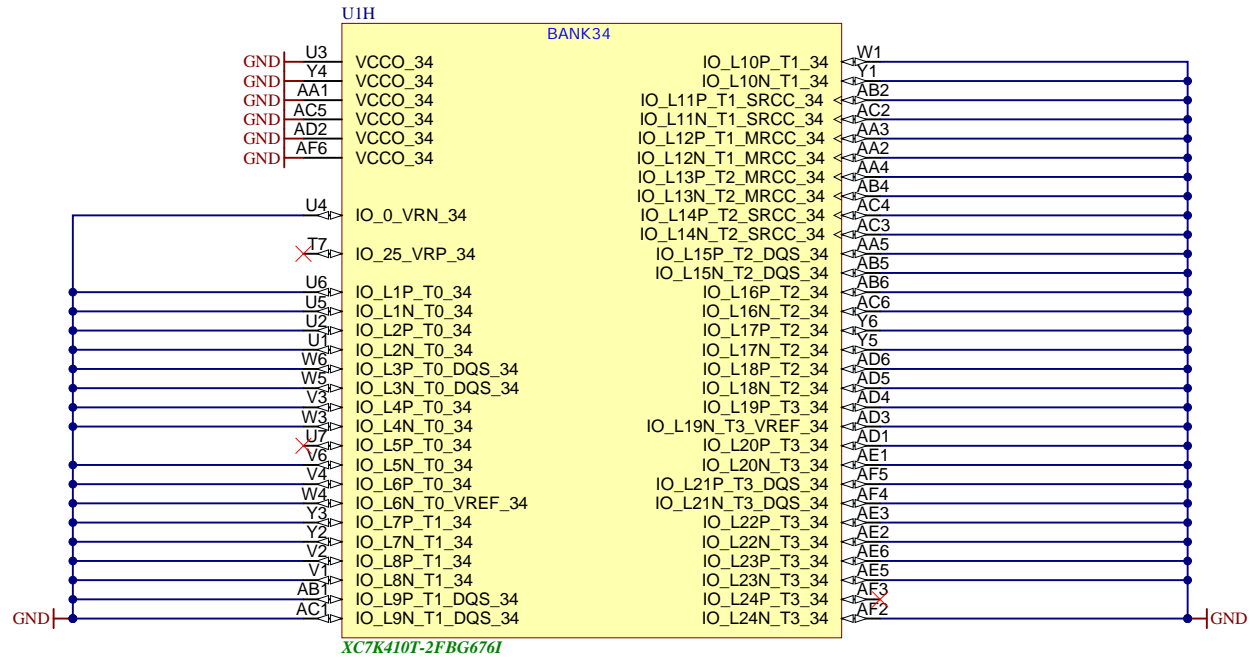

Title: TE0741		
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1

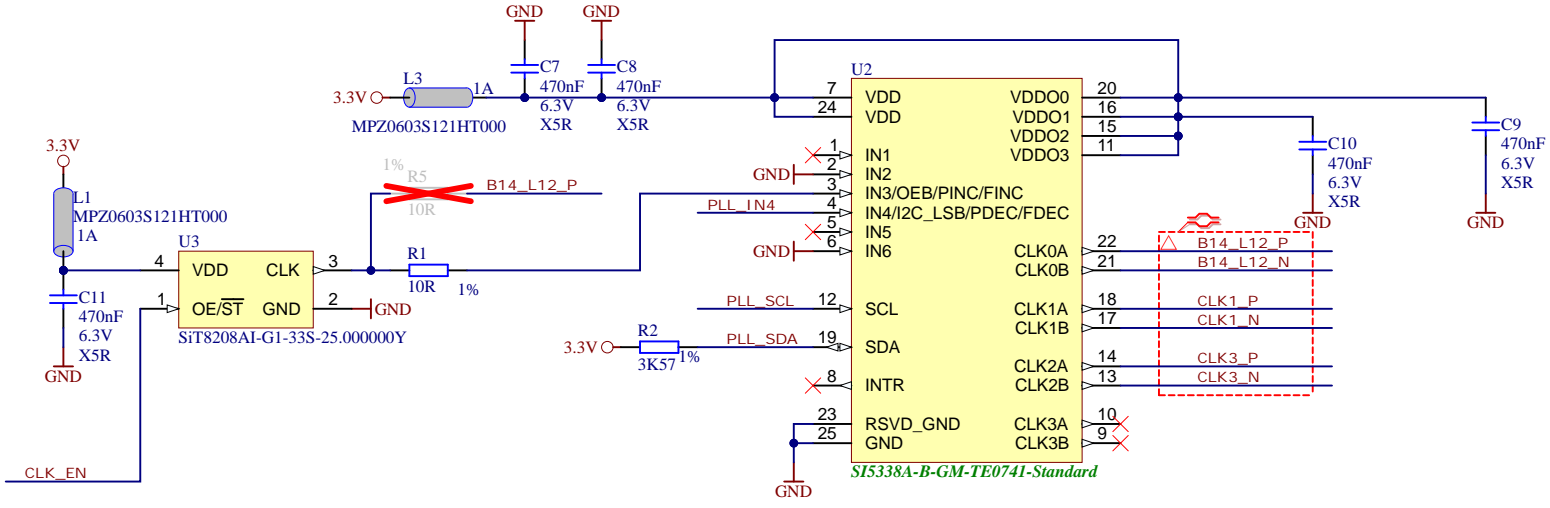
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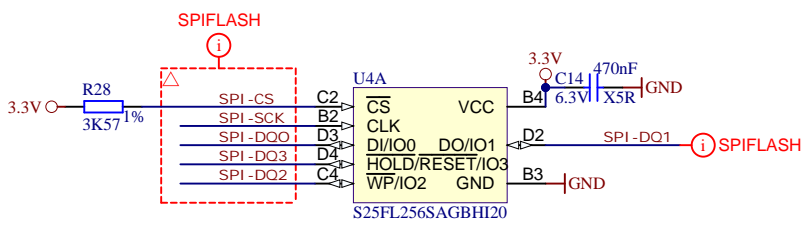
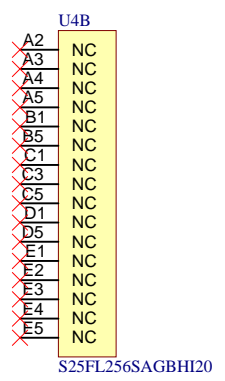
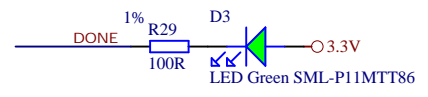
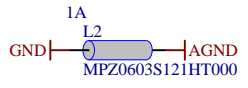
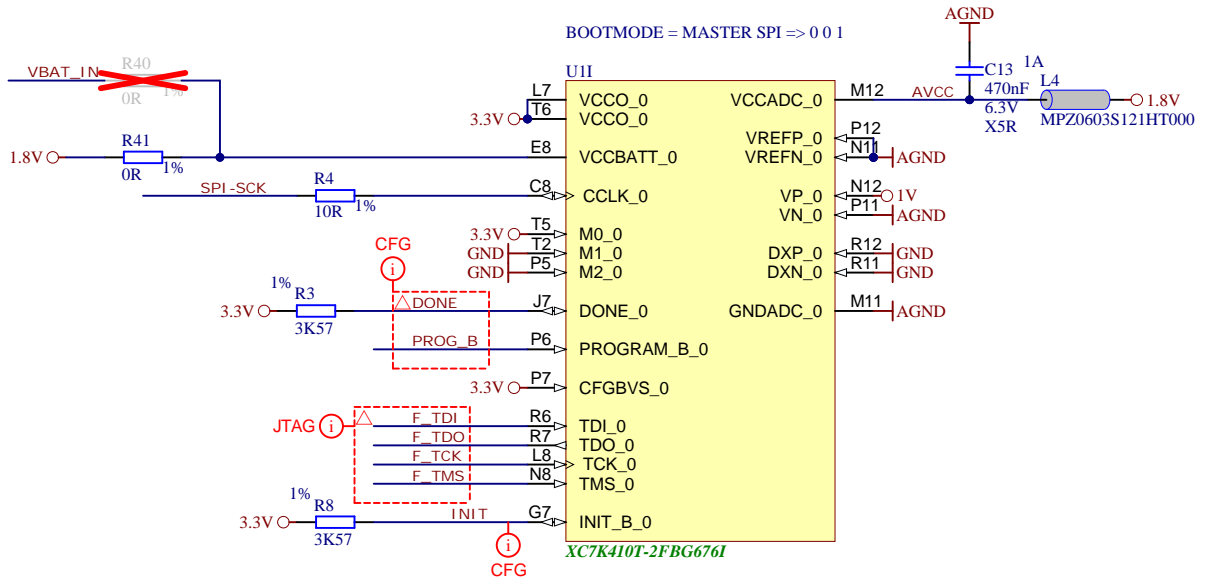
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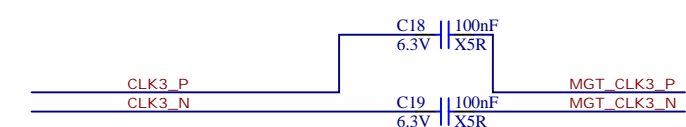
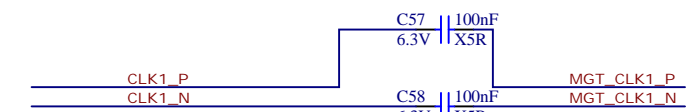
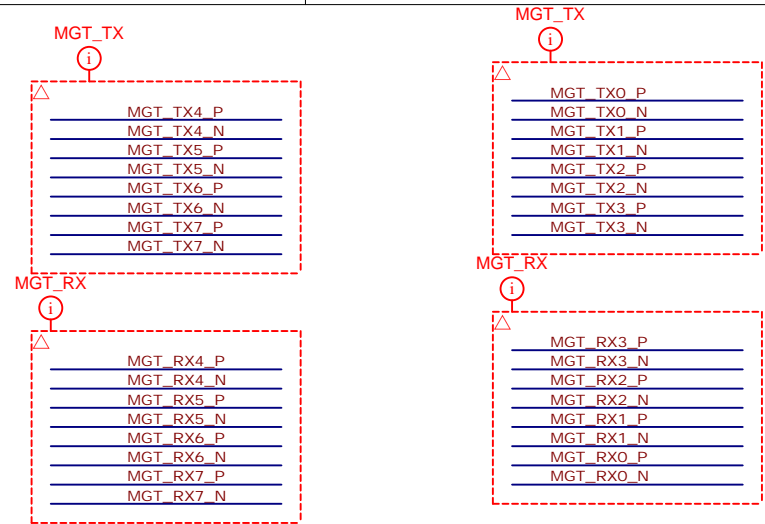
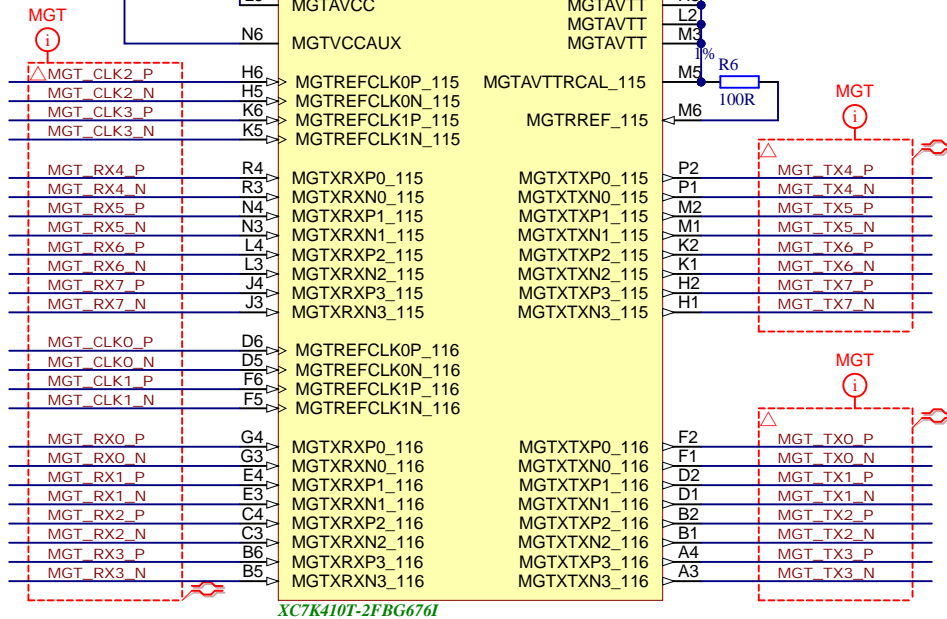
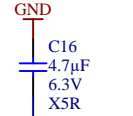
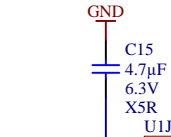
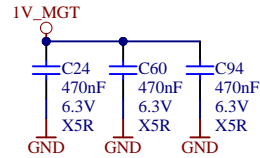
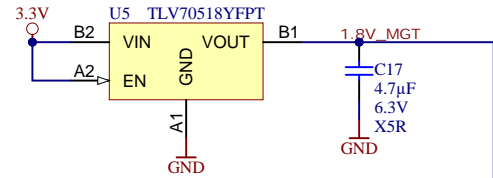
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Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page9 of 17
Filename: B34.SchDoc		




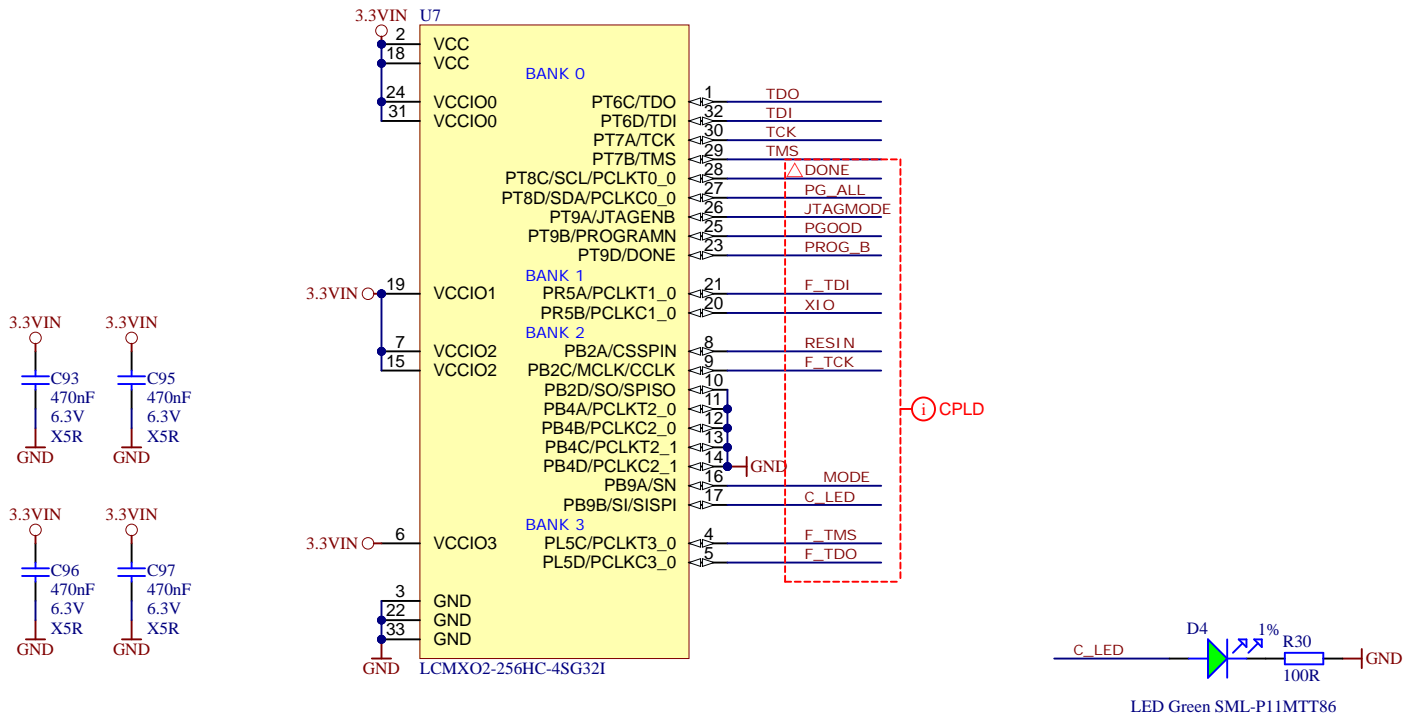
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Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Filename: Clock.SchDoc		Page 10 of 17	



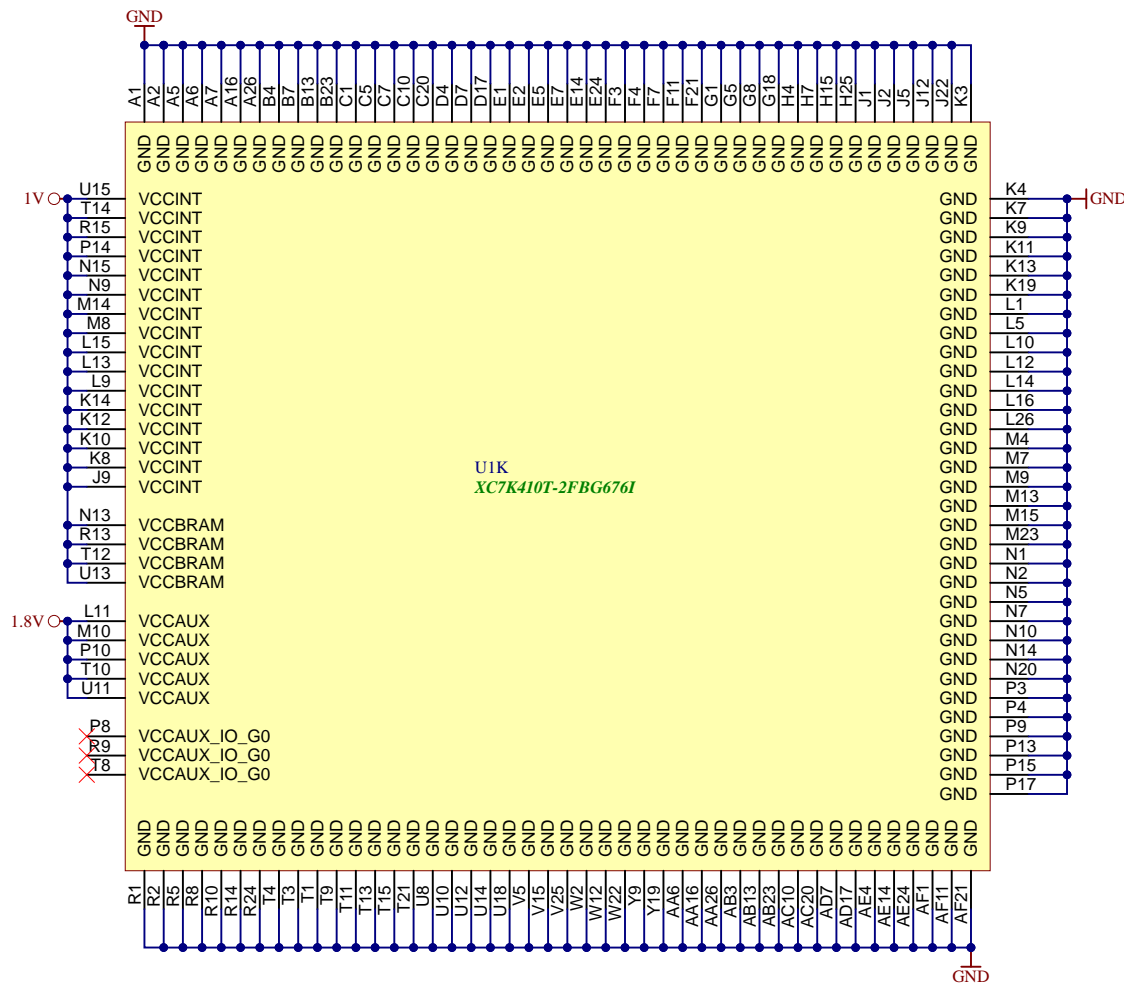
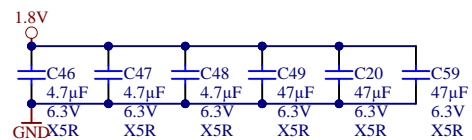
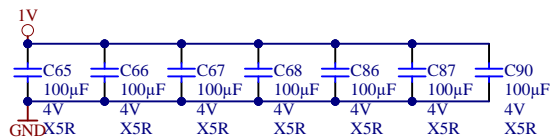
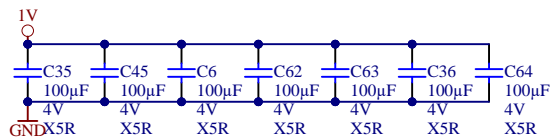
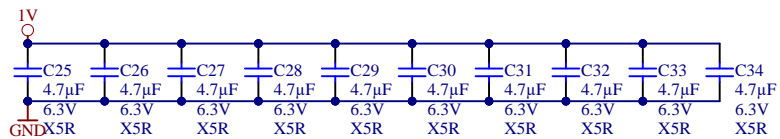
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Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA-CFG.SchDoc		



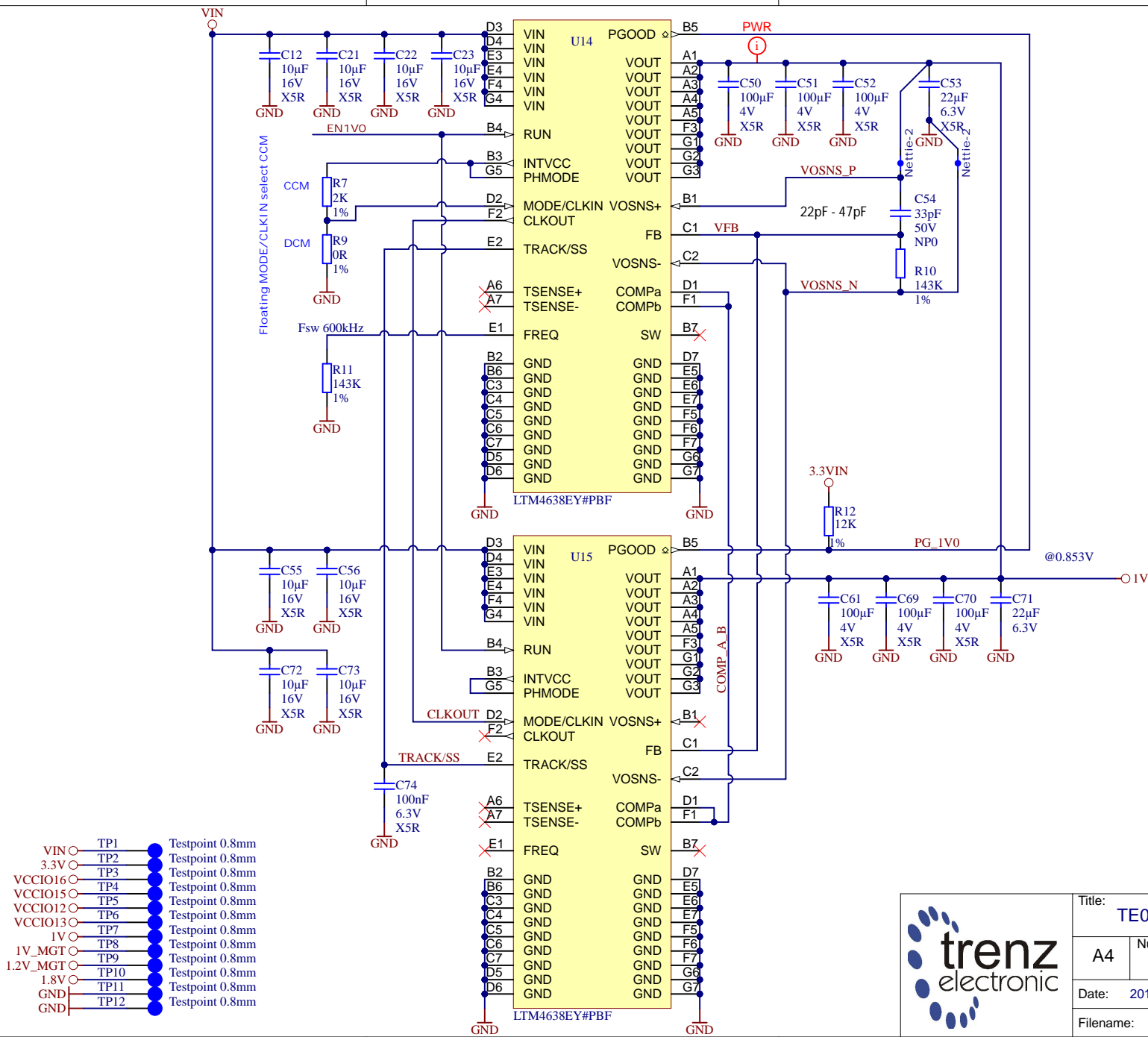
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Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH		Page 12 of 17
Filename: FPGA-MGT.SchDoc				



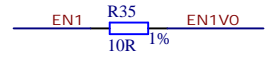
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Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page13 of 17
Filename: FPGA-MISC.SchDoc		



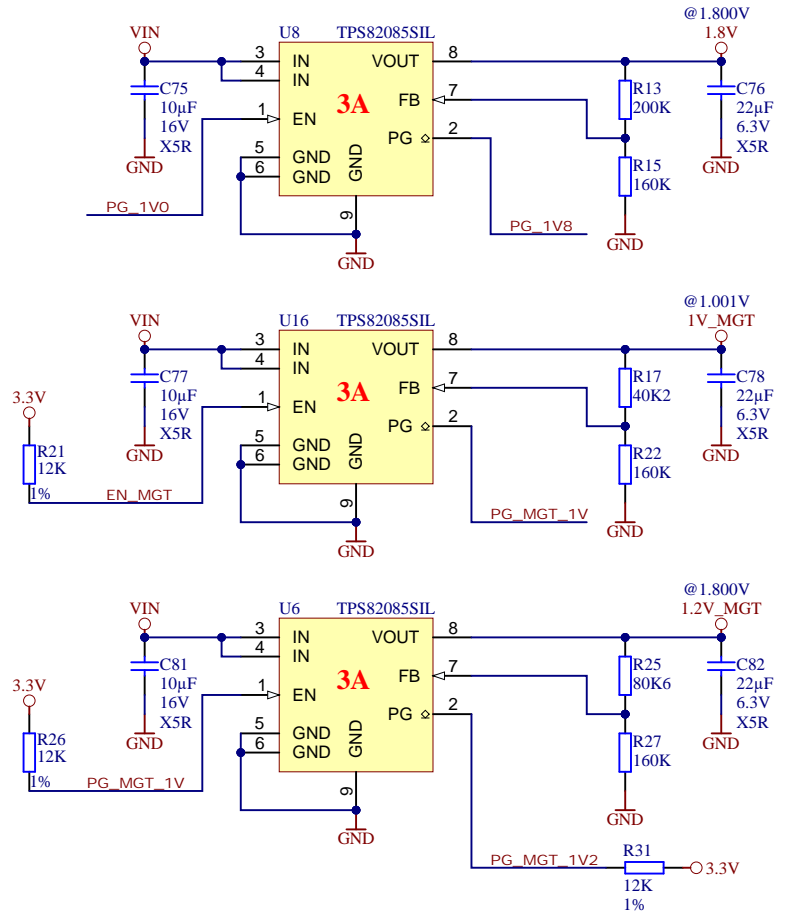
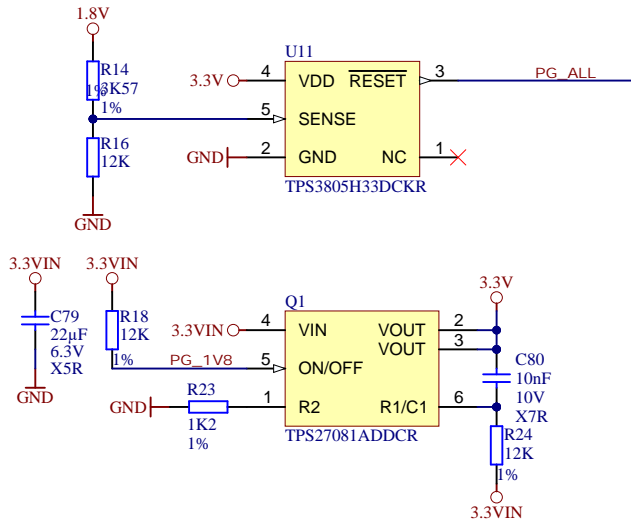
Title: TE0741		
A4	Number: TE0741 G2I-1-A	Rev. 04
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Filename: FPGA-PWR.SchDoc		



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3V ○ TP2 ● Testpoint 0.8mm
- VCCIO16 ○ TP3 ● Testpoint 0.8mm
- VCCIO15 ○ TP4 ● Testpoint 0.8mm
- VCCIO12 ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP6 ● Testpoint 0.8mm
- 1V ○ TP7 ● Testpoint 0.8mm
- 1V_MGT ○ TP8 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP9 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- GND ○ TP11 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm



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A4	Number: TE0741 G2I-1-A	Rev. 04
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A4	Number: TE0741 G2I-1-A	Rev. 04
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Filename: PWR2.SchDoc		

CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

Changes REV03 to REV04 (VT:10.2021):

- 1) replaced all DCDC (reason: not recommended use Enpirion DCDC)
- 2) remove Traceability Pad (reason: EOL)
- 3) added additional resistor for VBAT (reason: possibility using external VBAT from Carrier Board)
- 4) full upd LIB components
- 5) optimization PCB routing

A

A

B


B

C

C

D

D

		Title: TE0741 - Changes list	
		A4	Number: TE0741 G2I-1-A
Date: 2016-10-25		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page 17 of 17	