

**Customer Part:**



**Description**

- A GPS disciplined OCXO (GPSDO) incorporating sync to a 1pps input and 1pps output with tight holdover stability achieved by using an adaptive algorithm. Current internal parameters of the algorithm are available to the user via Tx and Rx commands.
- Model IQCM-100
- Model Issue number 2
- Application Information (Reference Drawing):  
Connect the 1PPS output of your GPS system to the IQCM-100. A MCU can be used to monitor the working state of the IQCM-100.
- Working States (Reference Drawing):  
Run1: Fast track. Adjust the OCXO 10MHz output frequency quickly to track the 1PPS to 10MHz with 1PPS reference.  
Run2: Slow track. Adjust the OCXO 10MHz output frequency slowly when phase error is in the defined range.  
Holdover: No 1PPS input present; an algorithm enables adaptive modelling of the frequency stability of an OCXO with reference to the GPS timing signal.  
Free Run: Clock module powered up with no 1PPS input.
- Note1: The IQCM-100 should be left powered and running for 7 days minimum before operation to allow for the OCXO's internal drift to stabilise.  
Note2: The adaptive module algorithm can be built after two days operation with good GPS signal, however this data will be lost at power down.  
Note3: When State input (Pin 8) is set low the IQCM-100 will operate in Holdover mode regardless of the 1PPS signal condition.
- Output Data Word Example:  
\$PDP,00,0,F,1,-3095,32768.0000,32768.0000,000,0000,0000,00000.0000,00000.0000,00000.0000,00000.0000,3-23,+000.0000,-0000,www.iqdfp.com,1.1,2011-05-16\*55

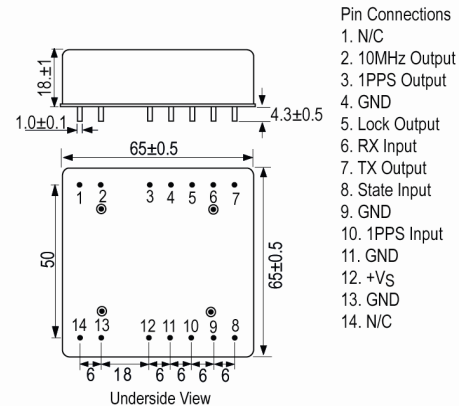
(See table for full description)

**Frequency Parameters**

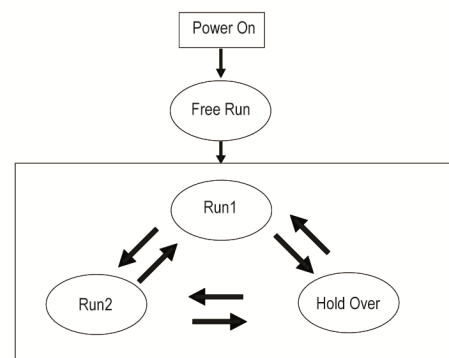
- Frequency 10.0MHz
- Operating Temperature Range -20.00 to 75.00°C
- Accuracy (24-hour averaging when locked to 1PPS): ±1E-12
- Ageing (Vs and temperature constant, reference to T=25°C, Vs = 5.0V and after 30 days operation): ±0.2ppb per day, ±10ppb per year
- Short Term Stability (tested after power for 1hr ref to 25°C, 1s): 2E-11 max



**Outline (mm)**



**Workflow Diagram**



**Sales Office Contact Details:**

UK: +44 (0)1460 270200  
Germany: 0800 1808 443

France: 0800 901 383  
USA: +1.760.318.2824

Email: [info@iqdfrequencyproducts.com](mailto:info@iqdfrequencyproducts.com)  
Web: [www.iqdfrequencyproducts.com](http://www.iqdfrequencyproducts.com)

**Customer Part:****Electrical Parameters**

- Supply Voltage 5.0V  $\pm$ 5%
- Note: Pins 3 to 11 and Pin 13 should not be subjected to a voltage greater 3.6V. If subjected to a higher voltage the processor will be damaged and the unit will not work correctly.
- 1PPS Reference Input, Pin 10 (50 $\Omega$  test condition):  
Waveform: HCMOS  
ViH: 2.7V min  
ViL: 0.4V max  
Pulse Width: 10 $\mu$ s min  
Stability: 200ns max
- State Input, Pin 8 (<5mA load):  
Lock: 2.7V min  
Unlock: 0.4V max
- Power Supply Details, Pin 12:  
Current Consumption: 2.5A during warm up, 1A steady state @25°C  
Warm up time: 15mins  
AC Ripple: 50mV pk-pk max, 10Hz to 1MHz
- 12.0V supply voltage also available, please contact our sales office for details.

**Output Details**

- Output Compatibility HCMOS
- 1PPS Reference Output, Pin 3 (15pF test condition):  
Waveform: HCMOS  
VoH: 2.7V min  
VoL: 0.4V max  
Pulse Width: 10 $\mu$ s min  
Phase Accuracy  
<30mins after GNSS lock status:  $\pm$ 200ns  
>30mins after GNSS lock status:  $\pm$ 80ns  
Phase Accuracy RMS  
>24hrs after GNSS lock status:  $\pm$ 25ns
- 10MHz RF Output Details, Pin 2:  
HCMOS Compatible, 15pF load (Sinewave 50 $\Omega$  option available)  
VoH: 2.7V min  
VoL: 0.4V max  
Rise and Fall time: 8ns max  
Duty Cycle: 45/55% max
- Lock Status Indicator, Pin 5:  
Module Locked: 2.7V min  
Module Holdover: 0.4V max  
Module Locked means Working State is = Run2
- Serial Interface (Pin 6 and Pin 7)  
UART  
VoL and ViL: 0.4V max  
VoH and ViH: 2.7V min  
Baud rate: 9600  
Bits: 8  
Parity: N  
Stop Bit: 1

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**Customer Part:**

**Noise Parameters**

- Phase Noise on 10MHz RF output signal (dBm/Hz)
 

Offset	Typical	Max
10Hz	-125	-120
100Hz	-140	-135
1kHz	-148	-143
10kHz	-152	-147
100kHz	-155	-150
1MHz	-155	-150

**Environmental Parameters**

- ESD Level: ANSI/ESDA/JEDEC JS-001-2010; HBM Class 2; 2kV to 4kV  
ANSI/ESDA/JEDEC JS-001-2010; Machine Model Class B 200V to 400V
- Storage Conditions: Temperature: -55 to 105°C  
Humidity: 30 to 80%
- Shock: IEC68-2-27 Test Ea, severity 50A, 50G 11ms half sine wave, 3 times in three mutually perpendicular axis
- Vibration: IEC 68-2-06 Test Fc, 10G, 0.75mm acceleration, 10Hz to 500Hz, 3 times in three mutually perpendicular axis

**Compliance**

- RoHS Status (2015/863/EU)      Compliant
- REACH Status                      Compliant
- MSL Rating (JDEC-STD-033):    Not Applicable

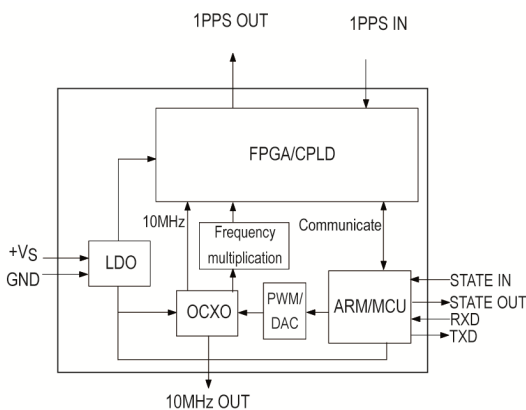
**Packaging Details**

- Pack Style: Bulk      Loose in bulk pack  
Pack Size: 1
- Alternative packing option available

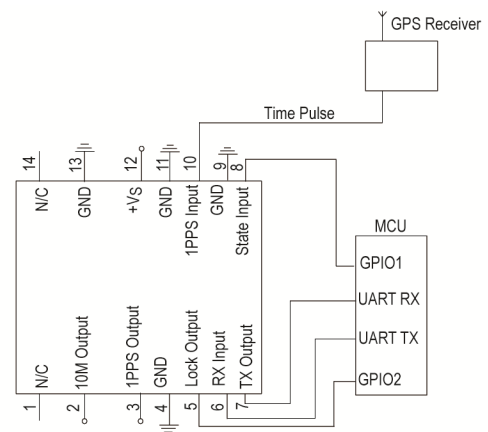
**Technical Notes**

- Holdover stability 1.5µs in 24hrs ref ±5°C

**Functional Block Diagram**



**Application Information**



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**Customer Part:**
**Output Data Word (Format Key: c=Character, d=Numerical Digit, s=Sign)**

Field No.	Name	Format	Description	Length
0	\$PDP\$	\$ccc	Message ID, Protocol Header	4
1	No	dd	Message No	2
2	TxRxFlag	d	Transmit and Receive Flag (0 = upper computer transmit, 1 = upper computer receive)	1
3	CStatus	c	Current Status (F = warm up, L = lock, H = holdover)	1
4	TrackStatus	d	Track status (Q = fast track, S = slow track)	1
5	cPHDiff	sdddd	Current phase difference, 1 unit = 6.25ns	5
6	cPWM1	dddd.dddd	Current PWM1 (Voltage control value1)	10
7	cPWM2	dddd.dddd	Current PWM2 (Voltage Controlled Value 2), not used, default value = 32769.000000	10
8	SYNCNT	ddd	The synchronous times	3
9	HCNT	ddd	Power on hours count	3
10	HPAVG	dddd.dddd	The average of the PWM in the last half hour	10
11	VCH1	dddd.dddd	Voltage Controlled compensation value every half hour	10
12	HPMOD	dddd.dddd	The Module PWM Value	10
13	VCM10	dddd.dddd	Voltage controlled compensation value every 10mins	10
14	POS	d-dd	The position of the product. (Layer-No), just for the inner test.	4
15	TEMP	sdddd.ddd	The temperature monitor inside the module	9
16	AlarmFlag	sdddd	Only the last 1 byte indicates Alarm flag (0=Normal, 1=OCXO warmup abnormal, 2=OCXOoutput abnormal, 3=Internal temperature sensor abnorm	5
17	Website		www.IQDFP.com	13
18	Version	d.d	version	3
19	Date	ddd-dd-dd	Date	10
20		dd	55	2
21	END		<CR><LF>	2

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