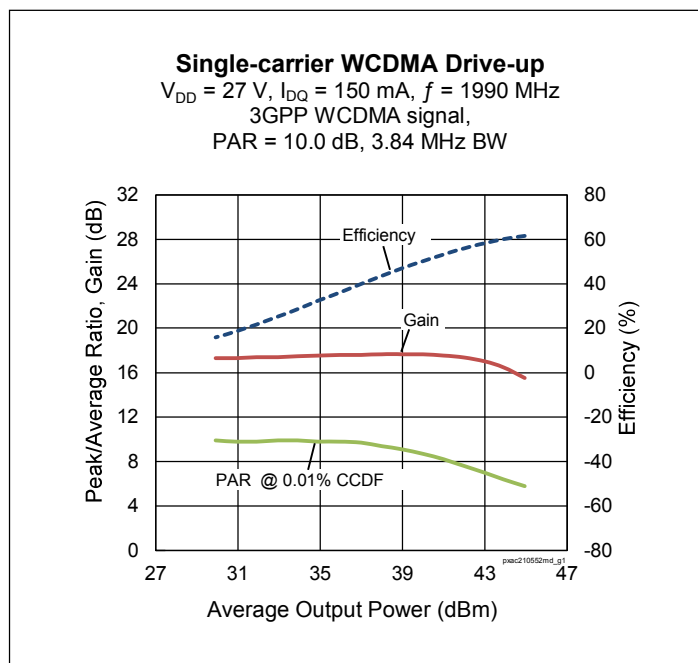


## Thermally-Enhanced High Power RF LDMOS FET 55 W, 28 V, 1805 – 2170 MHz

### Description

The PXAC210552MD is a 55-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1805 to 2170 MHz frequency band. Features include dual-path design, input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAC210552MD  
Package PG-HB1DSO-4



### Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main :  $P_{1dB} = 20\text{ W Typ}$
  - Peak :  $P_{1dB} = 35\text{ W Typ}$
- Typical Pulsed CW performance, 1990 MHz, 28 V, Doherty Configuration
  - Output power at  $P_{1dB} = 40.7\text{ W}$
  - Efficiency = 63.7 %
  - Gain = 16.7 dB
- Capable of handling 10:1 VSWR @ 27 V, 55 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1B (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

### RF Characteristics

#### Single-carrier WCDMA Specifications (tested in Infineon Doherty test fixture)

$V_{DD} = 27\text{ V}$ ,  $I_{DQ} = 150\text{ mA}$ ,  $V_{GS (Peak)} = 1.7\text{ V}$ ,  $P_{OUT} = 8.5\text{ W avg}$ ,  $f = 1995\text{ MHz}$ , 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	$G_{ps}$	15.0	16	—	dB
Drain Efficiency	$\eta_D$	42.0	44.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-33.75	-29.5	dBc

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

**ESD:** Electrostatic discharge sensitive device—observe handling precautions!

**DC Characteristics** (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1	$\mu\text{A}$
	$V_{DS} = 63\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	10	$\mu\text{A}$
Gate Leakage Current	$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	1	$\mu\text{A}$
On-State Resistance (main)	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.38	—	$\Omega$
	(peak) $V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.19	—	$\Omega$
Operating Gate Voltage (main)	$V_{DS} = 27\text{ V}, I_{DQ} = 0.15\text{ A}$	$V_{GS}$	2.1	2.6	3.1	V
	(peak) $V_{DS} = 27\text{ V}, I_{DQ} = 0\text{ A}$	$V_{GS}$	1.23	1.73	2.23	V

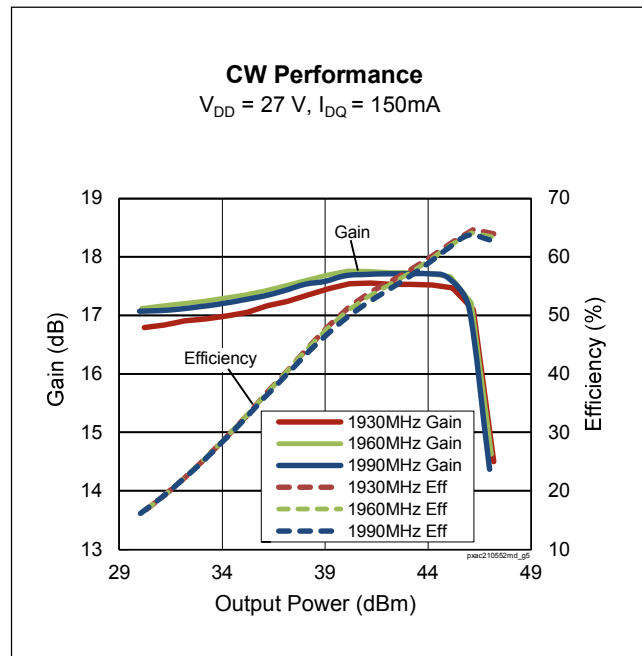
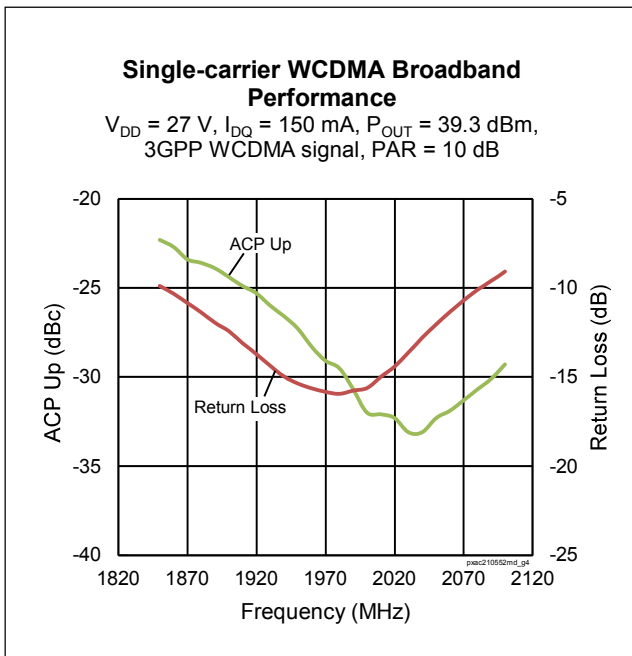
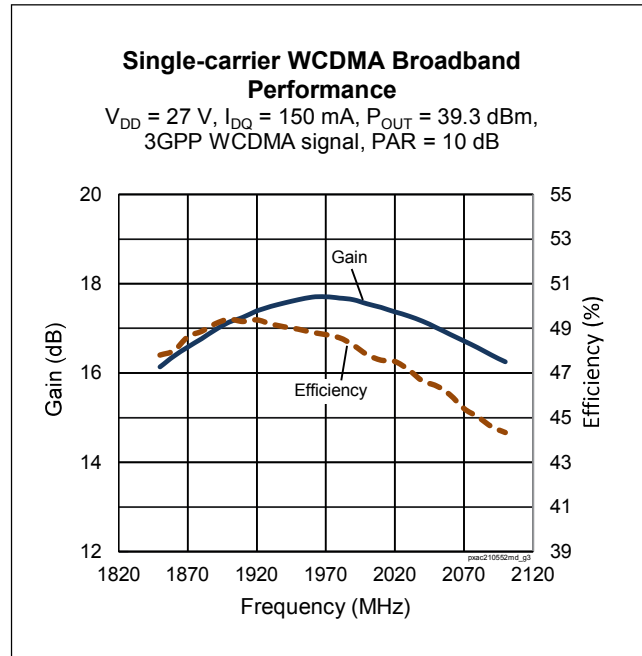
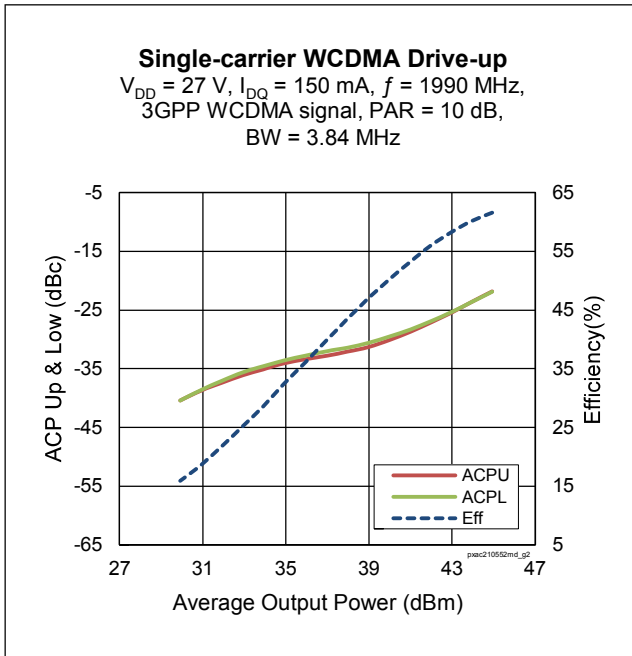
**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	V
Gate-Source Voltage	$V_{GS}$	-6 to +10	V
Operating Voltage	$V_{DS}$	0 to +32	V
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$
Thermal Resistance ( $T_{CASE} = 85^{\circ}\text{C}, 8.5\text{ W CW}$ )	$R_{\theta JC}$	1.004	$^{\circ}\text{C/W}$

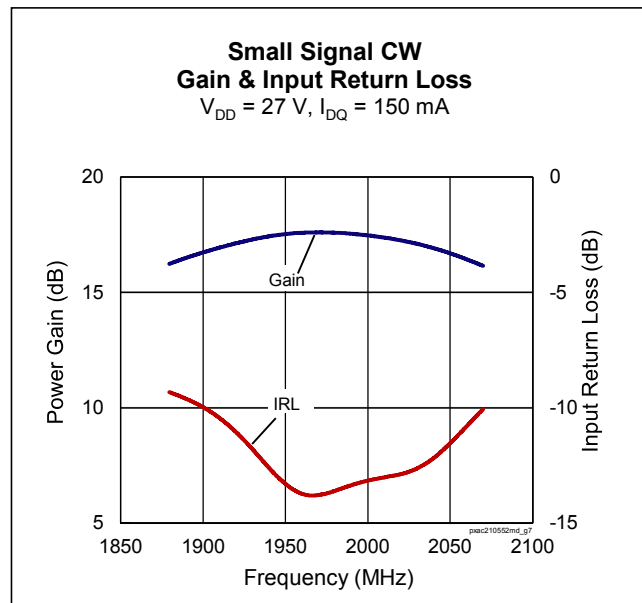
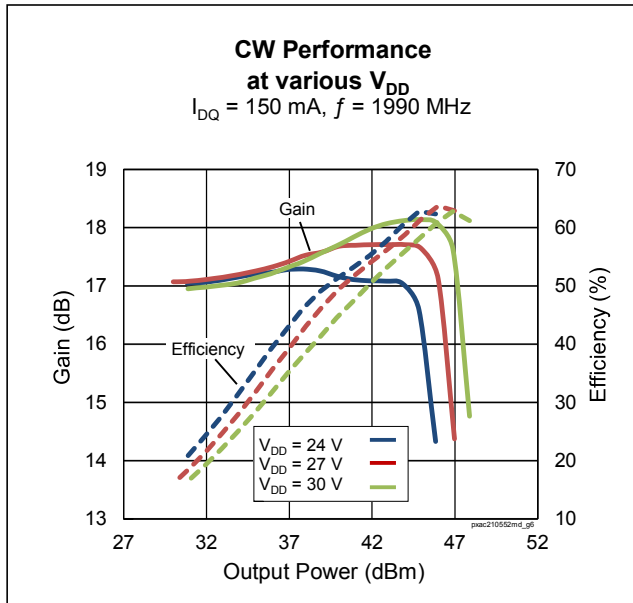
**Ordering Information**

Type and Version	Order Code	Package Description	Shipping
PXAC210552MD V1 R5	PXAC210552MDV1R5XUMA1	PG-HB1DSO-4, earless flange	Tape & Reel, 500 pcs

**Typical Performance** (data taken in a production test fixture)



Typical Performance (cont.)



Load Pull Performance

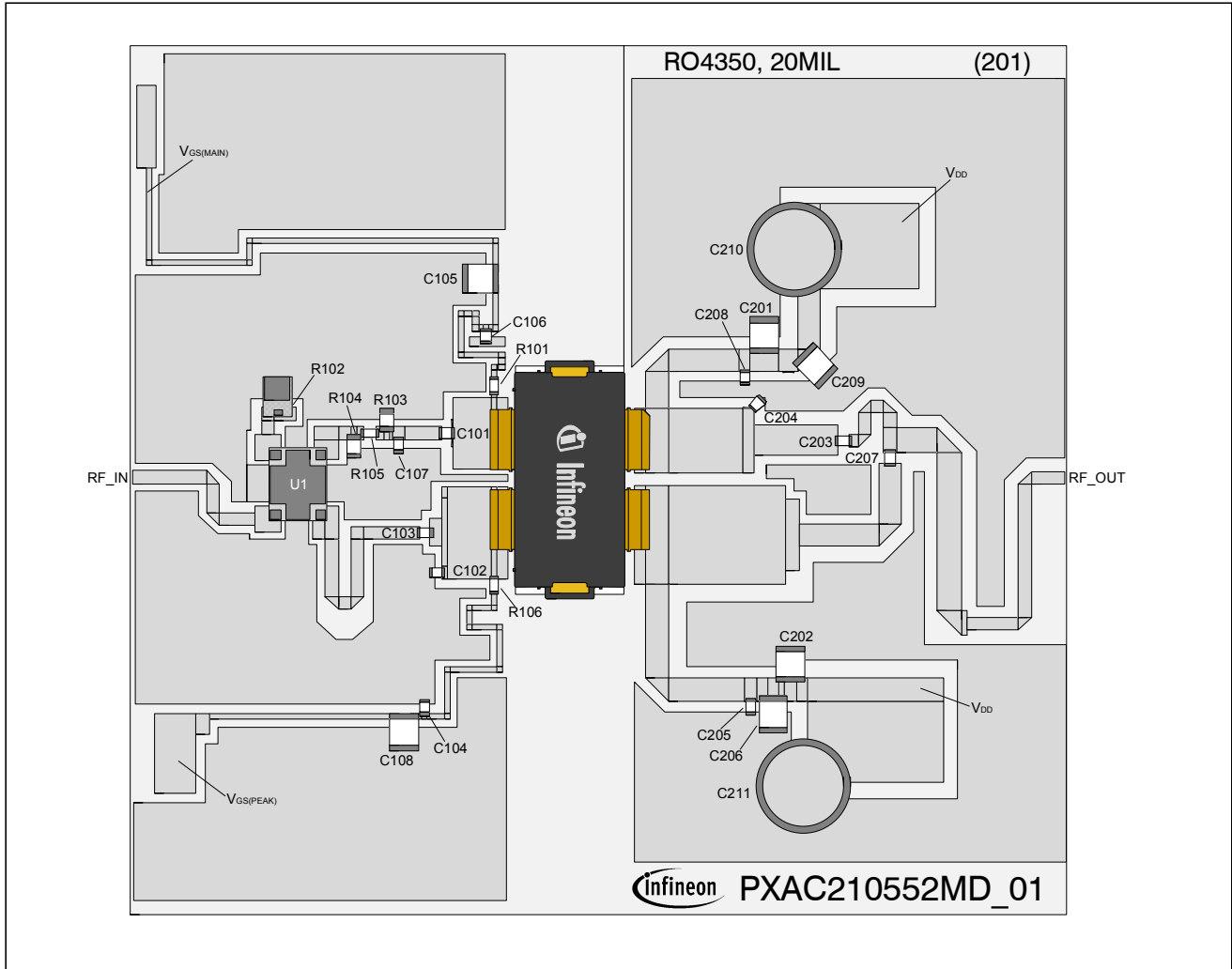
Main Side Load Pull Performance – Pulsed CW signal: 16  $\mu\text{s}$ , 10% duty cycle, 28 V,  $I_{DQ} = 130 \text{ mA}$

Freq [MHz]	$Z_s$ [ $\Omega$ ]	$P_{1dB}$									
		Max Output Power					Max PAE				
		$Z_L$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]	$Z_L$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]
1930	4.0-j14.02	8.06-j8.08	19.7	44.10	25.7	57.4	12.71-j1.6	21.6	42.40	17.4	65.8
1960	5.8-j15.08	7.01-j6.81	19.4	44.10	25.7	55.4	11.28+j0.06	21.6	42.20	16.6	65.4
1990	4.22-j17.11	7.29-j7.28	19.6	44.00	25.1	55.2	10.46-j0.71	21.7	42.40	17.4	64.8
2110	4.0-j14.02	7.1-j7.83	19.3	44.00	25.1	56.4	7.89-j0.63	21.7	42.00	15.8	64.7
2140	5.8-j15.08	7.21-j8.59	19.3	44.20	26.3	56.0	7.6-j3.18	21.0	42.90	19.5	65.2
2170	4.22-j17.11	7.18-j8.9	19.2	44.00	25.1	54.9	7.05-j2.48	21.4	42.10	64.0	64.1

Peak Side Load Pull Performance – Pulsed CW signal: 16  $\mu\text{s}$ , 10% duty cycle, 28 V,  $I_{DQ} = 250 \text{ mA}$

Freq [MHz]	$Z_s$ [ $\Omega$ ]	$P_{1dB}$									
		Max Output Power					Max PAE				
		$Z_L$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]	$Z_L$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]
1930	2.63-j8.36	3.21-j7.17	19.6	47.2	52.5	54.7	4.86-j3.72	22.0	45.30	33.9	65.4
1960	2.75-j8.79	3.07-j6.73	19.7	47.0	50.1	54.1	4.62-j3.84	22.1	45.10	32.4	63.5
1990	2.94-j8.93	3.09-j6.8	19.8	46.9	49.0	53.8	4.53-j3.83	22.3	44.90	30.9	63.0
2110	6.41-j10.53	3.23-j8.07	20.0	47.0	25.7	54.4	3.48-j5.04	22.4	45.10	32.4	63.4
2140	8.26-j10.26	3.28-j8.45	19.9	46.9	25.7	53.5	3.26-j5.24	22.6	44.90	30.9	63.6
2170	10.51-j5.44	2.78-j8.13	20.3	46.9	25.1	54.2	3.02-j5.67	22.6	44.90	30.9	61.9

Reference Circuit, 1805 – 2170 MHz



Reference circuit assembly diagram (not to scale)

**Reference Circuit** (cont.)

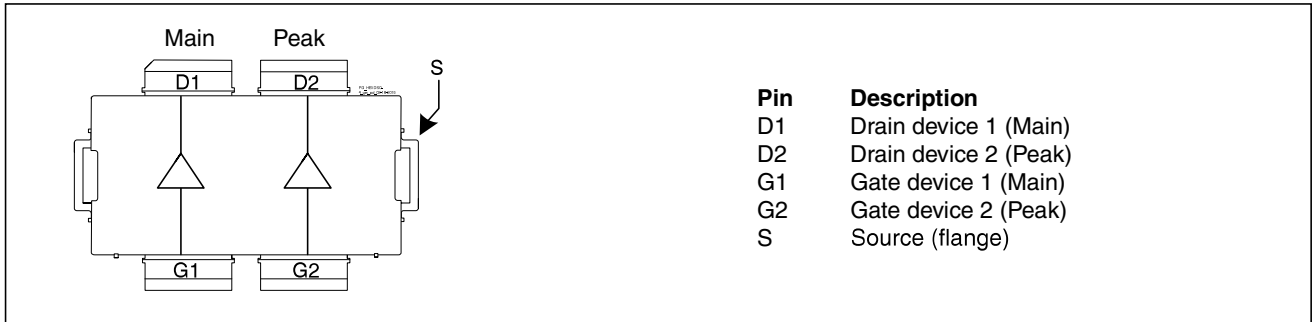
**Reference Circuit Assembly**

DUT	PXAC210552MD V1
Test Fixture Part No.	LTA/PXAC210522MD V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$ , $f = 1805 - 2170$ MHz
Find Gerber files for this test fixture on the Infineon Web site at <a href="http://www.infineon.com/rfpower">http://www.infineon.com/rfpower</a>	

**Components Information**

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101	Capacitor, 4.7 pF	ATC	ATC600F4R7CW250T
C102, C104, C106	Capacitor, 12 pF	ATC	ATC600F120JW250T
C103	Capacitor, 5.6 pF	ATC	ATC600F5R6CW250T
C105, C108	Capacitor, 10 $\mu$ F	Taiyo Yuden	UMK325C7106MM-T
C107	Capacitor, 2 pF	ATC	ATC600F2R0CW250T
R101, R106	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-3GEYJ100V
R102	Resistor, 50 ohms	Richardson	C8A50Z4A
R103, R104	Resistor, 470 ohms	Panasonic Electronic Components	ERJ-8GEYJ471V
R105	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-3GEYJ100V
U1	Hybrid Coupler	Anaren	X3C25P1-02S
<b>Output</b>			
C201, C202, C206, C209	Capacitor, 10 $\mu$ F	Taiyo Yuden	UMK325C7106MM-T
C203	Capacitor, 2 pF	ATC	ATC600F2R0CW250T
C204	Capacitor, 0.2 pF	ATC	ATC600F0R2CW250T
C205, C207, C208	Capacitor, 12 pF	ATC	ATC600F120JW250T
C210, C211	Capacitor, 47 $\mu$ F	Cornell Dubillier Electronics (CDE)	SEK470M100ST

**Pinout Diagram** (top view)



### Package Outline Specifications

**Package PG-HB1DSO-4 with Formed Leads (top view)**

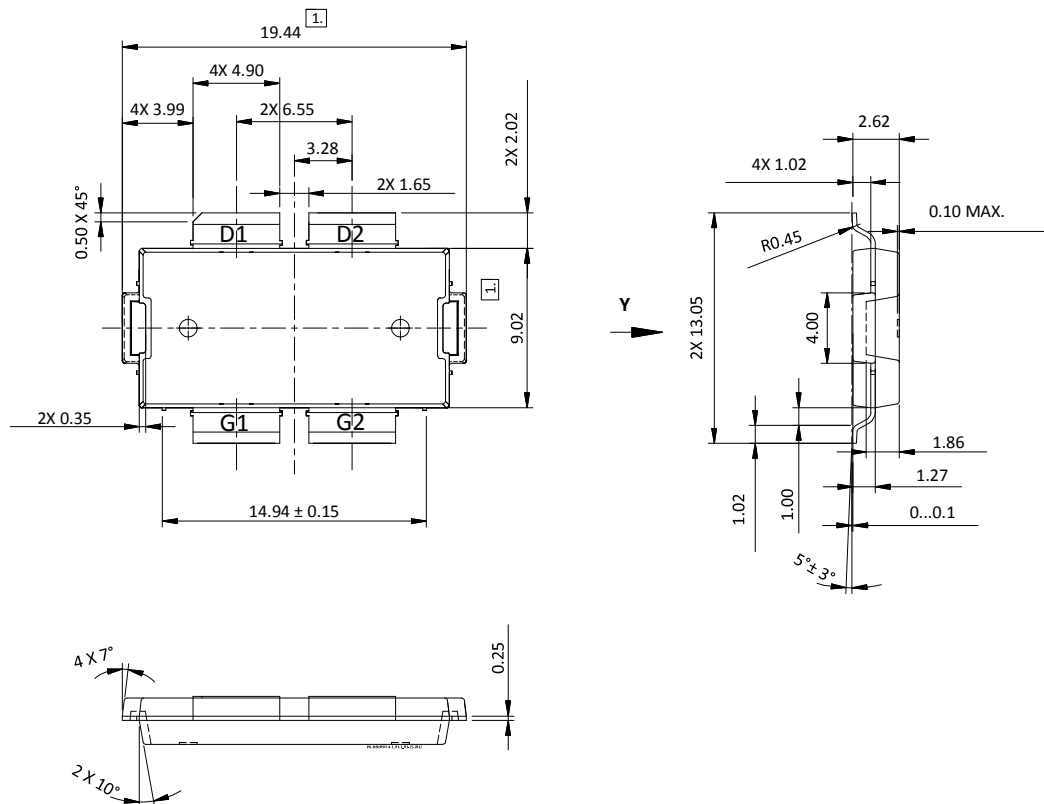


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.30 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. All tolerances ± 0.1 mm unless specified otherwise.
7. All metal surfaces pre-plated, except area of cut.
8. Lead thickness: 0.25 mm.
9. Gold plating thickness: 0.25 micron [10 microinch] max.
10. Pins: D1, D2 – drain; G1, G2 – gate; S – source.



## Package Outline Specifications

**Package PG-HB1DSO-4 with Formed Leads** (bottom view)

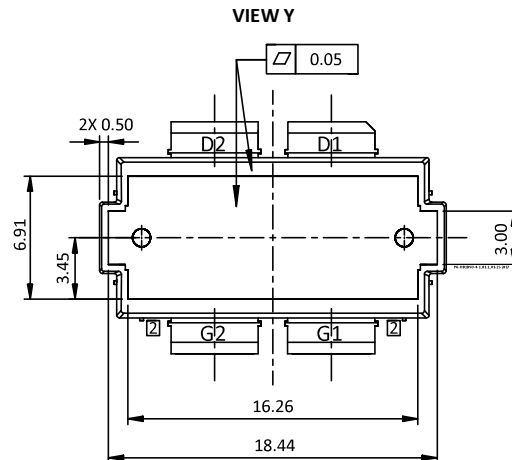


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.30 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. All tolerances  $\pm 0.1$  mm unless specified otherwise.
7. All metal surfaces pre-plated, except area of cut.
8. Lead thickness: 0.25 mm.
9. Gold plating thickness: 0.25 micron [10 microinch] max.
10. Pins: D1, D2 – drain; G1, G2 – gate; S – source.

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## Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2015-07-24	Advance	All	Data Sheet reflects advance specification for product development
02	2016-04-01	Production	All All	Data Sheet reflects released product specification Revised all data and includes updated final specs, typical performance graphs, loadpull, reference circuit, package outline
03	2016-06-02	Production	1–4 5, 6 8, 9	Revised graphs, VSWR voltage number Labeled V <sub>DD</sub> , V <sub>GG</sub> , R <sub>FIN</sub> and R <sub>FOUT</sub> in reference circuit, corrected components information Corrected package name
03.1	2017-01-25	Production	8, 9	Revised typo package outline

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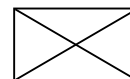
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