LC05551XA

Battery Protection IC, OTP Function, 1-Cell Lithium-Ion Battery

ON Semiconductor®

www.onsemi.com

WLCSP8
0.81 x 1.51 x 0.40
CASE 567UN

Overview

LC05551XA is a protection IC for 1 cell lithium-ion or lithium-polymer battery with built-in OTP. It provides highly accurate adjustable over-charge, over-discharge, over-current protection with adjustable detection delay by OTP. Current is detected by high precision external chip resistor. Which realizes accurate current detection over temperature. LC05551XA can control external FETs.

Function

- Highly Accurate Detection Voltage/Current at T_A = 25°C, V_{CC} = 3.8 V
- Over-charge Detection Voltage: 4.1 V to 4.55 V (5 mV steps)
- Over-charge Release Hysteresis: 0 V, 0.1 V, 0.15 V, 0.2 V
- Over-discharge Detection Voltage: 2.0 V to 3.3 V (50 mV step)
- Over-discharge Release Hysteresis: 0 V to 0.075 V (25 mV step)
- Over-discharge Release Hysteresis2: 0 V, 0.2 V, 0.3 V, 0.4 V
- Discharge Over-current Detection Voltage1: 3 mV to 30 mV (0.3 mV step)
- Discharge Over-current Detection Voltage2: 3 mV to 30 mV (0.6 mV step)
- Short Current Detection Voltage: 20 mV to 70 mV (5 mV step)
- Charge Over-current Detection Voltage: −30 mV to −3 mV (−0.6 mV step)
- Over-charge Detection Delay Time: 1024 ms
- Over-discharge Detection Delay Time: 32 ms, 64 ms, 128 ms, 256 ms
- Discharge Over-current Detection Delay Time1: 4 ms, 8 ms, 16 ms, 32 ms, 512 ms, 1024 ms, 2048 ms, 3482 ms
- Discharge Over-current Detection Delay Time2: 4 ms, 8 ms, 16 ms, 32 ms
- Short-current Detection Delay Time: 250 μs, 450 μs
- Charge Over-current Detection Delay Time: 4 ms, 8 ms, 16 ms, 128 ms
- 0 V Battery Charging: “Permission”
- Auto Wake-up Function: “Permission”
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Smart Phone
- Tablet
- Wearable Device

PART MARKING

510x = Specific Device Code
x = 1 or 2
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LC05551Z01XA	WLCSP8 (Pb−Free)	5000 / Tape & Reel
LC05551Z02XA	WLCSP8 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	VCC	Between PAC+ and VCC : R1 = 1 KΩ	−0.3 to 12.0	V
CS Terminal Input Voltage	VCS		−0.3 to 7	V
Short Delay TEST Terminal	SDT		−0.3 to 7	V
Reset terminal	RST		−0.3 to 7	V
VM Terminal Input Voltage	VVM		VCC − 24.0 to VCC + 0.3	V
CO Terminal Voltage	VCO		VCC − 24.0 to VCC + 0.3	V
DO Terminal Voltage	VDO		−0.3 to 7	V
Storage Temperature	T_{stg}		−55 to +125	°C
Operating Ambient Temperature	T_{opr}		−40 to +85	°C
Allowable Power Dissipation	P_d	Glass epoxy two-layer board. Board size 42 mm × 30 mm × 1.6 mm	0.6	W
Junction Temperature	T_j		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

EXAMPLE OF APPLICATION CIRCUIT

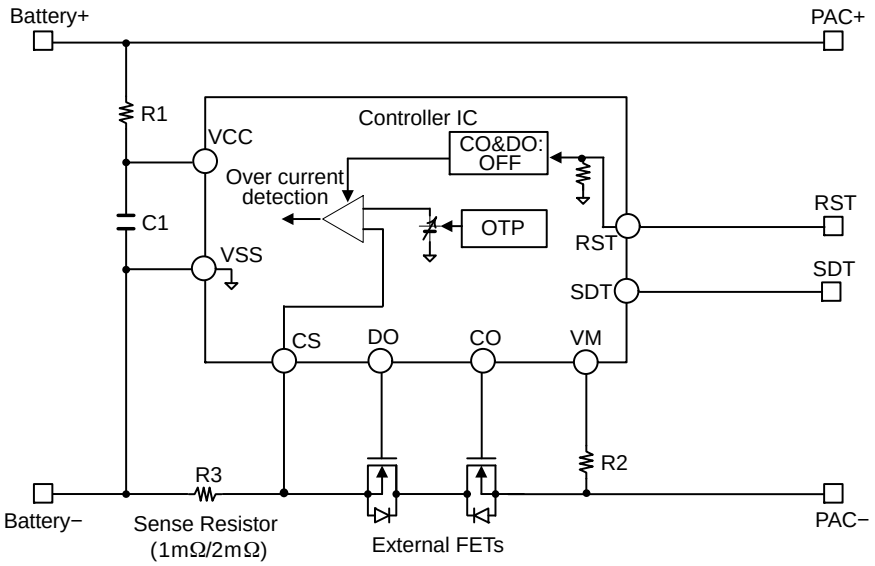


Figure 1. Example of Application Circuit

Components	Min	Recommended Value	Max	Unit	Description
R1	0.68	1	1.2	kΩ	Battery+ is filtered to VCC by R1 and C1
R2	0.1	1	2	kΩ	Protection from reverse connection of charger
C1	0.01	0.1	1.0	μF	Battery+ is filtered to VCC by R1 and C1
R3	1		20	mΩ	Sense resistor for over-current detection

ELECTRICAL CHARACTERISTICS (R1 = 1 kΩ, R2 = 1 kΩ, VCC = 3.8 V (Note 1))

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	TEST Circuit
DETECTION VOLTAGE								
Over−charge detection voltage	Vov	R1 = 1 kΩ	Ta = 25°C	Vov_set − 15	Vov_set	Vov_set + 15	mV	B
			Ta = −20 to 60°C	Vov_set − 20	Vov_set	Vov_set + 20		
Over−charge release voltage	Vovr1	R1 = 1 kΩ, VM < Vcocr & CS = 0	Ta = 25°C	Vovr_set − 30	Vovr_set	Vovr_set + 30	mV	B
			Ta = −20 to 60°C	Vovr_set − 55	Vovr_set	Vovr_set + 40		
	Vovr2	R1 = 1 kΩ, VM > Vcocr & CS = 0	Ta = 25°C	Vov_set − 20	Vov_set	Vov_set + 15	mV	I
			Ta = −20 to 60°C	Vov_set − 25	Vov_set	Vov_set + 20		
Over−discharge detection voltage	Vuv	R1 = 1 kΩ	Ta = 25°C	Vuv_set − 35	Vuv_set	Vuv_set + 35	mV	B
			Ta = −20 to 60°C	Vuv_set − 55	Vuv_set	Vuv_set + 55		
Over−discharge release voltage1	Vuvr1	R1 = 1 kΩ VM = 0 V	Ta = 25°C	Vuvr1_set − 35	Vuv_set	Vuv_set + 50	mV	B
			Ta = −20 to 60°C	Vuvr1_set − 55	Vuv_set	Vuv_set + 80		
Over−discharge release voltage2	Vuvr2	R1 = 1 kΩ VM = Open	Ta = 25°C	Vuvr2_set − 100	Vuvr2_set	Vuvr2_set + 100	mV	D
			Ta = −20 to 60°C	Vuvr2_set − 110	Vuvr2_set	Vuvr2_set + 110		
Discharge over−current detection voltage (primary protection)	Vdoc1	R2 = 1 kΩ	Ta = 25°C	Vdoc1 − 0.9	Vdoc1_set	Vdoc1 + 0.9	mV	F
			Ta = −20 to 60°C	Vdoc1 − 1.0	Vdoc1_set	Vdoc1 + 1.0		
Discharge over−current detection voltage2 (secondary protection)	Vdoc2	R2 = 1 kΩ	Ta = 25°C	Vdoc2 − 1.8	Vdoc2_set	Vdoc2 + 1.8	mV	F
			Ta = −20 to 60°C	Vdoc2 − 2.0	Vdoc2_set	Vdoc2 + 2.0		
Discharge over−current detection voltage (Short circuit)	Vshrt	R2 = 1 kΩ	Ta = 25°C	Vshrt_set − 5	Vshrt_set	Vshrt_set + 5	mV	F
			Ta = −20 to 60°C	Vshrt_set − 6	Vshrt_set	Vshrt_set + 6		
Dicharge over−current(short) release voltage	Vdocr	R2 = 1 kΩ CS = 0 V	Ta = 25°C	VCC - 1.1	VCC − 0.65	VCC − 0.2	V	A
			Ta = −20 to 60°C	VCC − 1.2	VCC − 0.65	VCC − 0.1		
Charge over−current	Vcoc	R2 = 1 kΩ	Ta = 25°C	Vcoc_set − 1.8	Vcoc_set	Vcoc_set + 1.8	mV	F
			Ta = −20 to 60°C	Vcoc_set − 2.0	Vcoc_set	Vcoc_set + 2.0		
Charge over−current	Vcocr	R2 = 1 kΩ CS = 0 V	Ta = 25°C	0.08	0.2	0.32	V	A
			Ta = −20 to 60°C	0.05	0.2	0.35		
RESET TERMINAL								
High−level input voltage	VIH		25°C	0.9*VCC			V	K
Low−level input voltage	VIL		25°C			0.1*VCC	V	K
High−level input leakage current	IIH	RST = 3.8 V	25°C		37		μA	L
Low−level input leakage current	IIL	RST = 0 V	25°C			0.1	μA	L
Factory−reset pulse width	Tw_res		25°C	33.6	48	62.4	ms	K
Factory−reset release pulse width	Twr_res		25°C	11.2	16	20.8	ms	K
INPUT VOLTAGE								
0 V battery charge permission charger voltage	Vchg	VCC - VM Vcc = VSS = 0 V	25°C			1.4	V	A
CURRENT CONSUMPTION								
Operating current	Icc	At normal state	25°C VCC = 3.8 V		3	6	μA	J
Stand−by current	Istb	At Stand−by state	25°C VCC = 2.0 V			0.95	μA	J
		Auto wake−up = enable						
RESISTANCE								
Internal resistance (VCC−VM)	Rvmu	VCC = 2.0 V VM = 0 V	25°C	150	300	600	kΩ	E
Internal resistance (VSS-VM)	Rvmd	VCC = 3.8 V VM = 0.1 V	25°C	5	10	20	kΩ	E
CO output resistance (High)	Rcoh	VCC = 3.8 V CO = 3.3 V CS = 0 V	25°C	6	12	24	kΩ	H

ELECTRICAL CHARACTERISTICS (R1 = 1 kΩ, R2 = 1 kΩ, VCC = 3.8 V (Note 1))

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	TEST Circuit
RESISTANCE								
CO output resistance (Low)	Rcol	VCC = 4.5 V CO = 0.5 V CS = 0 V	25°C	0.35	0.7	1.4	kΩ	H
DO output resistance (High)	Rdoh	VCC = 3.8 V DO = 3.3 V CS = 0 V	25°C	0.8	1.6	3.2	kΩ	G
DO output resistance (Low)	Rdol	VCC = 2.0 V CS = 0 V DO = 0.5 V	25°C	0.1	0.3	0.6	kΩ	G
DETECTION AND RELEASE DELAY TIME								
Over−charge detection delay time	Tov	VCC = 3 V to Vov_max VM = CS = 0 V	25°C	0.7	1.0	1.3	sec	B
			Ta = −20 to 60°C	0.6	1.0	1.4		
Over−charge release delay time	Tovr	VCC = Vov_max to 3 V VM = CS = 0 V	25°C	12.8	16	19.2	ms	B
			Ta = −20 to 60°C	11.2	16	20.8		
Over−discharge detection delay time	Tuv	VCC = 3 V to Vuv_min VM = CS = 0 V	25°C	Tuv_set x 0.8	Tuv_set	Tuv_set x 1.2	ms	B
			Ta = −20 to 60°C	Tuv_set x 0.65	Tuv_set	Tuv_set x 1.35		
Over−discharge release de-lay time	Tuvr	VCC = Vuv_min to 3 V VM = CS = 0 V	25°C	0.84	1.05	1.26	ms	B
			Ta = −20 to 60°C	0.68	1.05	1.42		
Discharge over−current detection delay time 1	Tdoc1	CS = 0 V to Vdoc1MAX VM = 0 V	25°C	Tdoc1_set x 0.8	Tdoc1_set	Tdoc1_set x 1.2	ms	F
			Ta = −20 to 60°C	Tdoc1_set x 0.7	Tdoc1_set	Tdoc1*_set x 1.3		
Discharge over−current detection delay time 2	Tdoc2	VM = 0 V to Vdoc2MAX VM = 0 V	25°C	Tdoc2_set x 0.8	Tdoc2_set	Tdoc2_set x 1.2	ms	F
			Ta = −20 to 60°C	Tdoc2_set x 0.7	Tdoc2_set	Tdoc2_set x 1.3		
Discharge over−current release delay time	Tdocr	VM = 3.8 V to 2.9 V CS = 0 V	25°C	3.2	4	4.8	ms	A
			Ta = −20 to 60°C	2.8	4	5.2		
Short−current detection delay time	Tshrt	CS = 0 V to VshrtMAX VM = 0	25°C	Tshrt_set x 0.7	Tshrt_set	Tshrt_set x 1.3	μs	F
			Ta = −20 to 60°C	Tshrt_set x 0.6	Tshrt_set	Tshrt_set x 1.4		
Charge over−current detection delay time	Tcoc	CS = 0 V to VcocMIN VM = 0	25°C	Tcoc_set x 0.8	Tcoc_set	Tcoc_set x 1.2	ms	F
			Ta = −20 to 60°C	Tcoc_set x 0.7	Tcoc_set	Tcoc_set x 1.3		
Charge over−current release delay time	Tcocr	VM = 0 V to VcocrMAX CS = 0 V	25°C	3.2	4	4.8	ms	F
			−Ta = −20 to 60°C	2.8	4	5.2		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. The specification in high temperature and low temperature are guaranteed by design.

TEST CIRCUITS

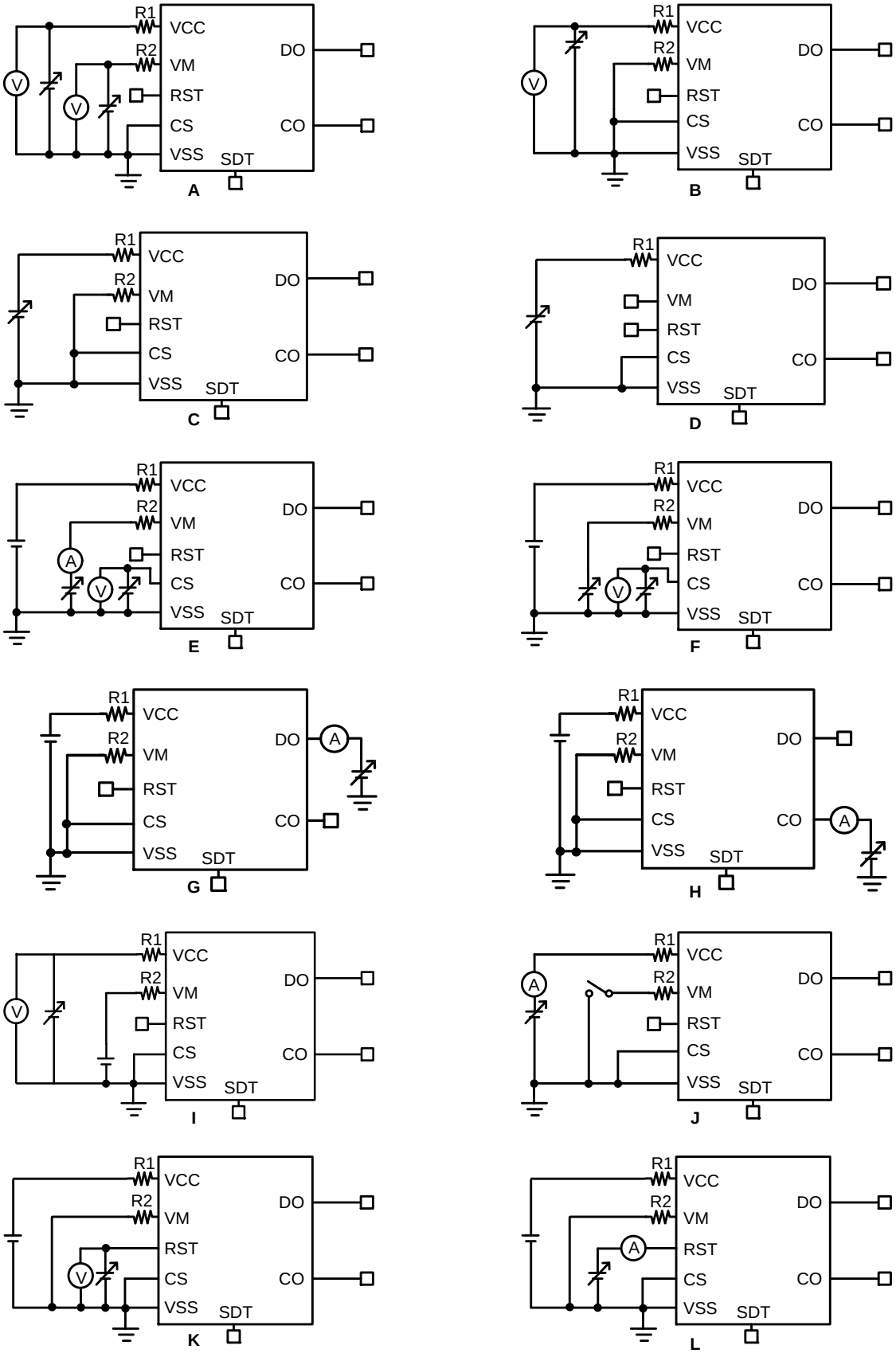


Figure 2. Test Circuits

Table 1. ADJUSTABLE PARAMETERS

Parameter	Unit	Range	Voltage
Vov	mV	4100 ~ 4600	5 mV step
Vovr	mV	Vov − Vovr_Hy	Vovr_Hy: 0, 100, 150, 200 (4 steps)
Vuv	mV	2100 ~ 3300	50 mV step
Vuvr2	mV	Vuv + Vuvr2_Hy	Vuvr2_Hy: 0, 200, 300, 400 (4 steps)
Vdoc1	mV	3 to 30	0.3 mV step
Vdoc2	mV	3 to 30	0.6 mV step
Vshrt	mV	20 to 70	5 mV step
Vcoc	mV	−30 to −3	0.6 mV step

Parameter	Unit	Delay
Tuv	ms	32, 64, 128, 256
Tdoc1	ms	4, 8, 16, 32, 512, 1024, 2048, 3482
Tdoc2	ms	4, 8, 16, 32
Tshrt	μs	250, 450
Tcoc	ms	4, 8, 16, 128

Table 2. SELECTION GUIDE

Device	Vov (mV)	Vovr1 (mV)	Vovr2 (mV)	Vuv (mV)	Vuvr1 (mV)	Vuvr2 (mV)	Vdoc1 (mV)	Vdoc2 (mV)	Vshrt (mV)	Vcoc (mV)	Tov (ms)	Tuv (ms)	Tdoc1 (ms)	Tdoc2 (ms)	Tshrt (μs)	Tcoc (ms)
LC05551Z01XA	4475	4325	4475	2500	2500	2900	7.5	10.0	25.0	−10.0	1024	64	3482	16	250	16
LC05551Z02XA	4445	4295	4445	2350	2350	2550	6.9	10.1	25.0	−7.8	1024	64	3482	16	250	16

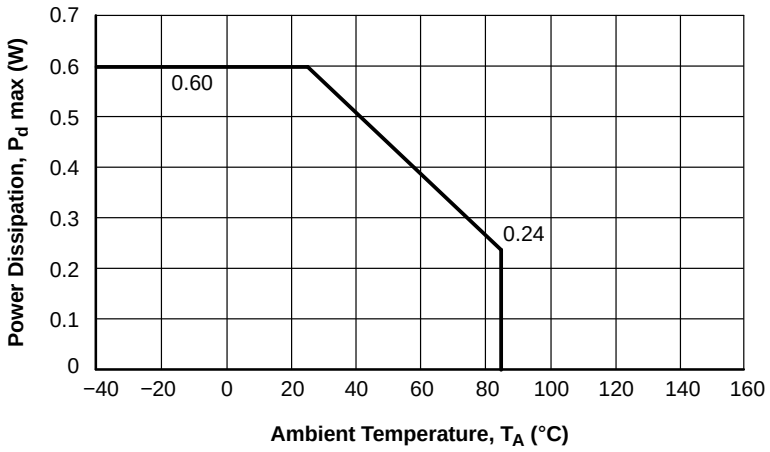


Figure 3. P_d max−T_A Graph

Table 3. PIN FUNCTION

Pin No.	Symbol	Pin Function
A1	VSS	VSS terminal
A2	VCC	VCC terminal
A3	CS	Overcurrent detection input terminal
A4	SDT	Input pin for function test − Open or VSS
B1	DO	Discharge FET control terminal
B2	CO	Charge FET control terminal
B3	VM	Charger negative voltage input terminal
B4	RST	Control pin for external charge FET and discharge FET

BLOCK DIAGRAM

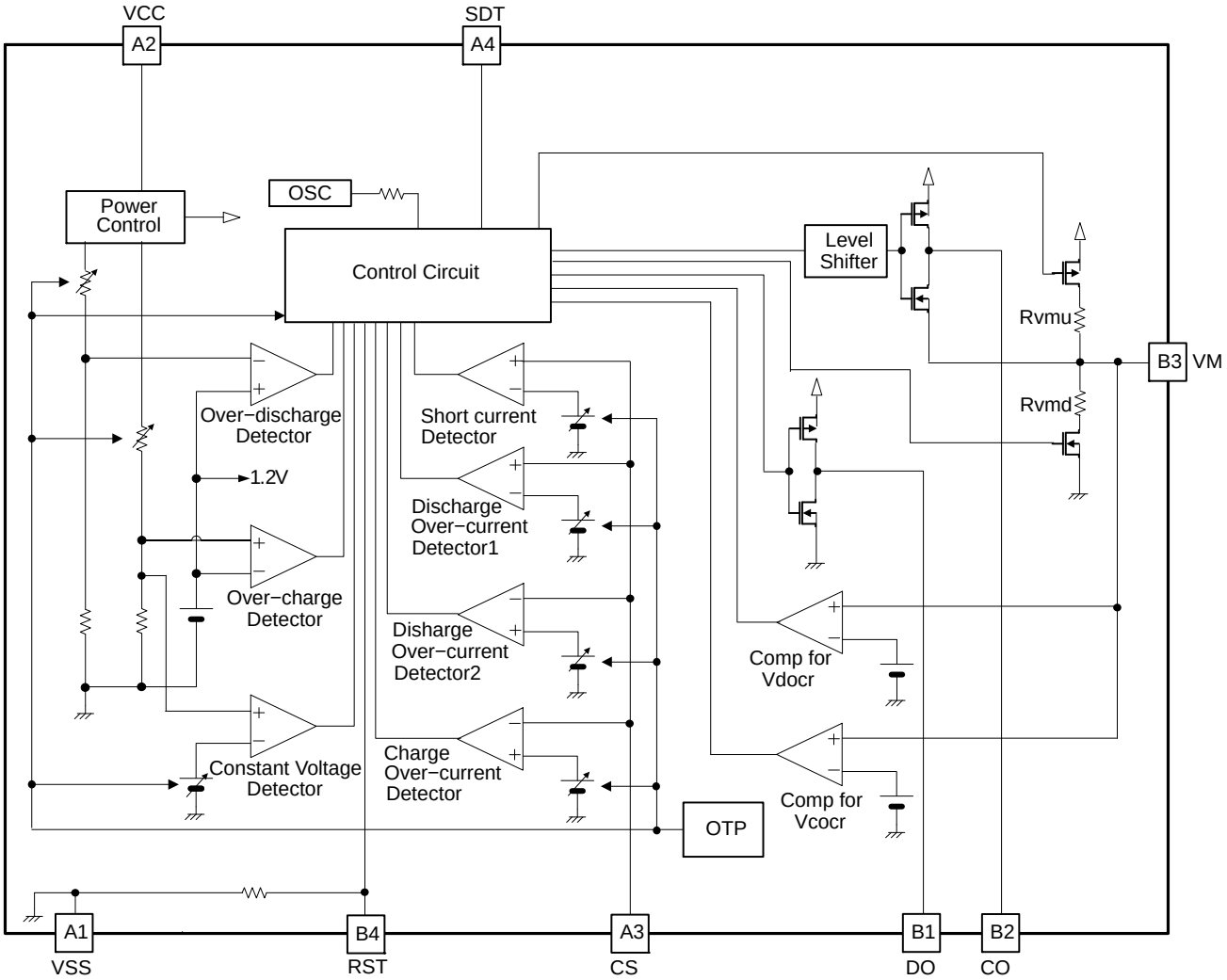


Figure 4. Block Diagram

DESCRIPTION OF OPERATION

The battery voltage is detected between VCC pin and VSS pin and the battery current is detected between VSS pin and CS pin.

(1) Normal State

- "VCC voltage" is between "over-discharge detection voltage (Vuv)", "over-charge detection voltage (Vov)", and "CS voltage" is between "charge over-current detection voltage (Vcoc)", "discharge over-current detection voltage (Vdoc)", and "VM voltage" is lower than "dicharge over-current (short) release voltage (Vdocr)". This is the normal state. Both CO and DO are high level output. Charge and discharge is allowed.

(2) Over-charging State

- "VCC voltage" is higher than or equal to "over-charge detection voltage (Vov)" for longer than "over-charge detection delay time (Tov)".
  This is the over-charging state, CO is low level output. Charge is prohibited.
- Release from Over-charging State 1
  "VM voltage" is lower than "charge over-current (short) release voltage (Vcocr)". Then "VCC voltage" is lower than "over-charge release voltage1 (Vovr1)" for longer than "over-charging release delay time (Tovr)".
- Release from Over-charging State 2
  "VM voltage" is higher than "charge over-current (short) release voltage (Vcocr)". Then "VCC voltage" is lower than "over-charge release voltage2 (Vovr2) for longer than "over-charge release delay time (Tovr)".

(3) Over-discharging State

- "VCC voltage" is lower than "over-discharge detection voltage (Vuv)" for longer than "over-discharge delay time (Tuv)".
  This is the over-discharging state, DO is low level output. Discharge is prohibited.
  During over-discharging state, VM pin is pulled up to Vcc by internal resistor (Rvmu) and circuits are shut down. The low power consumption is kept.
- Release from Over-discharging State 1
  Charger is connected, then "VCC voltage" goes higher than "over-discharge release voltage1 (Vuvr1)" for longer than "over-charge release delay time (Tuvr)".
- Release from Over-discharging State (with Auto Wake-up Feature) 2
  "VCC voltage" is higher than "over-discharge release voltage2 (Vuvr1)" without charger for longer than "over-charge release delay time (Tovr)".

(4) Discharging Over-current State

- Discharge Over-current Detection 1
  CS terminal is higher than or equal to "discharge over-current detection voltage (Vdoc1)" for longer than "discharge over-current detection delay time (Tdoc1)". DO is low level output. Discharge is prohibited.
- Discharge Over-current Detection 2
  CS terminal is higher than or equal to "discharge over-current detection voltage2 (Vdoc2)" for longer than "discharge over-current detection delay time 2 (Tdoc2)". DO is low level output. Discharge is prohibited.
- Discharge Over-current Detection (Short Circuit)
  CS terminal is higher than or equal to "discharge over-current detection voltage (Short circuit) (Vshrt)" for longer than "short-current detection delay time (Tshrt)". DO is low level output. Discharge is prohibited.
  During discharging over-current state, VM pin is pulled down to Vss by internal resistor (Rvmd).
- Release from Discharging Over-current State
  "CS voltage" goes lower than "discharge over-current detection voltage (Vdoc1)" and VM voltage goes lower than "discharge over-current (short) release voltage (Vdocr)" for longer than "discharge over-current release delay time (Tdocr)".

(5) Charging Over-current State

- "CS voltage" goes lower than or equal to "charge over-current detection voltage (Vcoc) for longer than "charge over-current detection delay time (Tcoc)".
  This is the charging over-current state, CO is low level output. Charge is prohibited.
- Release from charging over-current state
  "CS voltage" goes lower than "charge over−current detection voltage (Vcoc)" and "VM voltage" goes lower than "charge over-current release voltage (Vcocr)" for longer than "discharge over-current release delay time (Tcocr)".

(6) 0 V Battery Charging

- When the Battery voltage is lower than or equal to "0 V battery charge permission voltage (Vchg)", charge is allowed if charger voltage is higher than or equal "0 V battery charge permission voltage (Vchg)". CO is fixed by the "VCC voltage".

(7) Reset State

- RST voltage is higher than or equal to high level input voltage (VIH) for longer than the delay time of factory−reset pulse (Tw_res).
  This is the reset state, both CO and DO are low level output. Charge and discharge are prohibited.
- Release from Reset State
  RST voltage is lower than or equal to low level input voltage (VIL) for longer than the delay time of factory reset release pulse (Tw_res).
- Under reset state, any protection doesn't work. Under both charging over current state and discharging over current state, reset function doesn't work.

TIMING CHARTS

Over Charge Voltage and Charge Over Current

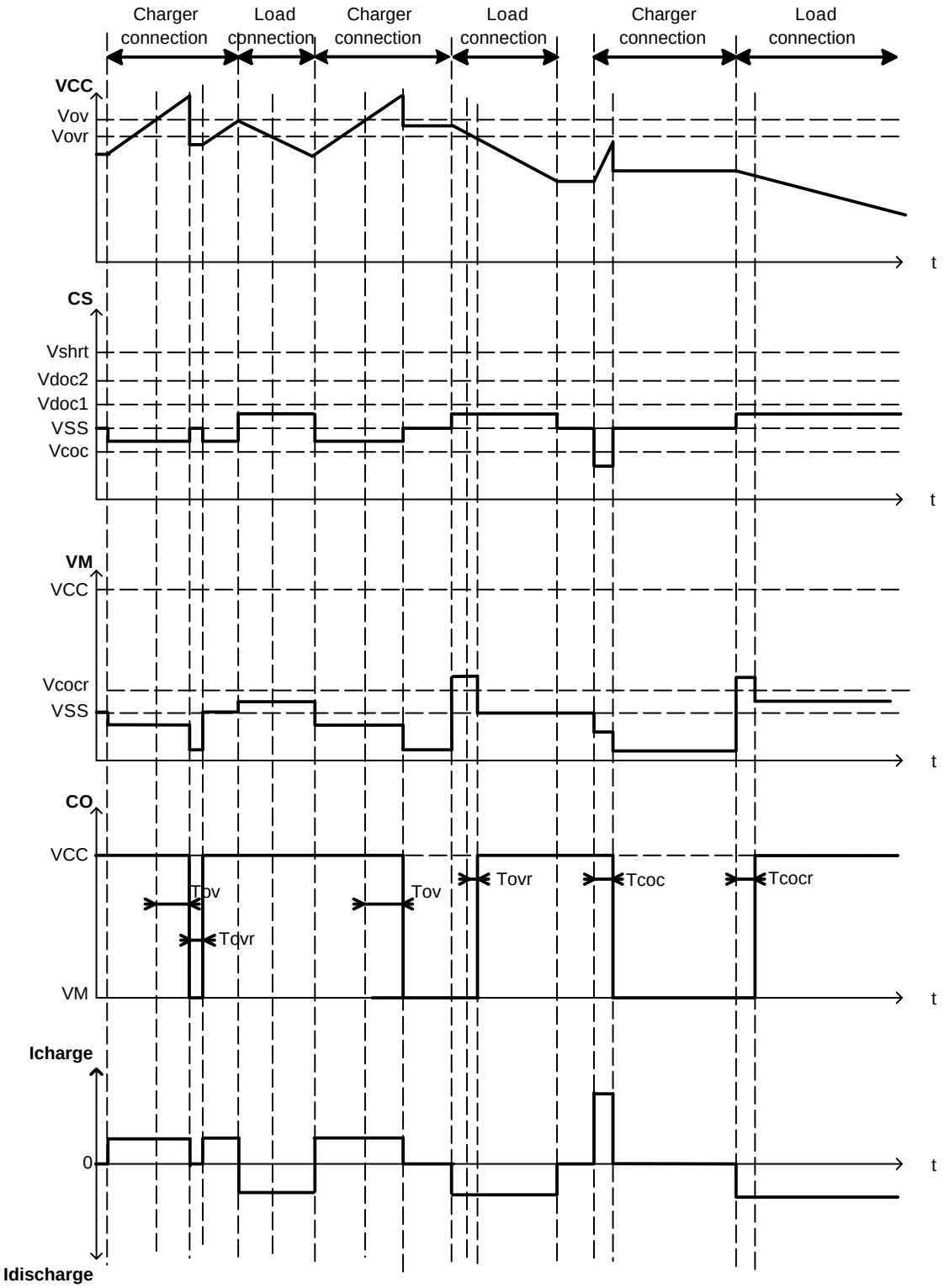


Figure 5. Over Charge Voltage and Charge Over Current

Over Discharge Detection and Release (with/without Charger)

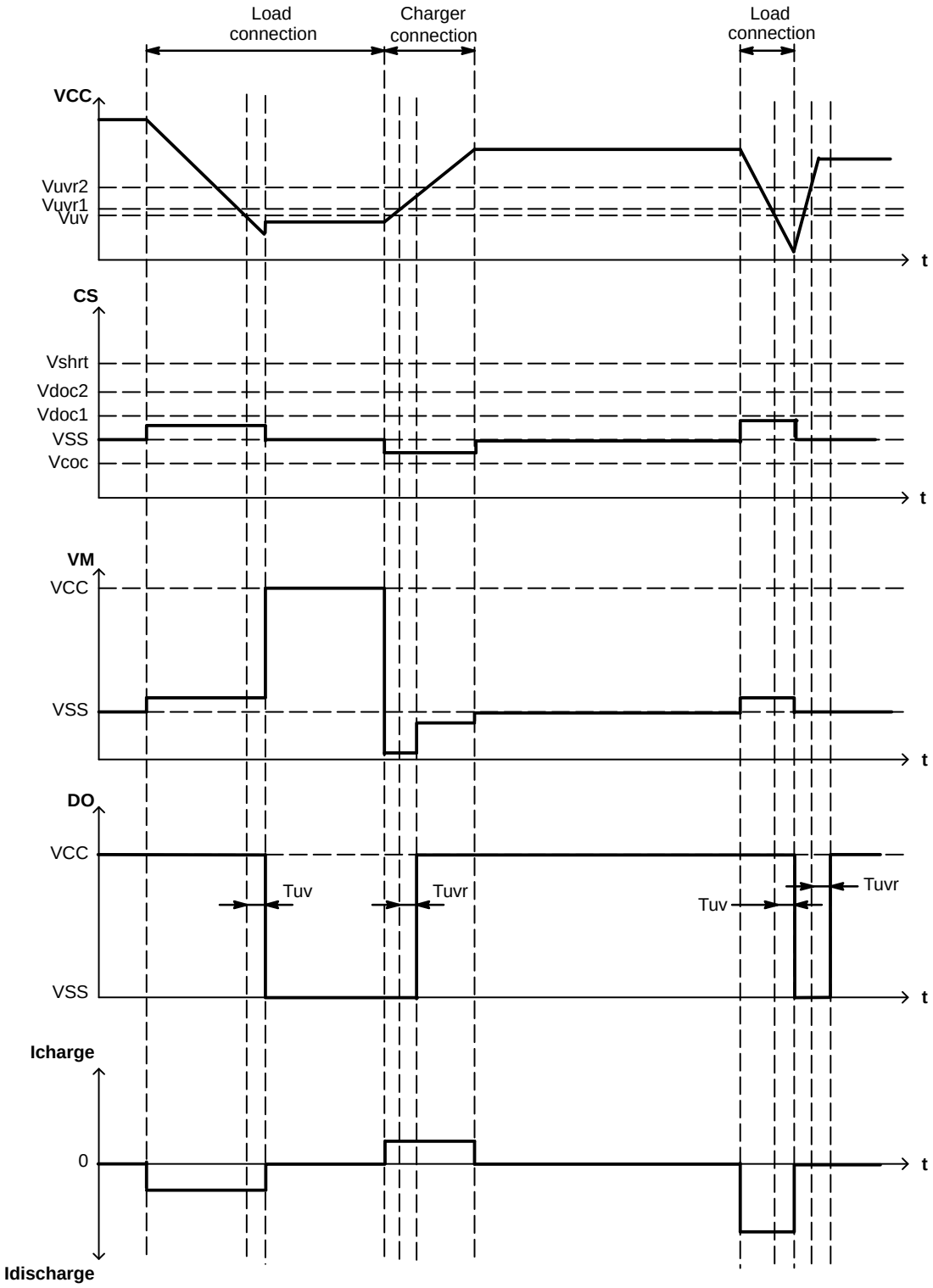


Figure 6. Over Discharge Detection and Release (with/without Charger)

Discharge Over Current and Short Current Detection and Release

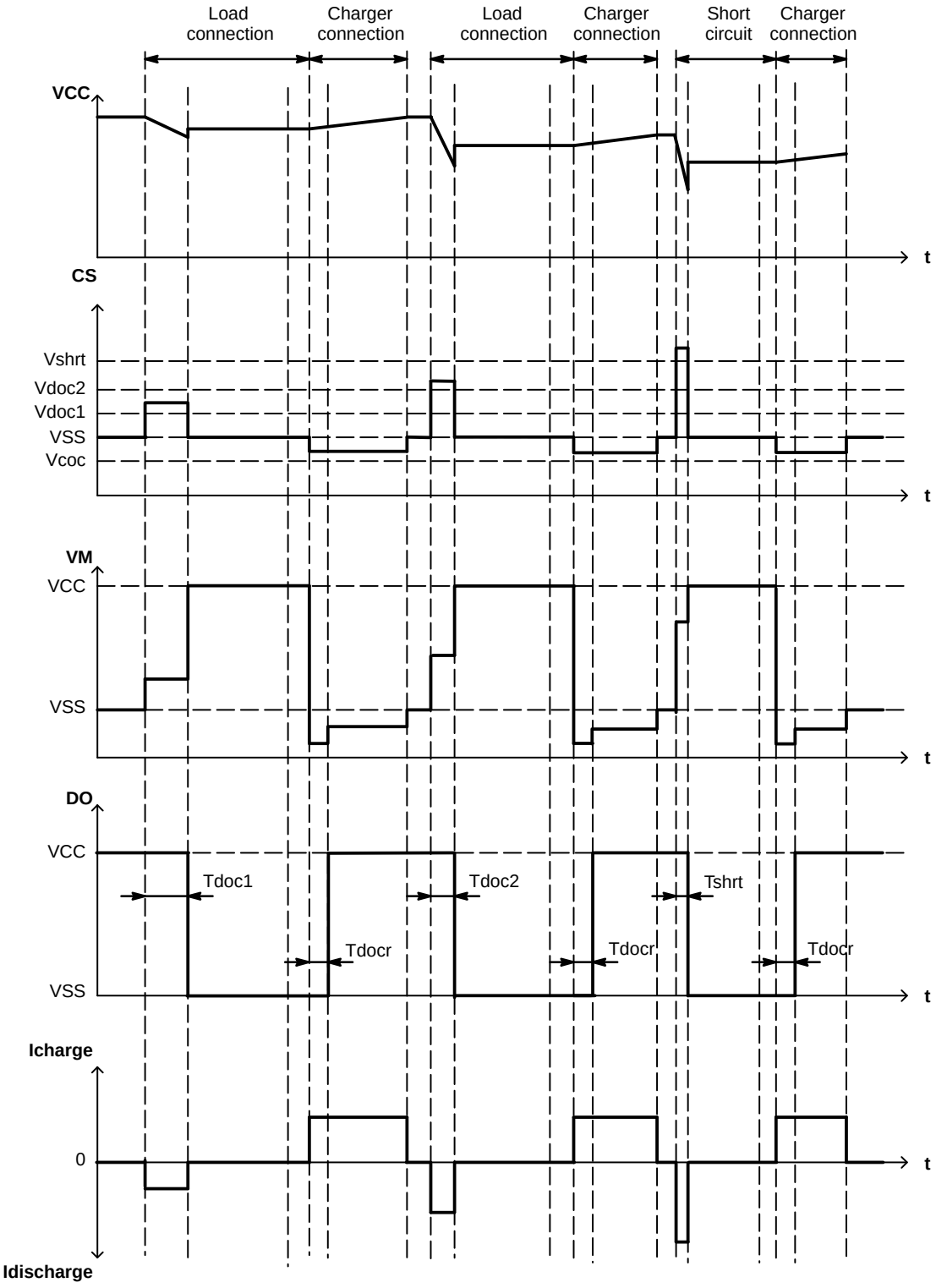
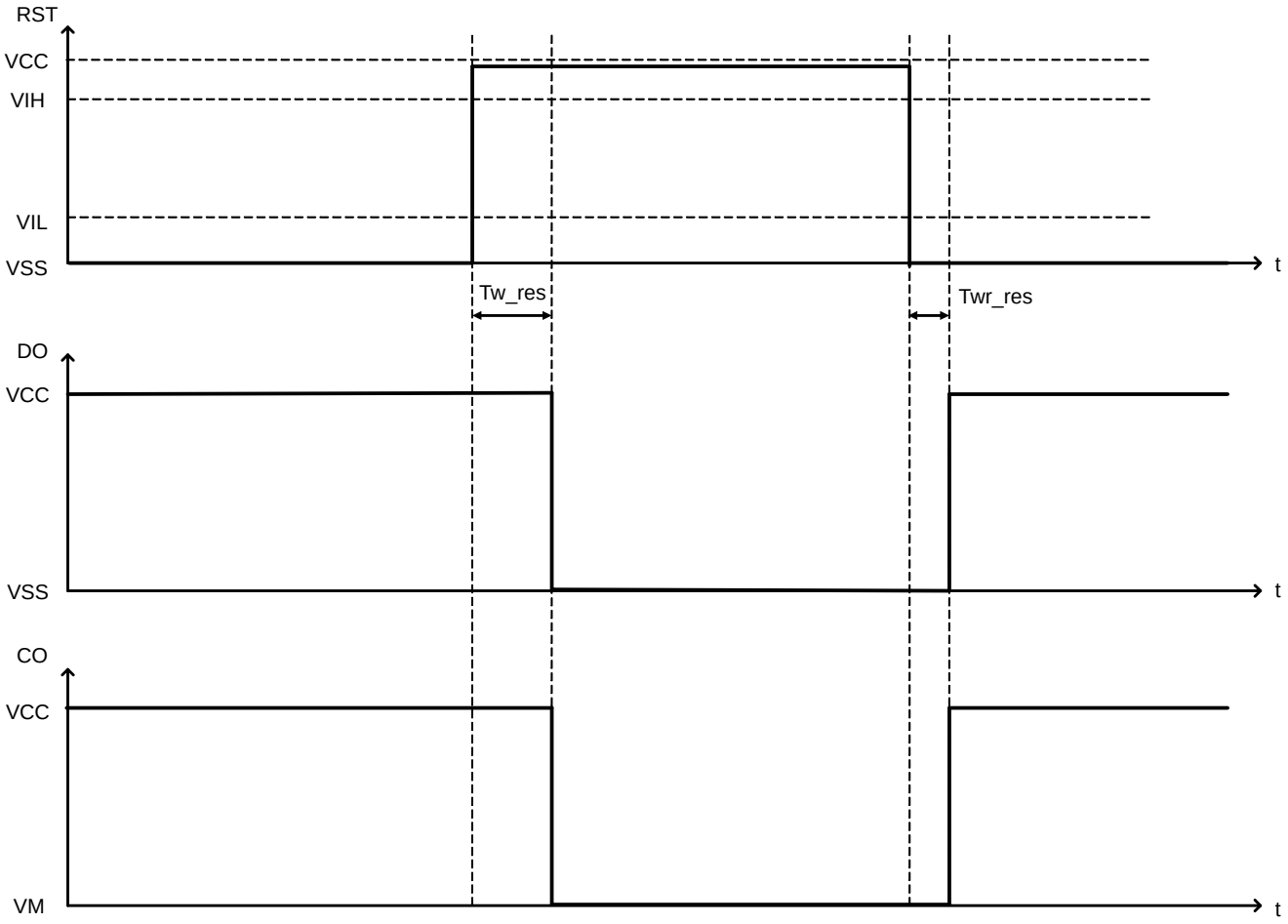


Figure 7. Discharge Over Current and Short Current Detection and Release

Reset State



CHARACTERISTICS OF LC05551Z01XA (TYPICAL DATA)

(1) Current Consumption and Protection Detection Voltage

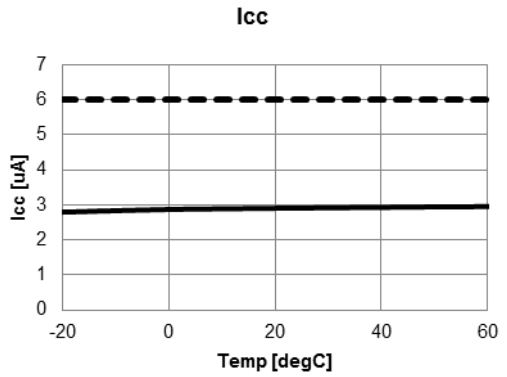


Figure 8. I_{CC} vs. Temperature

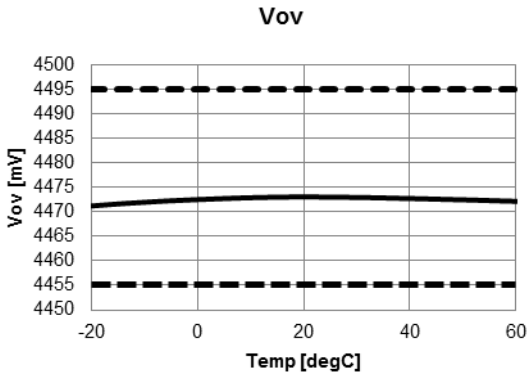


Figure 9. V_{OV} vs. Temperature

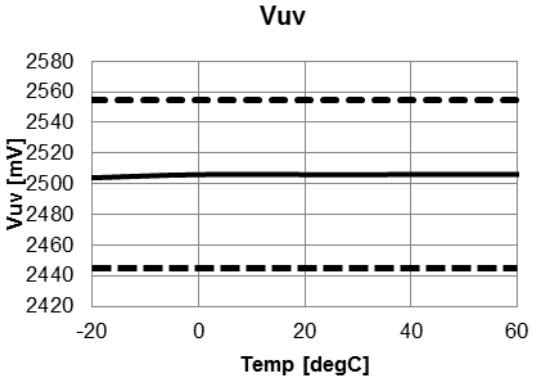


Figure 10. V_{UV} vs. Temperature

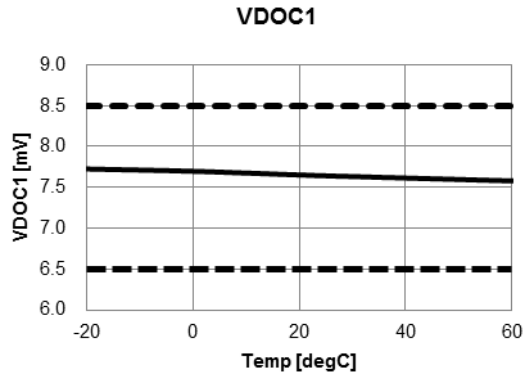


Figure 11. V_{DOC1} vs. Temperature

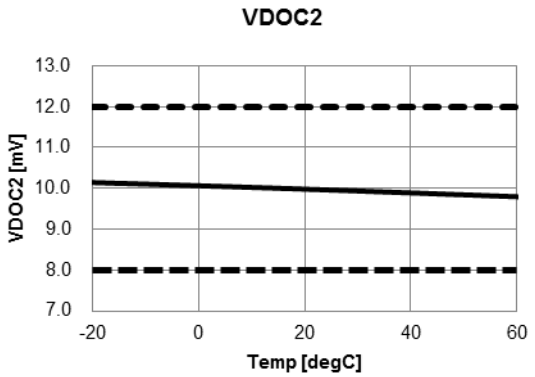


Figure 12. V_{DOC2} vs. Temperature

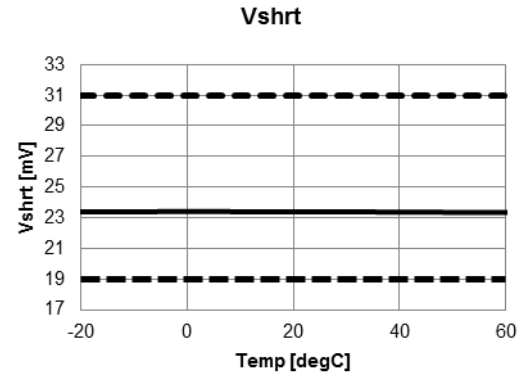


Figure 13. V_{SHRT} vs. Temperature

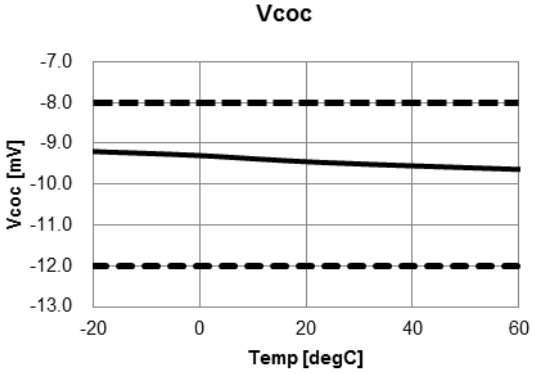


Figure 14. V_{COC} vs. Temperature

CHARACTERISTICS OF LC05551Z04XA (TYPICAL DATA)

(2) Protection Detection Delay Time

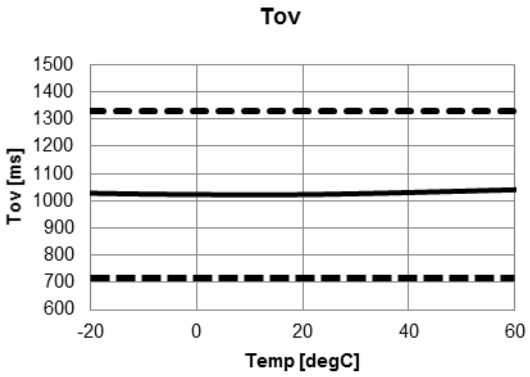


Figure 15. T_{OV} vs. Temperature

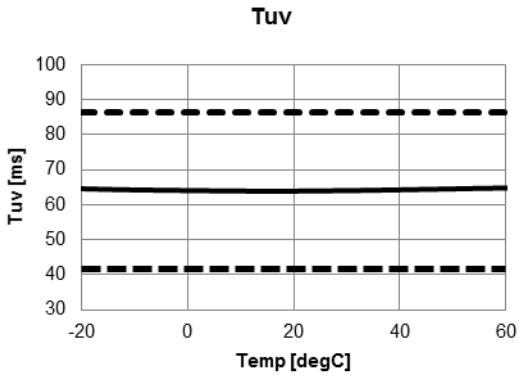


Figure 16. T_{UV} vs. Temperature

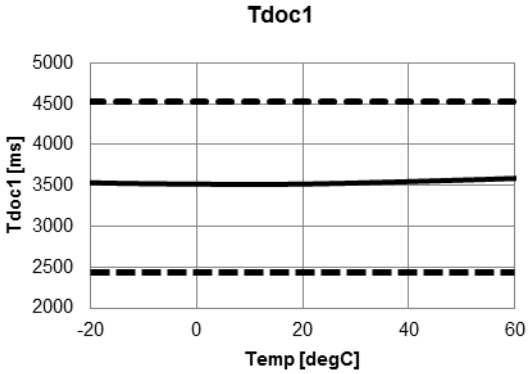


Figure 17. T_{DOC1} vs. Temperature

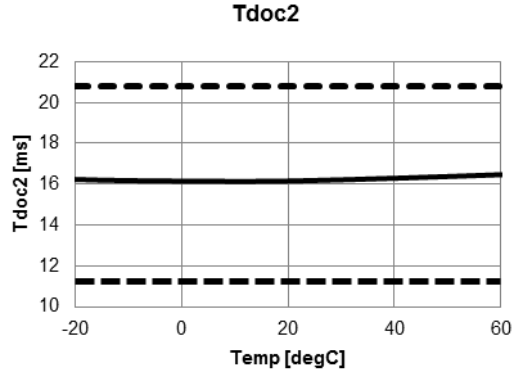


Figure 18. T_{DOC2} vs. Temperature

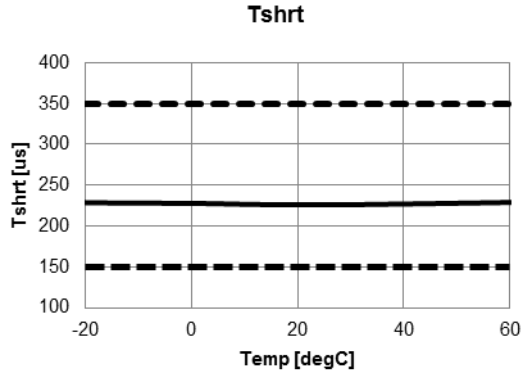


Figure 19. T_{SHRT} vs. Temperature

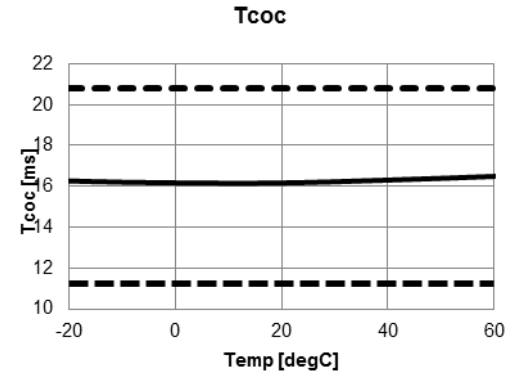


Figure 20. T_{COC} vs. Temperature

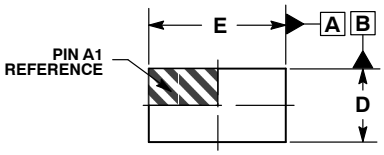
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

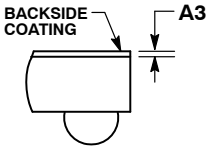
SCALE 4:1

WLCSP8 0.81x1.51x0.40
CASE 567UN
ISSUE O

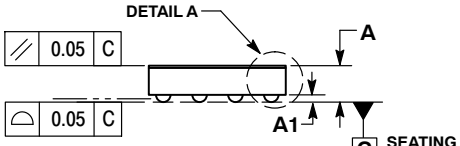
DATE 02 JUN 2017



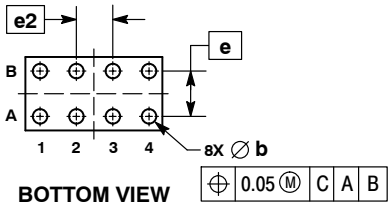
TOP VIEW



DETAIL A

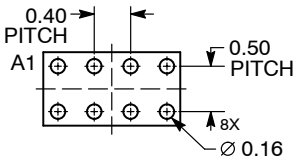


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	0.40
A1	0.05	0.08	0.11
A3		0.025 REF	
b	0.11	0.16	0.21
D	0.76	0.81	0.86
E	1.46	1.51	1.56
e		0.50 BSC	
e2		0.40 BSC	

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WLCSP8 0.81X1.51X0.40		PAGE 1 OF 1

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