



# **TFT LCD Module**

## **Product Specification**

### **DT035BTFT-PTS1**

**3.5" (320(RGB) x 240 DOTS) TFT Module  
with Capacitive Touch Screen**

October 28, 2016

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**Revision Record**

<b>REV</b>	<b>CHANGES</b>	<b>DATE</b>
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## 1. Scope

This data sheet is to introduce the specification of DT035BTFT-PTS1, active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC, capacitive touch panel and a backlight unit. The 3.5" display area contains 320 (RGB) x 240 pixels.

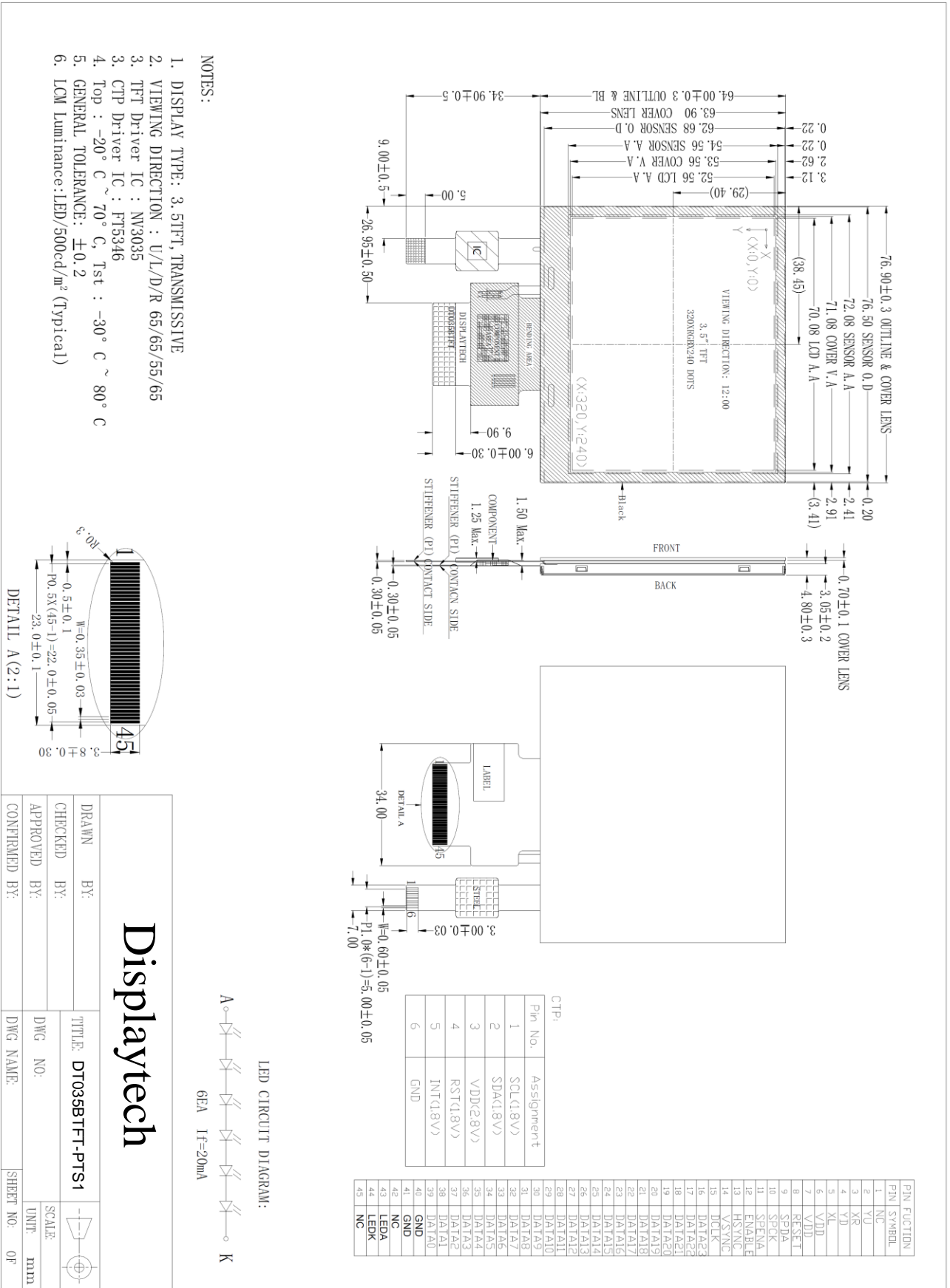
## 2. Application

Digital equipment which need color display, mobile phone, mobile navigator/video systems.

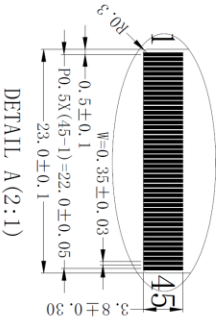
## 3. General Information

Item	Contents	Unit
Size	3.5	inch
Resolution	320(RGB) x 240	/
Interface	RGB	/
Technology Type	a-Si TFT	/
Pixel Configuration	R.G.B. Vertical Stripe	/
Pixel Pitch	0.219 x 0.219	mm
Outline Dimension (W x H x D)	76.90 x 64.00 x 4.8	mm
Active Area	70.08 x 52.56	mm
Display Mode	Transmissive, Normally White	/
Backlight Type	LED	/
Driver IC for PCAP	FT5346	
Weight	TBD	g

### 4. Outline Drawing



- NOTES:
1. DISPLAY TYPE: 3.5TFT, TRANSMISSIVE
  2. VIEWING DIRECTION : U/L/D/R 65/65/55/65
  3. TFT Driver IC : NV3035
  3. CTP Driver IC : FT5346
  4. Top : -20° C ~ 70° C, Tst : -30° C ~ 80° C
  5. GENERAL TOLERANCE: ±0.2
  6. LCM Luminance: LED/500cd/m<sup>2</sup> (Typical)

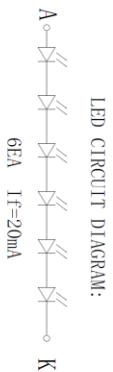


CTP:

Pin No.	Assignment
1	SCL(1.8V)
2	SDA(1.8V)
3	VDD(2.8V)
4	RST(1.8V)
5	INT(1.8V)
6	GND

PIN	FUNCTION
1	NC
2	YU
3	XR
4	YD
5	XL
6	VDD
7	VDD
8	RESET
9	SPDA
10	SPCK
11	SPENA
12	ENABLE
13	HSYNC
14	VSYNC
15	DCCLK
16	DATA23
17	DATA2
18	DATA21
19	DATA20
20	DATA19
21	DATA18
22	DATA17
23	DATA16
24	DATA15
25	DATA14
26	DATA13
27	DATA12
28	DATA11
29	DATA10
30	DATA9
31	DATA8
32	DATA7
33	DATA6
34	DATA5
35	DATA4
36	DATA3
37	DATA2
38	DATA1
39	DATA0
40	GND
41	NC
42	NC
43	LEDA
44	LEDB
45	NC



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APPROVED BY:	DWG NAME:	SHEET NO:	OF
CONFIRMED BY:			

## 5. Interface Signals

No	Symbol	Description	Remark
1 ~ 5	NC	No connection	
6	VDD	Power supply	
7	VDD	Power supply	
8	RESET	Global reset pin	
9	SPDA	SPI Serial data input/output	
10	SPCK	SPI interface clock	
11	SPENA	Serial port data enable signal	
12	ENABLE	Data enable input	
13	HSYNC	Horizontal sync input	
14	VSYNC	Vertical sync input	
15	DCLK	Data clock	
16 ~ 39	DATA23 ~ DATA0	Data bit	
40	GND	Power ground	
41	GND	Power ground	
42	NC	No connection	
43	LEDA	LED backlight (Anode)	
44	LEDK	LED backlight (Cathode)	
45	NC	No connection	

### CTP signal interface

No.	Symbol	Function
1	SCL	Clock for the data input
2	SDA	Data input
3	VDD	Power supply
4	RESET	Reset
5	INT	Interrupt output pin
6	GND	Ground

## 6. Absolute Maximum Ratings

### 6.1 Electrical absolute maximum ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power supply voltage	VDD	-0.3	5.0	V	

### 6.2 Environment conditions

Parameter	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	+70	°C	
Storage Temperature	TSTG	-30	+80	°C	

## 7. Electrical Specifications

### 7.1 Electrical characteristics

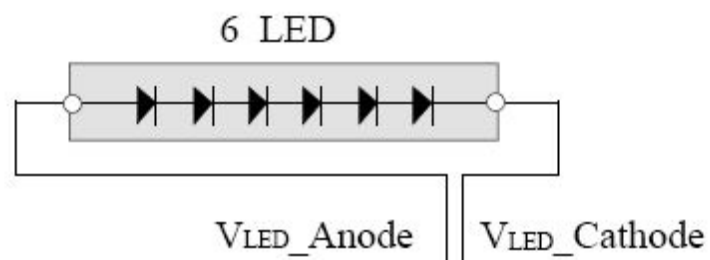
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply voltage	VDD	3	3.3	3.6	V	
Input signal voltage	Low level	VIL	GND	-	0.1xVDD	V
	High level	VIH	0.8xVDD	-	VDD	V
TFT Common electrode Voltage	VcomH	2.5	-	4.5	V	
TFT Gata ON voltage	VcomL	-3	-	0	V	
TFT Gata OFF voltage	VcomH			15	V	
	VcomL	-10			V	

### 7.2 LED backlight

Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward current	IF	-	20	25	mA	
Forward voltage	VF	16.8	19.2	21.6	V	
LED life time	-	-	25,000	-	Hr	

The figure below shows the connection of LED



## 8. Command / AC Timing

### 8.1 AC Electrical Characteristics

Test Condition: (VDD=VDDP=3.3V, VDDA=5.0V, GND=GNDA=GNDP=0V, TA= 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>System Operation Timing</b>						
VDD power source slew time	T <sub>POR</sub>			1000	us	From 0V to 90% VDD
RSTB active pulse width	T <sub>RSTB</sub>	40			us	VDD = 3.3V
<b>Input Output Timing</b>						
CLKIN clock time	T <sub>clk</sub>	33.3/125	-	-	ns	Please refer to timing table(p.32)
HSD to CLKIN	T <sub>hc</sub>	-	-	1	CLKIN	
HSD width	T <sub>hwh</sub>	1	-	-	CLKIN	
VSD width	T <sub>vwh</sub>	1	-	-	Th	
HSD period time	T <sub>h</sub>	60	63.56	67	us	
VSD setup time	T <sub>vst</sub>	8	-	-	ns	
VSD hold time	T <sub>vhd</sub>	10	-	-	ns	
HSD setup time	T <sub>hst</sub>	8	-	-	ns	
HSD hold time	T <sub>hhd</sub>	10	-	-	ns	
Data set-up time	T <sub>dsu</sub>	8	-	-	ns	DIN[23:0] to CLKIN
Data hold time	T <sub>dhd</sub>	10	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	T <sub>eed</sub>	12	-	-	ns	DEN to CLKIN
Time that VSD to 1 <sup>st</sup> line data input	T <sub>vs</sub>	2	13	127	Th	@CCIR601 / 8bit RGB HV mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that CCIR_V to 1 <sup>st</sup> line data input	T <sub>vs</sub>	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that CCIR_V to 1 <sup>st</sup> line data input	T <sub>vs</sub> 17 25 33 Th					@CCIR656 PAL mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that VSD to 1 <sup>st</sup> line data input	T <sub>vs</sub>	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Source output stable time 1	T <sub>st</sub>	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	T <sub>gst</sub>	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	T <sub>cst</sub>	-	4	8	us	96% final, CL=33nF, RL=100ohm
<b>3-wire serial communication AC timing</b>						
Serial clock	T <sub>spck</sub>	320	-	-	ns	
SPCK pulse duty		40	50	60	%	T <sub>ckh</sub> / T <sub>spck</sub>
Serial data setup time	T <sub>isu</sub>	120	-	-	ns	
Serial data hold time	T <sub>ihd</sub>	120	-	-	ns	
Serial clock high/low	T <sub>ckh/l</sub>	120	-	-	ns	
Chip select distinguish	T <sub>cd</sub>	1	-	-	us	
SPENB to VSD	T <sub>cv</sub>	1	-	-	us	
SPENB input setup time	T <sub>eck</sub>	150	-	-	ns	
SPENB input hold time	T <sub>cke</sub>	150	-	-	ns	

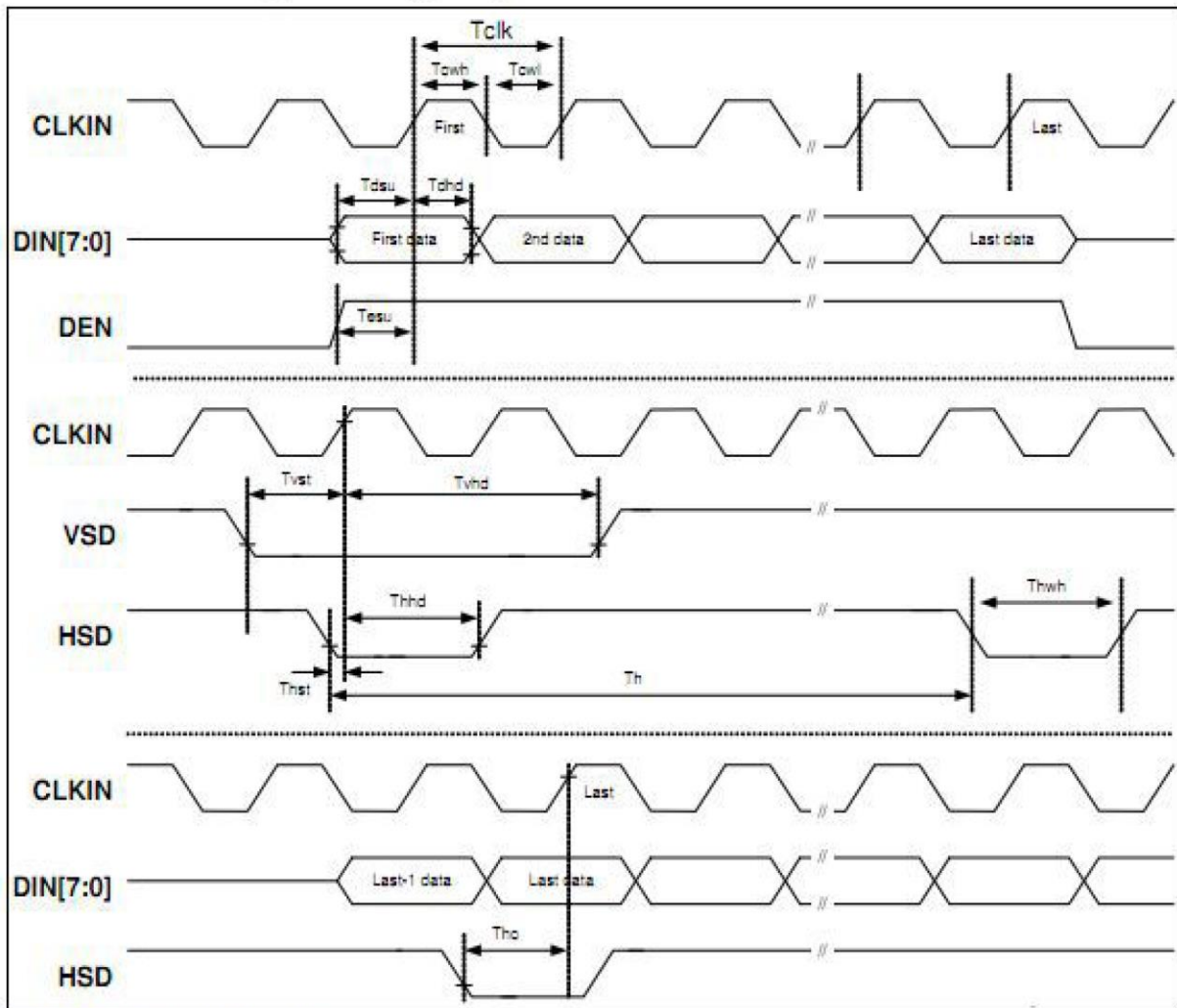
### 8.2 24 Bit RGB Mode (@ SEL[3:0] = 1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	F <sub>clk</sub>	6.1	6.4	8.0	MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	T <sub>clk</sub>	125	156	164	ns	
CLKIN pulse duty	T <sub>cwh</sub>	40	50	60	%	T <sub>clk</sub>
Time that HSD to 1 <sup>st</sup> data input(NTSC)	T <sub>hs</sub>	40	70	255	CLKIN	DDLY = 70, Offset = 0 (fixed)

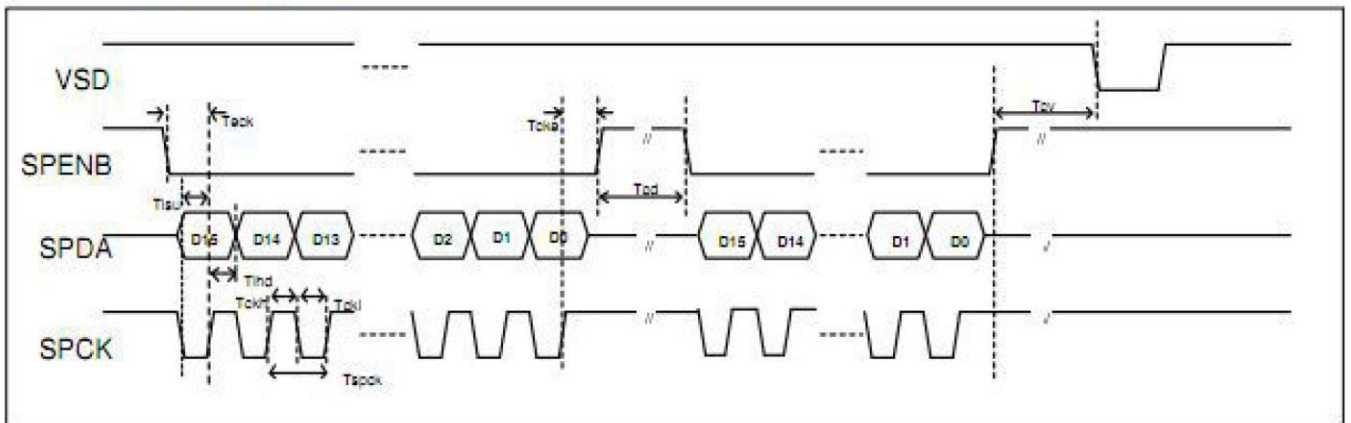


### 8.3 Timing Diagram

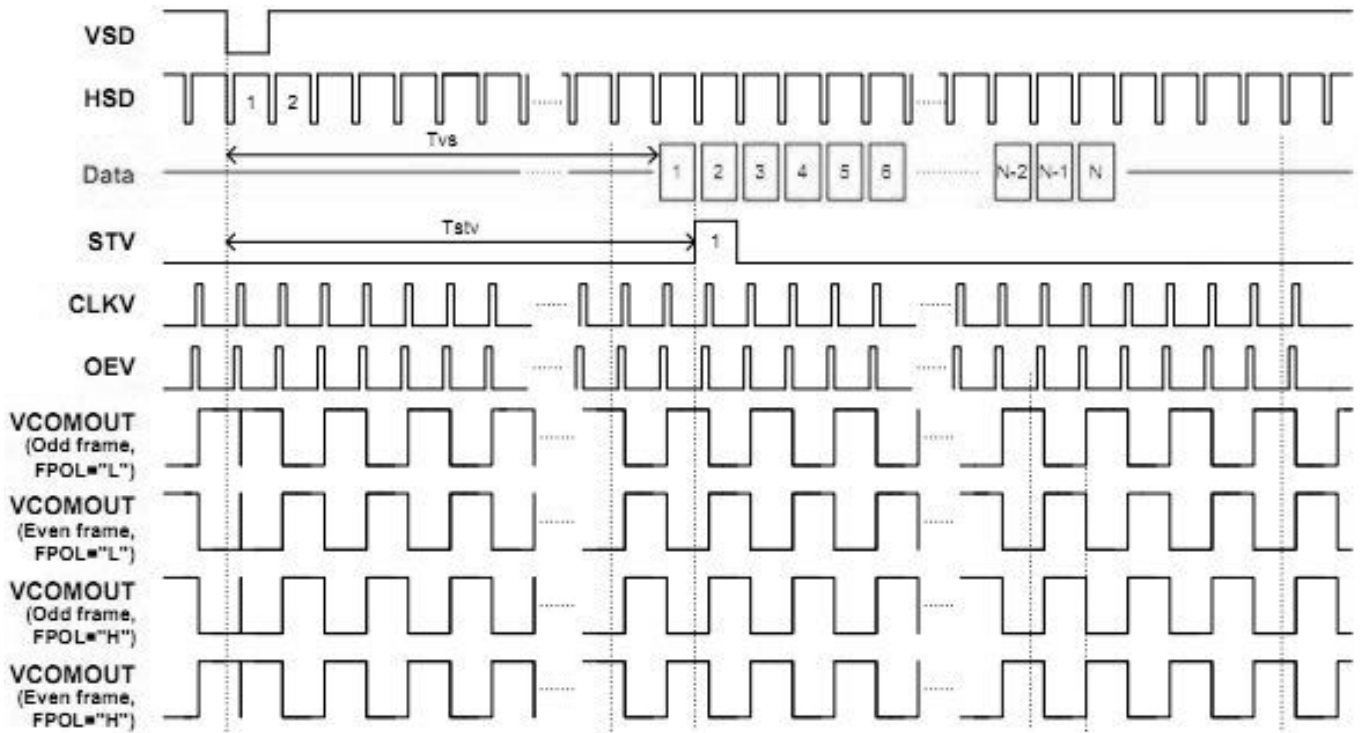
#### Clock and Data Input Timing Diagram



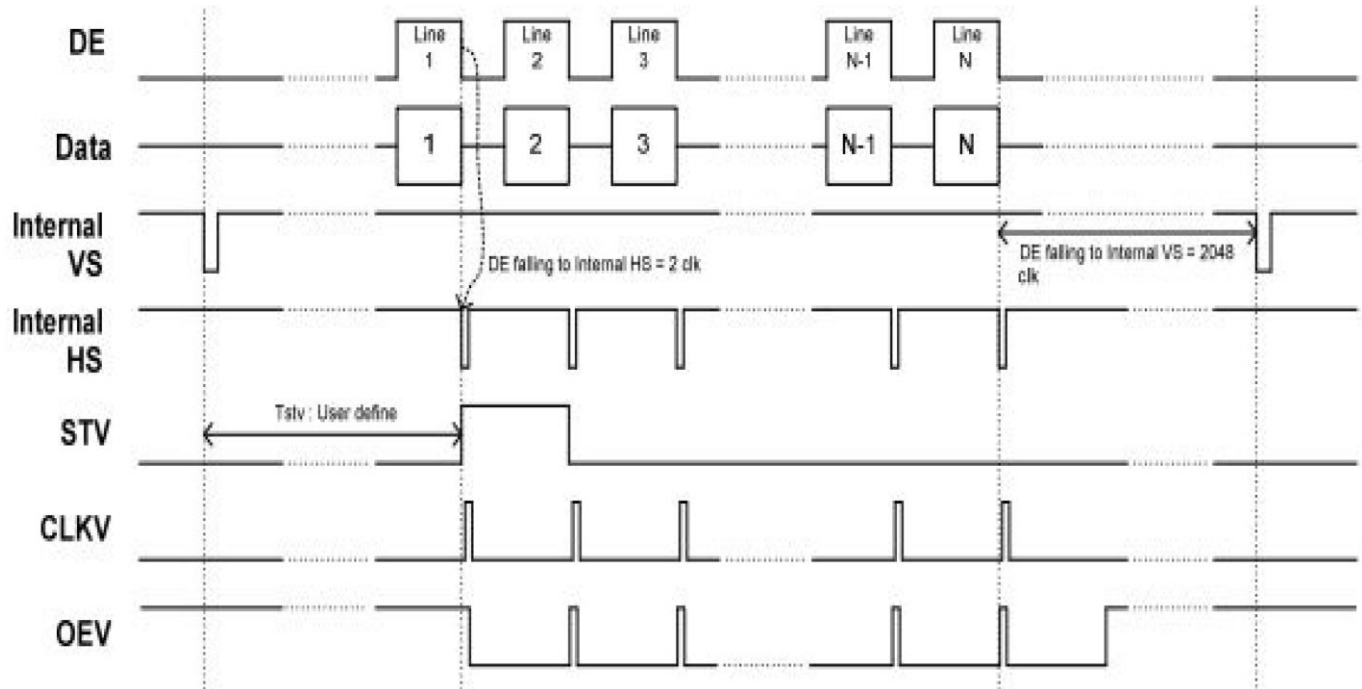
#### 3-Wire Timing Diagram



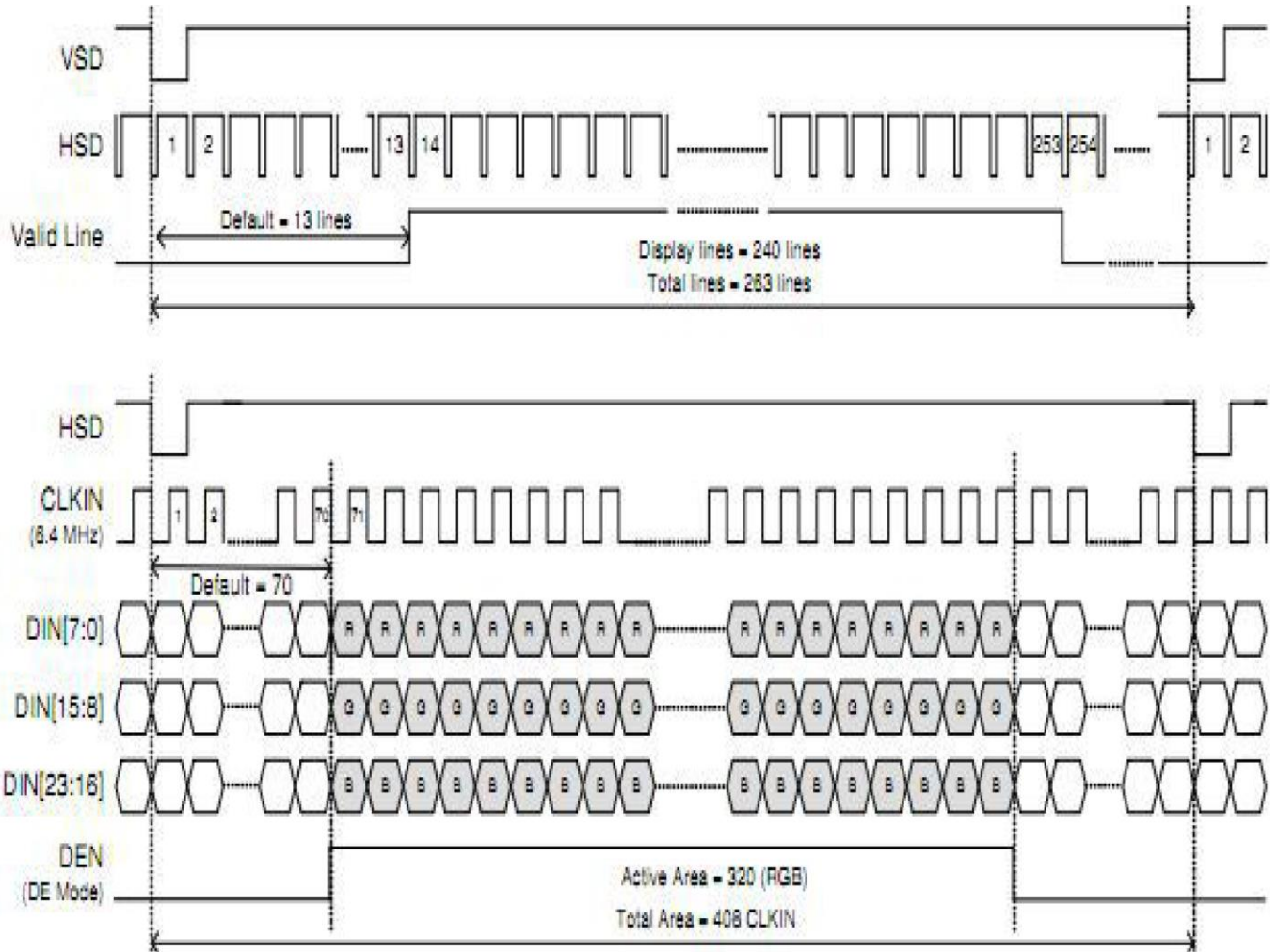
8.4 Vertical Timing Diagram (HV Mode)



8.5 Vertical Timing Diagram (DE Mode)



8.6 Input Data Timing (24 bit RGB mode for 960 x 240 @ SEL[3:0] = 1100b)



9. Optical Specification

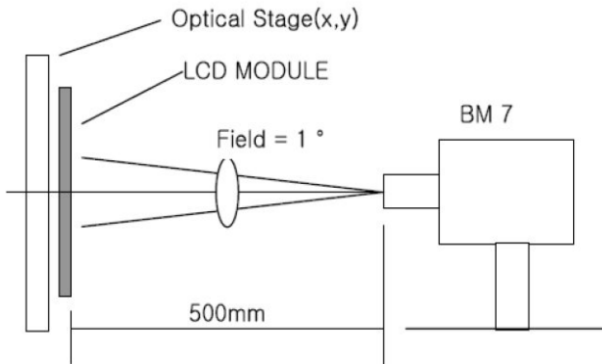
Ta=25°C

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remark
Contrast ratio	CR	$\theta=0^\circ$	350	500	-		Note 1, 2
Response time	Tr / Tf	25°C	-	10	-	ms	Note 1, 3
View angles	$\theta T$	CR $\geq$ 10	-	65	-	Degree	Note 4
	$\theta B$		-	55	-		
	$\theta L$		-	65	-		
	$\theta R$		-	65	-		
Chromaticity	Red	x	-	0.51	-	Note 1, 5	
		y	-	0.34	-		
	Green	x	-	0.31	-		
		y	-	0.56	-		
	Blue	x	-	0.15	-		
		y	-	0.14	-		
White	x	Brightness is on	-	0.28	-		
	y		-	0.33	-		
NTSC			50	60		%	Note 5
Luminance	L		-	480	-	cd/m <sup>2</sup>	Note 1, 6
Uniformity	U		75	80	-	%	Note 1, 7

Note 1: Definition of optical measurement system.

Temperature = 25°C(±3°C)

LED back-light: ON, Environment brightness < 150 lx

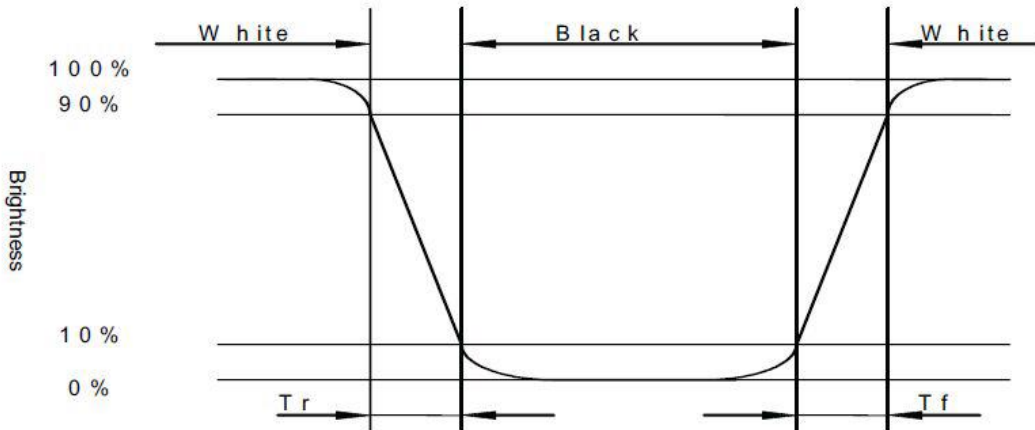


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

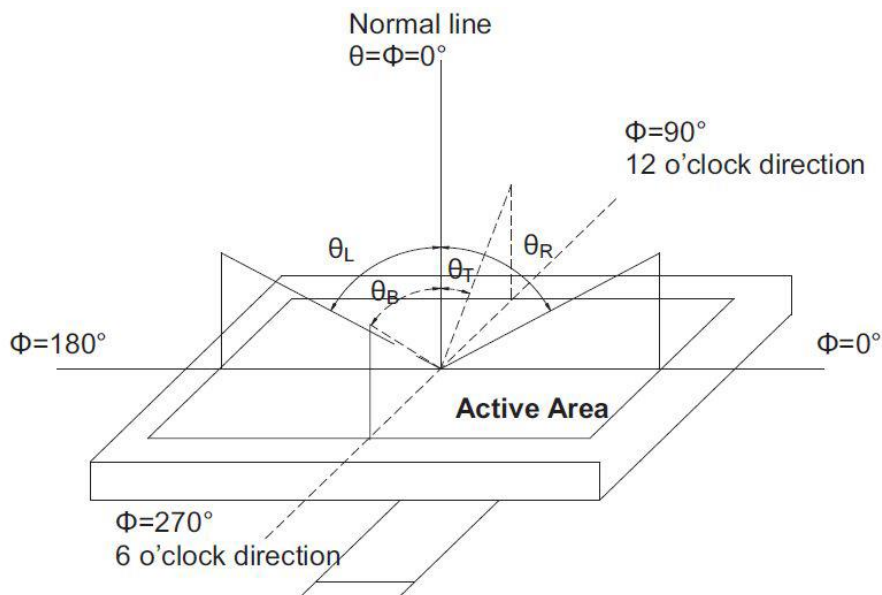
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise time,  $T_r$ ) and from white to black (Decay Time,  $T_f$ ).



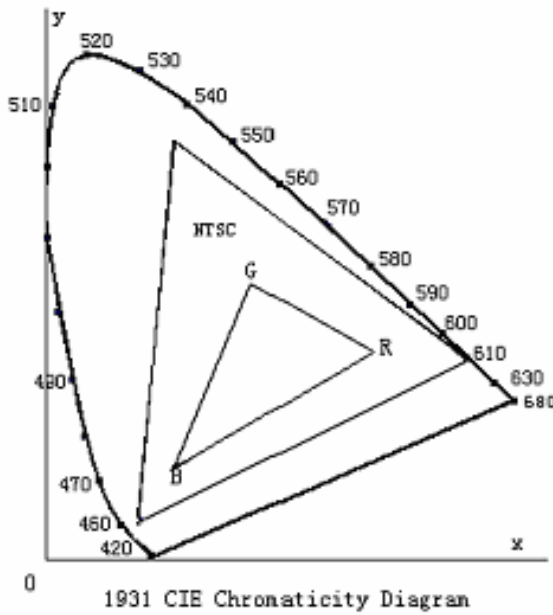
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig.2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance( brightness ) in 9 points}}{\text{Maximum Luminance( brightness ) in 9 points}}$$

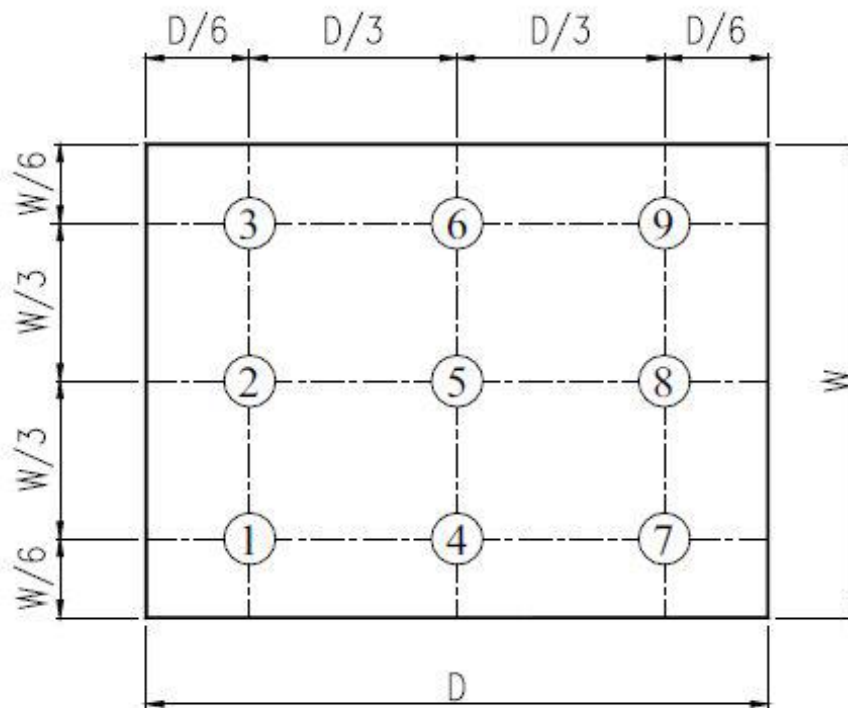


Fig. 2 Definition of uniformity

## 10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment Criteria
1	High Temp Operation	Ta=+70°C, 120hrs	Per table below
2	Low Temp Operation	Ta=-20°C, 120hrs	Per table below
3	High Temp Storage	Ta=+80°C, 120hrs	Per table below
4	Low Temp Storage	Ta=-30°C, 120hrs	Per table below
5	High Temp & High Humidity Storage	Ta=+60°C, 90% RH, 120hrs	Per table below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30°C 30 min ~ +80°C 30 min, Change time: 5 min, 10 cycles	Per table below
7	ESD (Operation)	C=150pF, R=330Ω, 5points/panel Air:±8KV, 5 times; Contact:±4KV, 5 times	Per table below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table below
9	Shock (Non-operation)	60G 6ms, ±X, ±Y, ±Z, 3 times, for each direction	Per table below
10	Package Drop Test	Height: 80cm, 1 corner, 3 edges, 6 surfaces	Per table below

Inspection	Criterion (after test)
Appearance	No crack on the FPC, on the LCD panel
Alignment of LCD panel	No bubbles in the LCD panel No other defects of alignment in active area
Electrical current	Within device specifications
Function / Display	No broken circuit, no short circuit or no black line No other defects of display

## 11. Precautions for Use of LCD Modules

### 11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

### 11.2 Handling

- a. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- b. Do not handle the product by holding the flexible pattern portion in order to assure the reliability.
- c. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- d. Provide a space so that the panel does not come into contact with other components.
- e. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- f. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.

- g. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
- h. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

### 11.3 Static electricity

- a. Ground soldering iron tips, tools and testers when they are in operation.
- b. Ground your body when handling the products.
- c. Power on the LCD module before applying the voltage to the input terminals.
- d. Do not apply voltage which exceeds the absolute maximum rating.
- e. Store the products in an anti-electrostatic bag or container.

### 11.4 Storage

- a. Store the products in a dark place at  $+25^{\circ}\text{C}\pm 10^{\circ}\text{C}$  with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- b. Storage in a clean environment, free from dust, active gas, and solvent.

### 11.5 Cleaning

- a. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- b. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

### 11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

