

NCV7471B, NCV7471C

System Basis Chip with a High-Speed CAN/CANFD, Two LINs and a Boost-Buck DC/DC Converter

NCV7471B/C is a System Basis Chip (SBC) integrating functions typically found in automotive Electronic Control Units (ECUs) in the body domain. NCV7471B/C provides and monitors the low-voltage power supplies for the application microcontroller and other loads, monitors the application software via a watchdog and includes high-speed CAN/CANFD and LIN transceivers allowing the ECU to host multiple communication nodes or to act as a gateway unit. The on-chip state controller ensures safe power-up sequence and supports low-power modes with a configurable set of features including wakeup from the communication buses or by a local digital signal WU. The status of several NCV7471B/C internal blocks can be read by the microcontroller through the serial peripheral interface or can be used to generate an interrupt request.

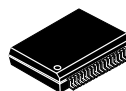
Features

- Control Logic
 - ◆ Ensures safe power-up sequence and the correct reaction to different supply conditions
 - ◆ Controls mode transitions including the power management and wakeup treatment – bus wakeups, local wakeups (via WU pin) and cyclic wakeups (through the on-chip timer)
 - ◆ Generates reset and interrupt requests
- Serial Peripheral Interface
 - ◆ Operates with 16-bit frames
 - ◆ Ensures communication with the ECU's microcontroller unit
 - ◆ Mode settings, chip status feedback and watchdog are accessible through eight twelve-bits registers
- 5 V VOUT Supply from a DC/DC Converter
 - ◆ Can deliver up to 500 mA with accuracy of $\pm 2\%$
 - ◆ Supplies typically the ECU's microcontroller
- 5 V VOUT2 Low-drop Output Regulator
 - ◆ Can supply external loads – e.g. sensors
 - ◆ Controlled by SPI and the state machine
 - ◆ Protected against short to the car battery
- 11 V (NCV7471B) or 6.5 V (NCV7471C) V_MID Supply from a DC/DC Converter
- A High-speed CAN/CANFD Transceiver
 - ◆ ISO11898-2: 2016 Compliant
 - ◆ Communication speed up to 1 Mbps
 - ◆ Specification for loop delay symmetry up to 2 Mbps
 - ◆ TxD dominant time-out protection
- Two LIN Transceivers
 - ◆ ISO17987-4, LIN2.X and J2602 compliant
 - ◆ TxD dominant time-out protection
- Wakeup Input WU
 - ◆ Edge-sensitive high-voltage input
 - ◆ Can be used as a wake-up source or as a logical input polled through SPI
- Protection and Monitoring Functions
 - ◆ Monitoring of the main supply through the V_MID point
 - ◆ Monitoring of VOUT supply output with programmable threshold
 - ◆ VOUT2 supply diagnosis through SPI and interrupt
 - ◆ Thermal warning and thermal shutdown protection
 - ◆ Programmable watchdog monitoring the ECU software
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



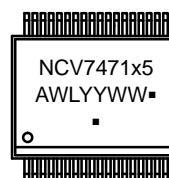
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SSOP36-EP
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MARKING DIAGRAM



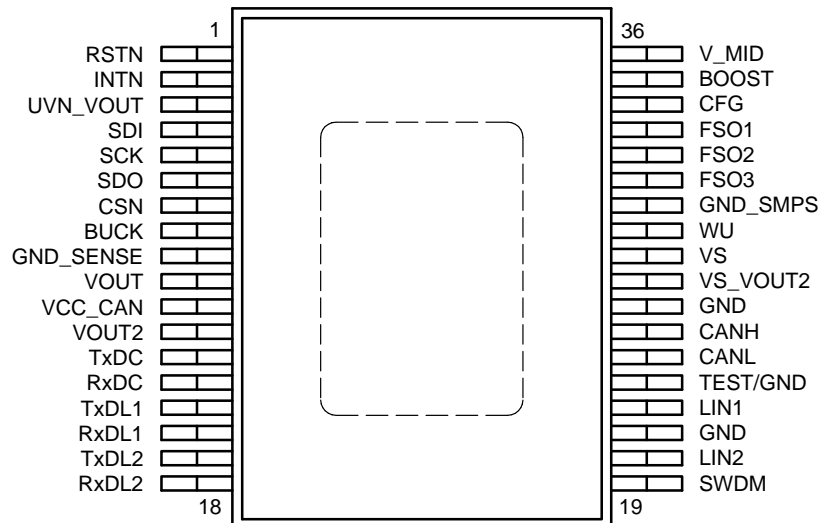
NCV7471x5 = Specific Device Code
x = B or C
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 52 of this data sheet.

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Pin Connections

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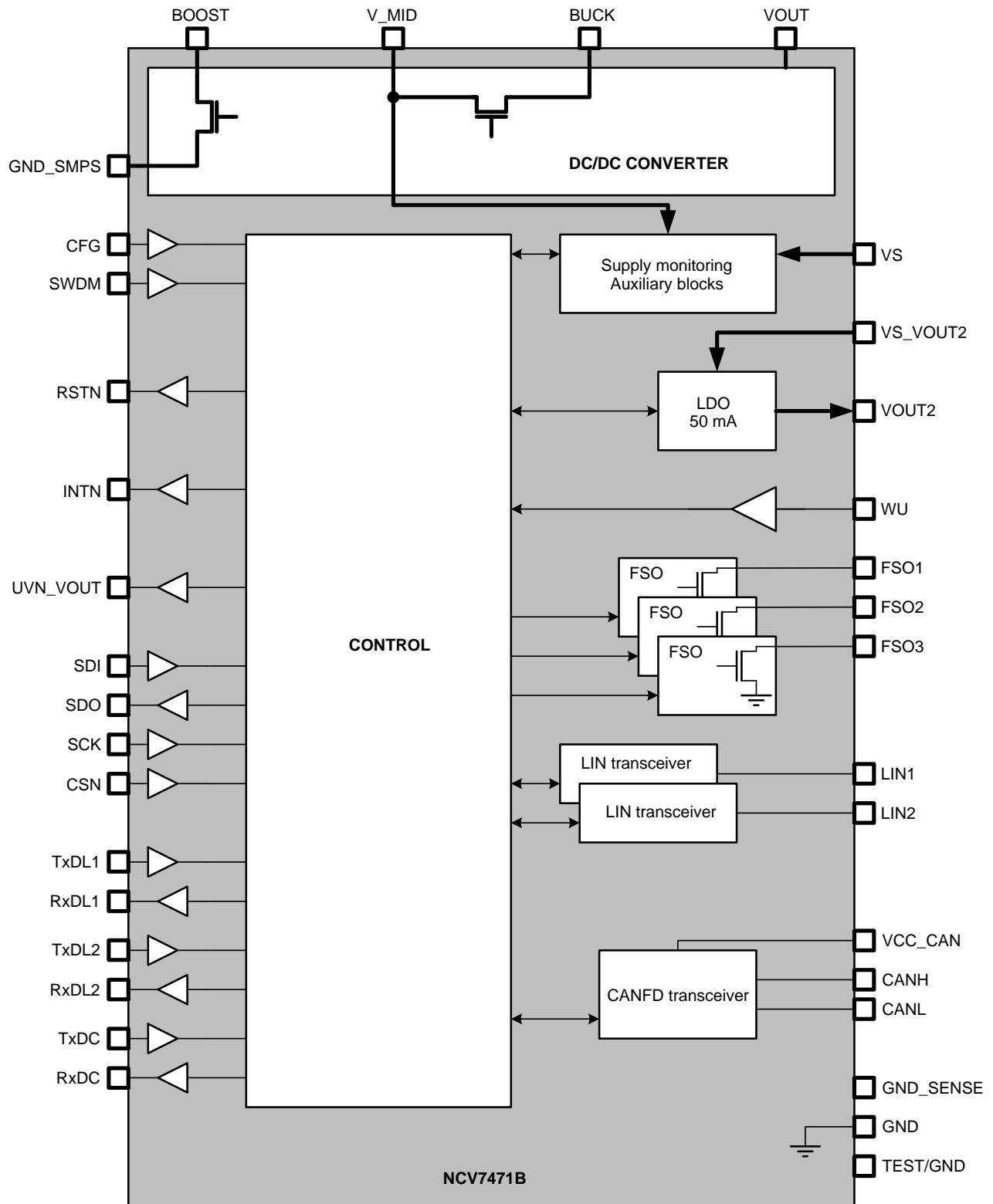


Figure 1. Block Diagram

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Table 1. PIN DESCRIPTION

| Pin Number | Pin Name | Pin Type (LV = Low Voltage; HV = High Voltage) | Pin Function |
|------------|-----------|--|---|
| 1 | RSTN | LV digital input/output; open drain; internal pull-up | System reset |
| 2 | INTN | LV digital output; open drain; internal pull-up | Interrupt request to the MCU |
| 3 | UVN_VOUT | LV digital output; open drain; internal pull-up | VOUT under-voltage signal to the MCU |
| 4 | SDI | LV digital input; internal pull-down | SPI data input |
| 5 | SCK | LV digital input; internal pull-down | SPI clock input |
| 6 | SDO | LV digital output; push-pull with tri-state | SPI data output |
| 7 | CSN | LV digital input (HV tolerant); internal pull-up | SPI chip select input |
| 8 | BUCK | HV analog input/output | Connection of L _{buck} coil to the integrated serial switch |
| 9 | GND_SENSE | Ground connection | Ground sense for the internal circuitry (e.g. VOUT2 regulator) |
| 10 | VOUT | LV supply input | Feedback of the DC/DC converter output; main 5 V LV supply for the digital IO's |
| 11 | VCC_CAN | LV supply input | Core supply for the CAN transceiver |
| 12 | VOUT2 | LV supply output | Output of the 5 V/50 mA low-drop regulator for external loads |
| 13 | TxDC | LV digital input; internal pull-up | Input of the data to be transmitted on CAN bus |
| 14 | RxDC | LV digital output; push-pull | Output of data received from CAN bus |
| 15 | TxDL1 | LV digital input; internal pull-up | Input of the data to be transmitted from LIN1 bus |
| 16 | RxDL1 | LV digital output; push-pull | Output of data received on LIN1 bus |
| 17 | TxDL2 | LV digital input; internal pull-up | Input of the data to be transmitted from LIN2 bus |
| 18 | RxDL2 | LV digital output; push-pull | Output of data received on LIN2 bus |
| 19 | SWDM | HV digital input; internal pull-down | Input to select the SW Development configuration |
| 20 | LIN2 | LIN bus interface | LIN2 bus line |
| 21 | GND | Ground connection | Ground connection |
| 22 | LIN1 | LIN bus interface | LIN1 bus line |
| 23 | TEST/GND | LV digital input; internal pull-down | Test-mode entry pin for production testing; should be grounded in the application |
| 24 | CANL | CAN bus interface | CANL line of the CAN bus |
| 25 | CANH | CAN bus interface | CANH line of the CAN bus |
| 26 | GND | Ground connection | Ground connection |
| 27 | VS_VOUT2 | HV supply input | Separate line input for the VOUT2 low-drop regulator |
| 28 | VS | HV supply input | Line supply for the battery-related core blocks |
| 29 | WU | HV digital input | Input for monitoring of external contacts |
| 30 | GND_SMPS | Ground connection | Power ground connection for the DC/DC converter |
| 31 | FSO3 | HV digital output; open drain low-side | Indication of a fail-safe event by rectangular signal of 100 Hz with 20% duty cycle; high-impedant in normal operation |
| 32 | FSO2 | HV digital output; open drain low-side | Indication of a fail-safe event by rectangular signal of 1.25 Hz with 50% duty cycle; high-impedant in normal operation |
| 33 | FSO1 | HV digital output; open drain low-side | Indication of a fail-safe event by static Low level; high-impedant in normal operation |
| 34 | CFG | HV digital input; internal pull-down or pull-up (depends on voltage) | Configuration of fail-safe behavior; in SW Development, CFG enables boost stage operation |
| 35 | BOOST | HV analog input/output | Connection of L _{boost} coil to the integrated switch to ground. |
| 36 | V_MID | HV analog input/output | Output of the 11 V/6.5 V boost stage; Intermediate point connecting the step-up and step-down stages of the DC/DC converter |

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APPLICATION INFORMATION

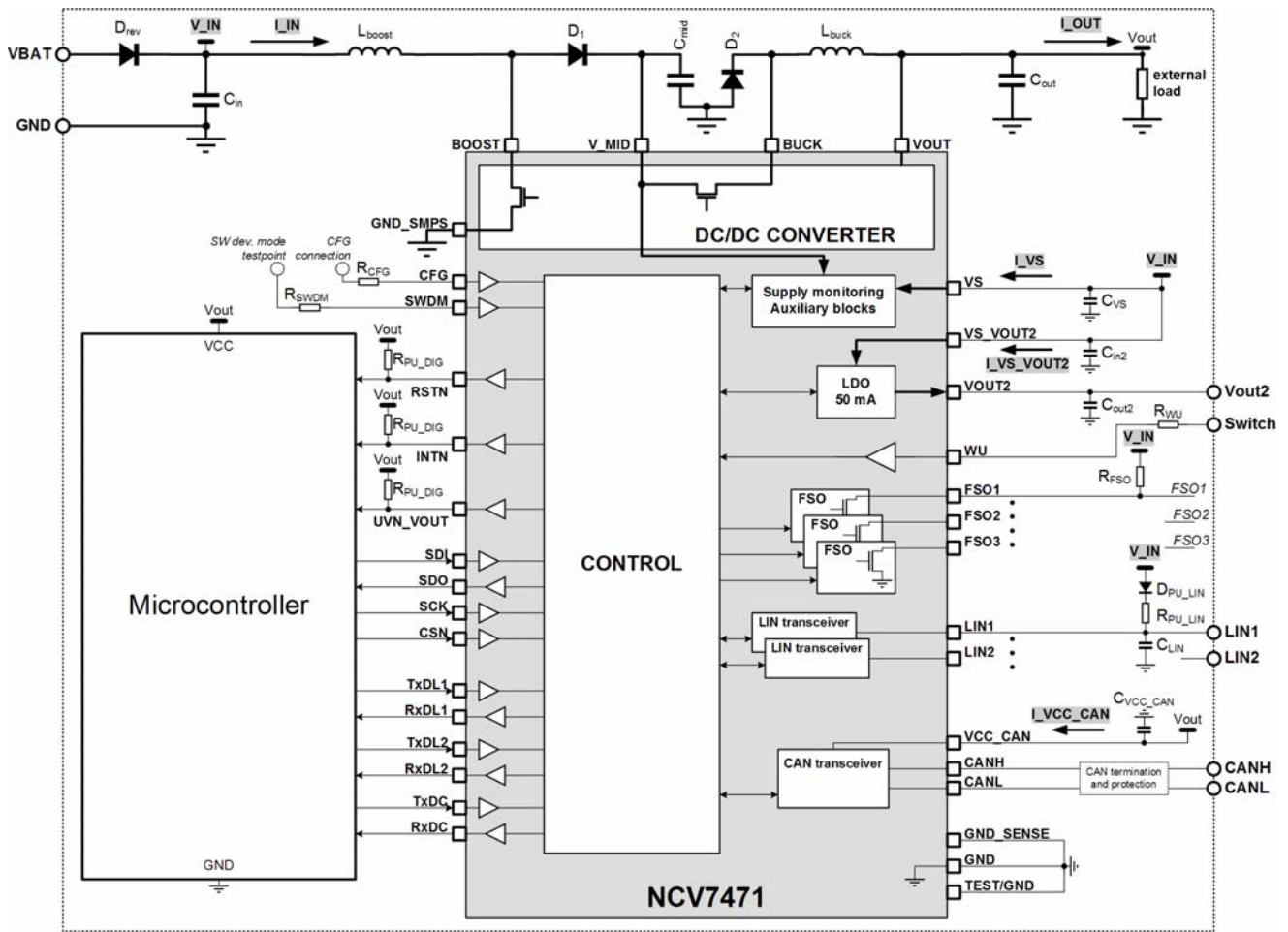


Figure 2. Example Application Diagram

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External Components

Overview of external components from application schematic in Figure 2 is given in Table 2 together with their recommended or required values.

Table 2. EXTERNAL COMPONENTS OVERVIEW

| Component Name | Description | Value | Note |
|--------------------------------|---|--|--|
| D _{rev} | Reverse-protection diode | parameters application-specific; e.g. 1 A / 50 V | Values and types depend on the application needs and conditions. Guidelines for their selection can be found in the product's application note. The given examples are suitable for NCV7471B, total boost stage loads of up to 425 mA, V _{OUT} loads of up to 250 mA, and for V _{IN} above 6 V. |
| C _{in} | Filtering capacitor for the DC/DC converter input | ≥ 1 μF ceramic; e.g. 1 μF / 40 V | |
| L _{boost} | Inductor for the converter boost stage; EMC filtering inductance | recommended range 3.3 μH – 22 μH; e.g. 22 μH / 2 A | |
| D ₁ | Diode for the converter boost stage | Shottky or ultra-fast; parameters application-specific; e.g. 1 A / 50 V | |
| C _{mid} | Filtering and stabilization capacitor for the converter intermediate voltage | ≥ 1 μF ceramic; + ≥ 10 μF electrolytic e.g. 1 μF / 40 V + 10 μF / 35 V | |
| D ₂ | Diode for the converter buck stage | Shottky or ultra-fast; parameters application-specific; e.g. 0.25 A / 50 V | |
| L _{buck} | Inductor for the converter buck stage | recommended range 10 μH – 22 μH; e.g. 10 μH / 0.5 A | |
| C _{out} | Filtering and stabilization capacitor for the converter output voltage | ≥ 10 μF ceramic; e.g. 10 μF / 10 V | |
| C _{VS} | Filtering capacitor for the VS input supplying LIN and auxiliary internal circuitry | recommended >100 nF ceramic | optional; depends on the application PCB |
| C _{in2} | Filtering capacitor for the VOUT2 regulator input | recommended >100 nF ceramic | optional; depends on the application PCB |
| C _{out2} | Filtering and stabilization capacitor for the VOUT2 regulator output | >1 μF ceramic (recommended 2.2 μF nominal) | required for VOUT2 stability |
| R _{WU} | Protection and filtering resistor for the WU input | recommended 33 kΩ nominal | optional; depends on the application needs |
| R _{FSO} | Pull-up resistors on the FSO outputs | | depends on the application needs |
| D _{PU_LIN} | Pull-up diode on LIN line | | required only for master LIN node |
| R _{PU_LIN} | Pull-up resistor on LIN line | 1 kΩ nominal | |
| C _{LIN} | Filtering capacitor on LIN line | Typically 100 pF – 220 pF nominal | optional; is function of the entire LIN network |
| C _{VCC_CAN} | Filtering capacitor on the CAN transceiver supply input | recommended >100 nF ceramic | optional; depends on the application PCB |
| CAN termination and protection | | | optional; is function of the entire CAN network |
| R _{PU_DIG} | Pull-up resistor for the open-drain digital outputs (INTN, RSTN, UVN_VOUT) | recommended 10 kΩ nominal | optional; only if the integrated pull-ups are not sufficient for the application |
| R _{SWDM} | Protection resistor on SWDM input | recommended 10 kΩ nominal | optional; depends on the application |
| R _{CFG} | Protection resistor on CFG input | recommended 10 kΩ nominal | optional; depends on the application CFG connection details can be found in the product's application note. |

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

VS Supply Input

VS pin of NCV7471B/C is typically connected to the car battery through a reverse-protection diode and can be exposed to all relevant automotive disturbances (ISO7637 pulses, system ESD...). VS supplies mainly the integrated LIN transceivers. Filtering capacitors should be connected between VS and GND.

V_MID Supply Point

V_MID node is the connection point between the two stages of the DC/DC converter. If only the buck (i.e. step-down) function of the converter is active (because the input voltage is sufficient or because boosting is not enabled), V_MID level stays two diode drops below the battery input to the application – see Figure 2. In case the boost stage of the converter is active, V_MID voltage is regulated to V_{MID_reg} (11 V typically).

V_MID pin is used to supply the core auxiliary blocks of the device – namely the voltage reference, biasing, internal regulator and the wakeup detector of the CAN bus. When the DC/DC converter is boosting, it is ensured that the internal core blocks remain functional even for low input supply level.

During power-up of the battery supply, V_MID point must reach V_{MID_PORH} level in order for the circuit to become functional – the internal state machine is initiated and the converter is activated in buck-only mode. The

circuit remains functional until V_MID falls back below V_{MID_PORL} level, when the device enters the Shut-down mode.

VOUT DC/DC Converter

The main application low-voltage supply is provided by an integrated boost-buck DC/DC converter, delivering a 5 V output VOUT. The converter can work in two modes:

- **Buck-only mode** is the default mode of the VOUT power-supply. In this mode, the boosting part of the converter is never activated and the resulting VOUT voltage can be only lower than the input line voltage. Buck-only mode is applied during the initial power-up (after the V_IN connection), wakeup from Sleep-mode and also recovery from the Fail-safe mode.
- **Boost-buck mode** ensures that the correct VOUT voltage is generated even if the input line voltage falls below the required VOUT level. This mode can be requested through the corresponding SPI control register. If selected, the boost-buck mode is used during Reset, Start-up, Normal, Standby, and Flash modes. It is also preserved during VOUT under-voltage recovery through Power-up mode. In SW Development configuration, boost-buck mode can be additionally enabled by High level on CFG pin. No SPI communication is therefore necessary to select the DC/DC mode in SW Development – see Table 3.

Table 3. CONTROL OF DC/DC CONVERTER MODES (“X” Means “Don’t Care”)

| Device Configuration | SPI enBOOST Bit | Signal on CFG Pin | Applied DC/DC Mode |
|----------------------|-----------------|-------------------|--------------------|
| Config 1, 2, 3, 4 | Low | X | Buck-Only |
| | High | | Boost-Buck |
| SW Development | Low | Low | Buck-Only |
| | | High | Boost-Buck |
| | High | X | Boost-Buck |

By default, the converter works with a fixed switching frequency f_{sw_DCDC} (typ. 485 kHz). Through the SPI settings, a switching frequency modulation can be applied with fixed modulation frequency of 10 kHz and three selectable modulation depth values – 10%, 20% or 30% of the nominal frequency.

VOUT level is monitored by an under-voltage detector with multiple thresholds:

- Comparison with selectable threshold $VOUT_RESx$. By default, the lowest threshold (typ. 3.1 V) applies for the state machine control and the activation of the RSTN signal. This reset threshold can be changed via SPI to any of the four programmable values.
- A second monitoring signal – UVN_VOUT – is generated based on comparison of the VOUT level with the highest monitoring level (typ. 4.65 V).

- VOUT is compared with a fixed threshold $VOUT_FAIL$ (typ. 2 V). If VOUT stays below $VOUT_FAIL$ level for longer than $t_{VOUT_powerup}$, a VOUT short-circuit is detected and Fail-safe mode is entered with the corresponding fail-safe information stored in SPI.

Both UVN_VOUT and RSTN pins provide an open drain output with integrated pull-up resistor. The split between reset-generating level VOUT_RESx and an under-voltage indication allows coping with VOUT dips in case of high loads coinciding with low input line voltages. The function of the VOUT and V_MID monitoring is illustrated in Figure 3 and Figure 4. FSO1 output activation and Fail-safe mode entry caused by VOUT undervoltage are shown in Figure 5 and Figure 6.

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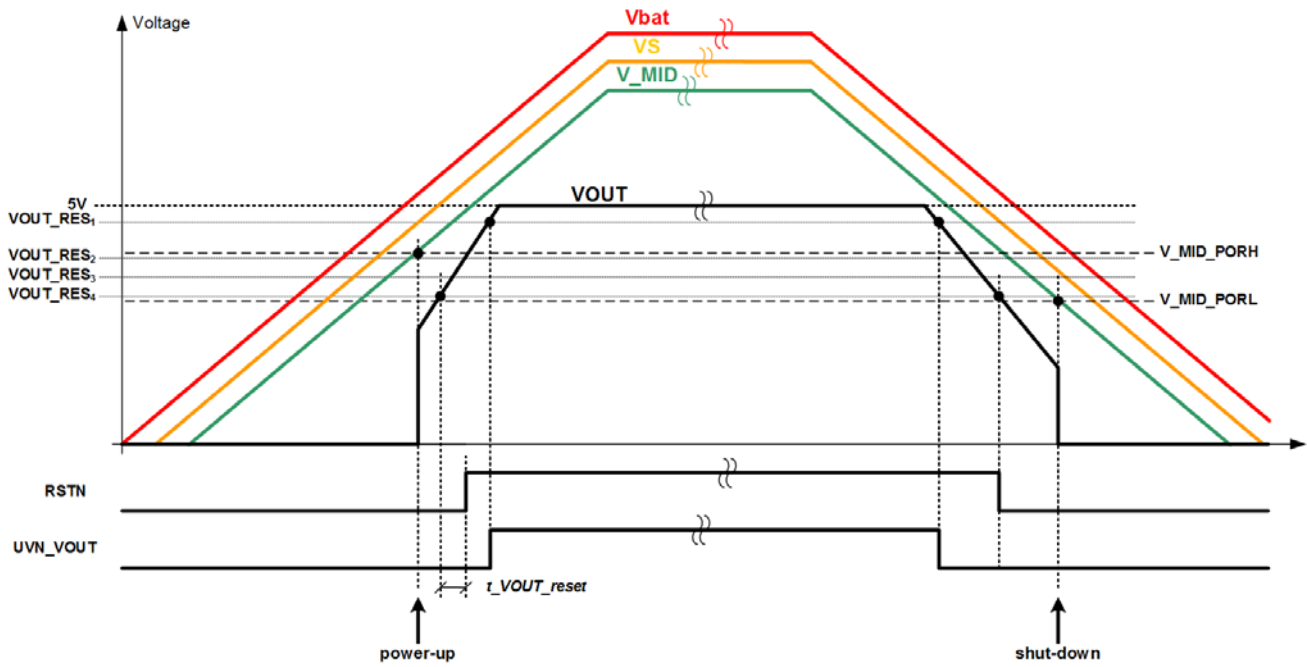


Figure 3. V_MID and VOUT Supply Monitoring (Filtering times are neglected)

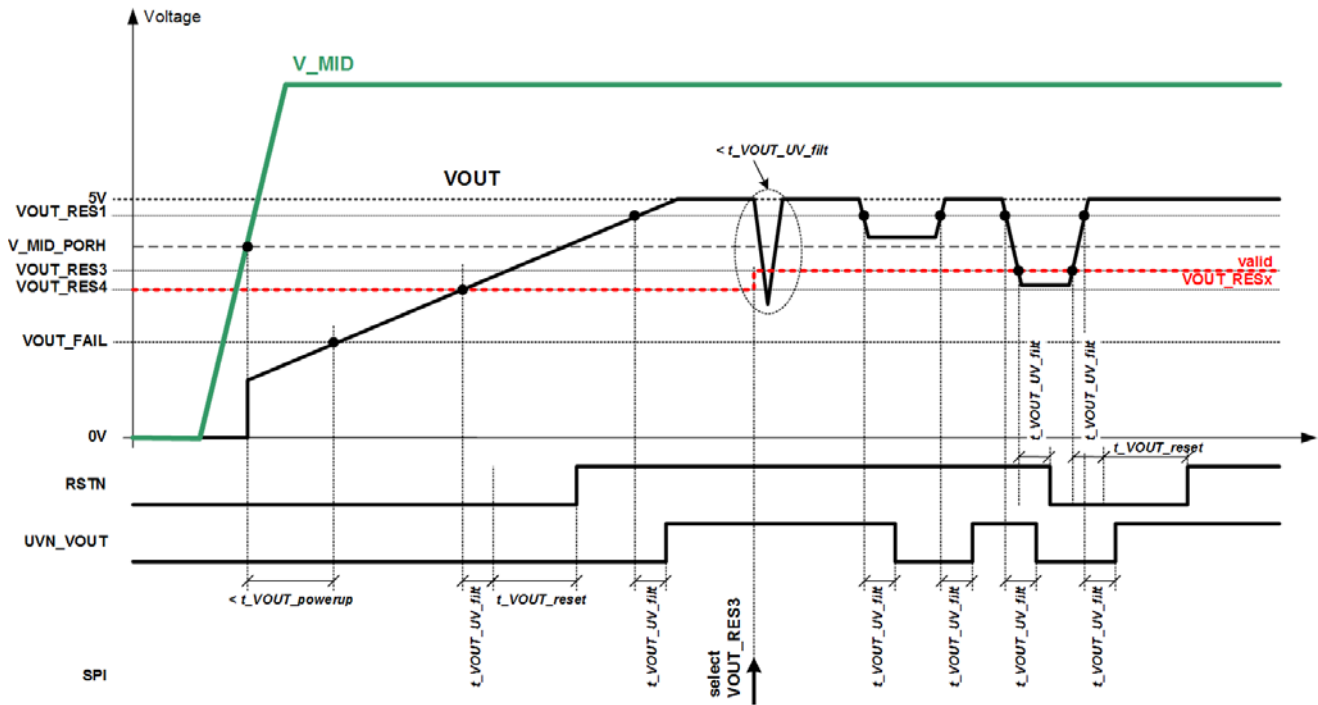


Figure 4. VOUT Monitoring

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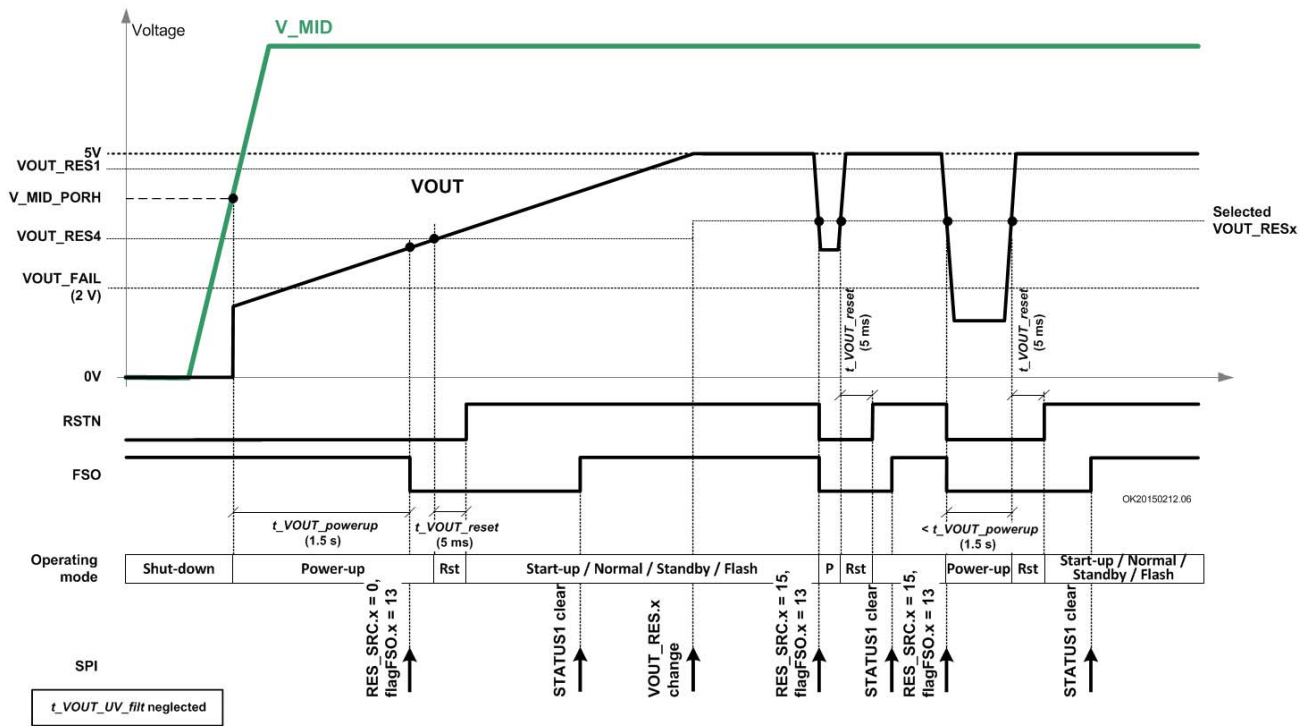


Figure 5. VOUT Monitoring

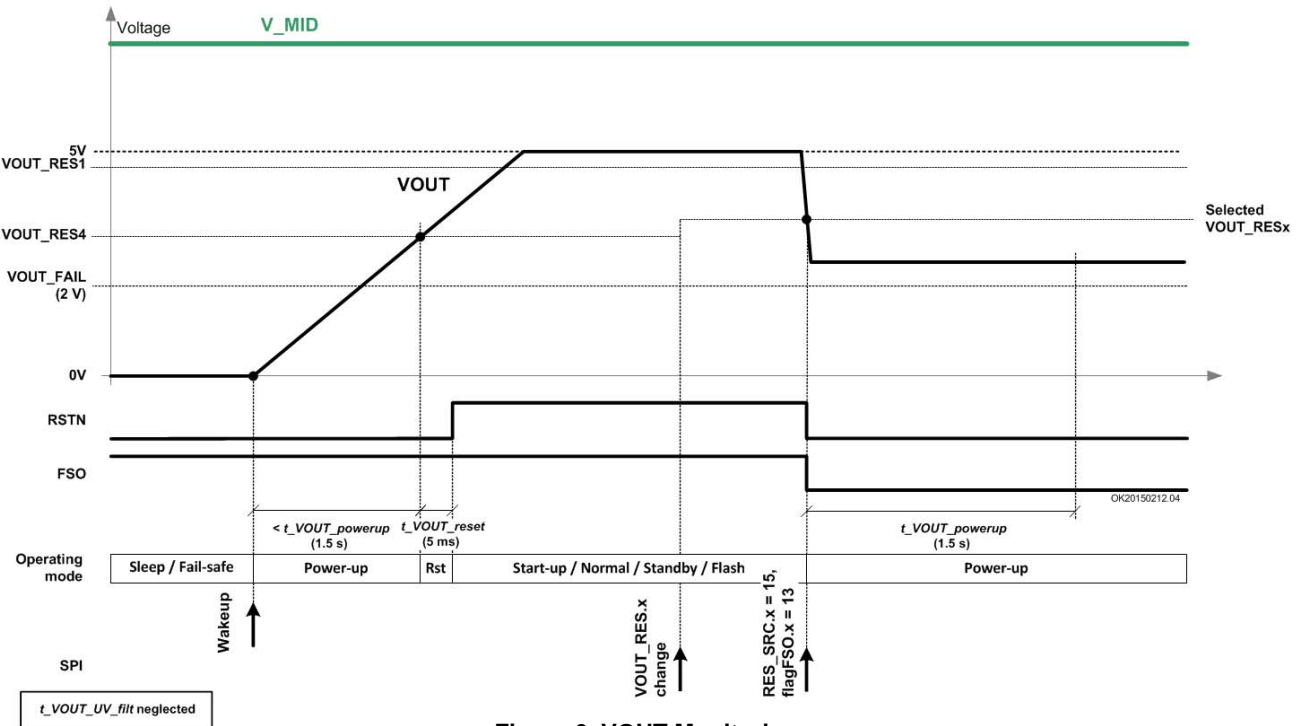


Figure 6. VOUT Monitoring

VOUT2 Auxiliary Supply

An integrated low-drop regulator provides a second 5 V supply VOUT2 to external loads, typically sensors. The regulator’s input is taken from a dedicated pin VS_VOUT2, which does not feature an explicit under-voltage monitoring. VS_VOUT2 would be typically connected to the VS pin or, in function of the application needs, might be taken from other nodes like, e.g., the DC/DC converter’s auxiliary node V_MID.

After a power-up or a reset event, as well as in Sleep mode, VOUT2 regulator is switched off. In Start-up, Normal, Standby and Flash modes, it can be freely activated or deactivated via SPI control register.

VOUT2 is diagnosed for under-voltage and over-voltage via comparators with fixed thresholds *VOUT2_UV* and *VOUT2_OV*, respectively. Under-voltage detection is working only when VOUT2 regulator is on, while the over-voltage is monitored regardless the VOUT2 regulator activation. Output of both detectors can be polled via SPI status bits. Change of the detection status (in either direction) is recorded as an SPI flag bit and, if enabled, can lead to an interrupt.

VCC_CAN Transceiver Supply

The integrated CAN transceiver uses a dedicated supply input VCC_CAN. The transceiver is supplied by VCC_CAN when configured for full-speed transmission or reception. When configured for wakeup detection, the transceiver is internally supplied from the V_MID pin.

A 5 V supply must be externally connected to VCC_CAN pin for the correct transceiver’s functionality in full-speed mode (“CAN Normal” or “CAN Receive-only”). VCC_CAN input has no dedicated monitoring and its correct level shall be ensured by the application – e.g. if VOUT is connected to VCC_CAN, then VOUT under-voltage monitoring can also cover the correct VCC_CAN level.

Communication Transceivers

High-Speed CAN/CANFD Transceiver

NCV7471B/C contains a high-speed CAN/CANFD transceiver compliant with ISO11898-2 standard, consisting of a transmitter, receiver and wakeup detector. The CAN transceiver can be connected to the bus line via a pair of pins CANH and CANL, and to the digital control through pins TxDC and RxDC. The functional mode of the CAN transceiver depends on the chip operating mode and on the status of the corresponding SPI bits – see Table 4, Table 5 and Figure 7.

Table 4. CAN TRANSCEIVER SPI CONTROL

| SPI Control Bits | | CAN Transceiver Function in Operating Modes | | | | |
|------------------|----------|---|-----------------------|------------------|------------|--------------------------------------|
| modCAN.1 | modCAN.0 | Power-up Reset | Start-up Normal Flash | Standby | Sleep | Fail-safe (except thermal shut-down) |
| 0 | 0 | CAN Off | CAN Off | CAN Off | CAN Off | CAN Wakeup |
| 0 | 1 | CAN Off | CAN Wakeup | CAN Wakeup | CAN Wakeup | CAN Wakeup |
| 1 | 0 | CAN Off | CAN Receive-only | CAN Receive-only | CAN Off | CAN Wakeup |
| 1 | 1 | CAN Off | CAN Normal | CAN Off | CAN Off | CAN Wakeup |

Table 5. CAN TRANSCEIVER MODES

| Mode | Transceiver | RxDC Pin | TxDC Pin | CANH/CANL Pins | Supply |
|------------------|---------------------------------|--|--|---------------------|---------|
| CAN Off | Fully off | High (if VOUT available) | Ignored | Biased to GND | n.a. |
| CAN Wakeup | Wakeup detector active | Low if wakeup detected; High otherwise (if VOUT available) | Ignored | Biased to GND | V_MID |
| CAN Receive-Only | Receiver active | Received data | Ignored | Biased to VCC_CAN/2 | VCC_CAN |
| CAN Normal | Transmitter and Receiver active | Received data | Data to transmit; checked for time-out | Biased to VCC_CAN/2 | VCC_CAN |

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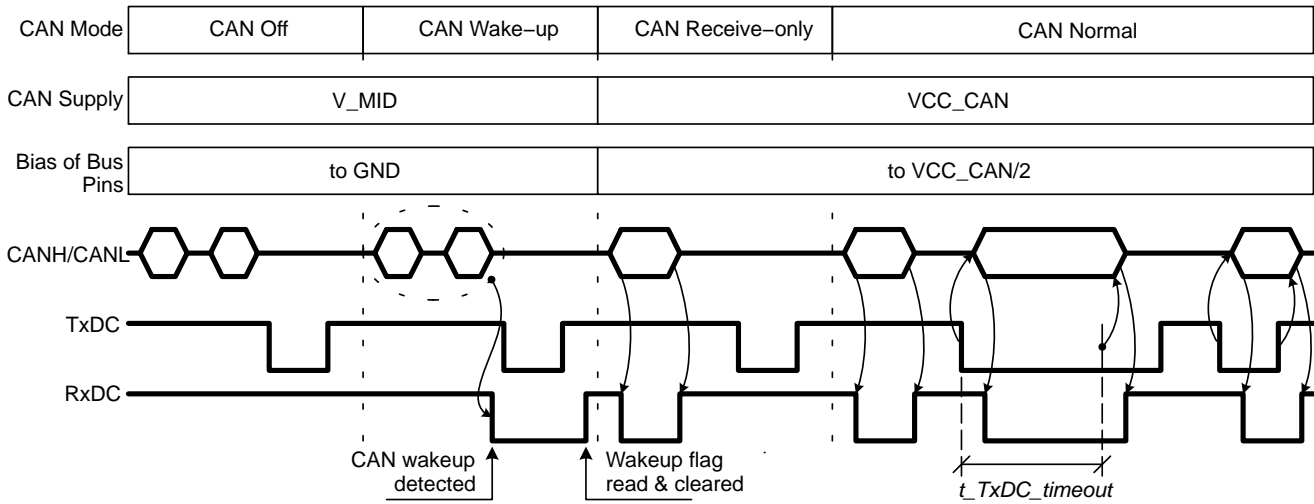


Figure 7. CAN Transceiver Modes

In **CAN Off** mode, the CAN transceiver is fully deactivated. Pin RxDC stays High (as long as VOUT is provided) and logical level on TxDC is ignored. The bus pins are weakly biased to ground via the input impedance.

In **CAN Wakeup** mode, the CAN transceiver, being supplied purely from V_MID pin, detects wakeups on the CAN lines. A valid wakeup on the CAN bus corresponds to a pattern of two dominants at least $t_{CAN_wake_dom}$ long, interleaved by a recessive at least $t_{CAN_wake_rec}$ long.

The total length of the pattern may not exceed $t_{CAN_wake_timeout}$. The CAN wakeup handling is illustrated in Figure 8.

In function of the current operating mode, a CAN wakeup can lead either to an interrupt request or to a reset. A CAN wakeup is also indicated by a Low level on the RxDC pin (which otherwise stays High as long as VOUT is available). Logical level on TxDC pin is ignored. The bus pins remain weakly biased to ground in the wakeup CAN mode.

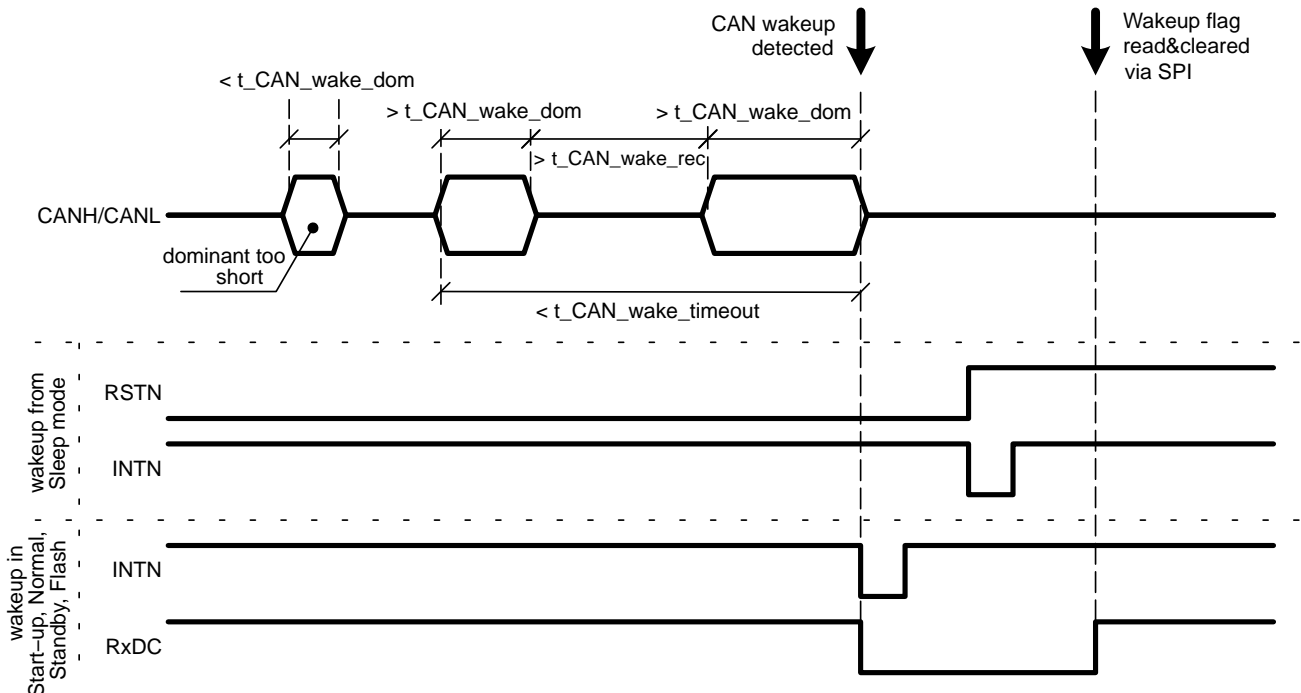


Figure 8. CAN Wakeup Detection

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In **CAN Receive-Only** mode, the receiver part of the CAN block detects data on the bus with the full speed and signals them on the RxDC pin. Logical level on TxDC pin is ignored. The receiver is supplied from the VCC_CAN supply input. The bus pins are biased to VCC_CAN/2 level through the input circuitry.

In **CAN Normal** mode, the full CAN transceiver functionality is available. Both reception and transmission at the full speed can be used. Received data are signaled via RxDC pin, while logical level on TxDC pin is translated into the corresponding bus level (TxDC = High or Low leading to a recessive or dominant being transmitted, respectively). Both the receiving and the transmitting part are supplied from the VCC_CAN supply input. The bus pins are biased to VCC_CAN/2 level through the input circuitry. TxDC input signal is monitored with a time-out timer. If a dominant longer than $t_{TxDC_timeout}$ is requested (i.e.

TxDC is Low for longer than $t_{TxDC_timeout}$), the transmission is internally disabled. The reception from the CAN bus remains functional and the internally set CAN transceiver mode does not change. The transmission is again enabled when TxDC becomes High.

LIN Transceivers

NCV7471B/C integrates two on-chip LIN transceivers – interfaces between physical LIN buses and the LIN protocol controllers compatible to LIN2.X and J2602 specifications – consisting of a transmitter, receiver and wakeup detector. Each LIN transceiver can be connected to the bus line via LINx pin, and to the digital control through pins TxDLx and RxDLx. The functional mode of the LIN transceivers depends on the chip operating mode and on the status of the corresponding SPI bits – see Table 6, Table 7, and Figure 9. The LIN transceivers are supplied directly from the VS pin.

Table 6. LIN TRANSCEIVERS SPI CONTROL

| SPI Control Bits x = 1 ... 2 | | LINx Transceiver Function in Operating Modes | | | | |
|------------------------------|-----------|--|-----------------------|-------------------|-------------|--------------------------------------|
| modLINx.1 | modLINx.0 | Power-up Reset | Start-up Normal Flash | Standby | Sleep | Fail-safe (except thermal shut-down) |
| 0 | 0 | LINx Off | LINx Off | LINx Off | LINx Off | LINx Wakeup |
| 0 | 1 | LINx Off | LINx Wakeup | LINx Wakeup | LINx Wakeup | LINx Wakeup |
| 1 | 0 | LINx Off | LINx Receive-only | LINx Receive-only | LINx Off | LINx Wakeup |
| 1 | 1 | LINx Off | LINx Normal | LINx Normal | LINx Off | LINx Wakeup |

Table 7. LIN TRANSCEIVERS MODES

| Mode | Transceiver | RxDLx Pin | TxDLx Pin | LINx Pin Bias |
|-------------------|---------------------------------|--|---|------------------------------|
| LINx Off | Fully off | High (if VOUT available) | Ignored | Pull-up current source to VS |
| LINx Wakeup | Wakeup detector active | Low if wakeup detected; High otherwise (if VOUT available) | Ignored | Pull-up current source to VS |
| LINx Receive-Only | Receiver active | Received data | Ignored | Pull-up current source to VS |
| LINx Normal | Transmitter and Receiver active | Received data | Data to transmit; checked for time-out (if enabled via SPI); transmitted if VS > VS_MON | 30 kΩ pull-up |

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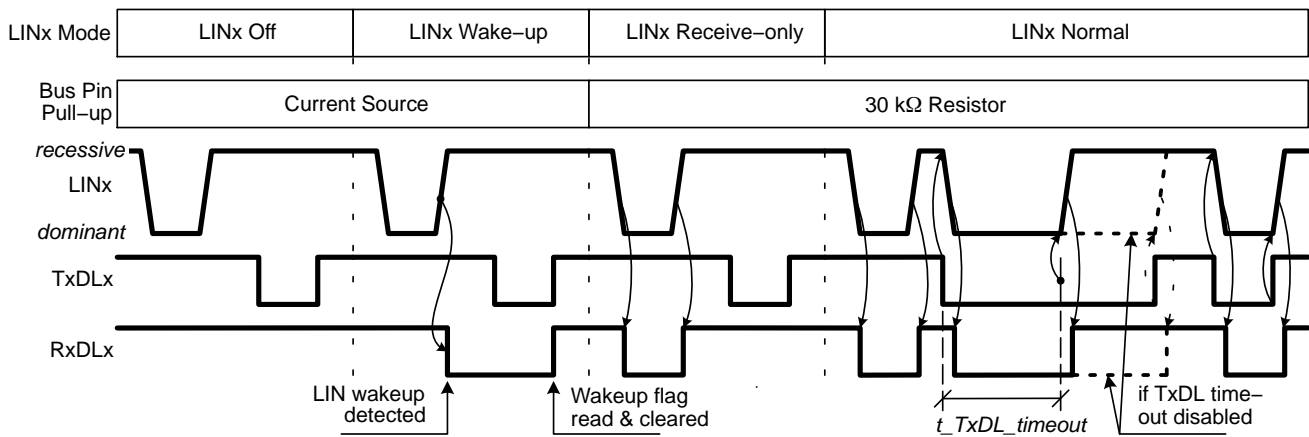


Figure 9. LIN Transceiver Modes

In **LINx Off** mode, the respective LIN transceiver is fully deactivated. Pin RxDLx stays High (as long as VOUT is provided) and logical level on TxDLx is ignored. The bus pin is internally pulled to VS with a current source (thus limiting VS consumption in case of a permanent LINx short to GND).

In **LINx Wakeup** mode, the LIN transceiver detects wakeups on the LIN line. A valid wakeup on the LIN bus corresponds to a dominant at least t_{LIN_wake} long, followed by a recessive. Thus the wakeup will not be

detected in case of a permanent LIN short to GND, because a rising edge on LIN is necessary for the wakeup detection – see Figure 10.

In function of the current operating mode, a LIN wakeup can lead to an interrupt request or to a reset. A LIN wakeup is also indicated by a Low level on the corresponding RxDLx pin (which otherwise stays High as long as VOUT is available). Logical level on TxDLx pin is ignored; bus pin is internally pulled to VS with a current source.

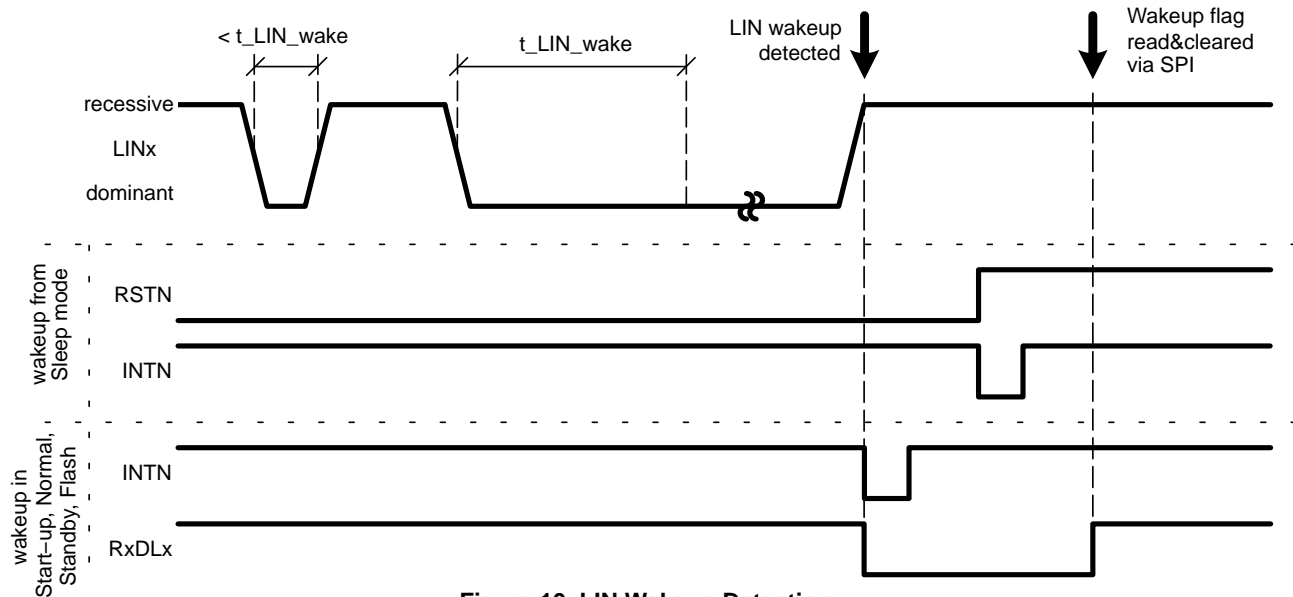


Figure 10. LIN Wakeup Detection

In **LINx Receive-Only** mode, the receiver part of the LINx block detects data on the bus with the normal speed and signals them on the RxDLx pin. Logical level on TxDLx pin is ignored; bus pin is internally pulled to VS with a current source.

In **LINx Normal** mode, the full LIN transceiver functionality is available. Both reception and transmission at the normal speed can be used. Received data are signaled via RxDLx pin, while logical level on TxDLx pin is translated into the corresponding bus level (TxDLx = High or Low leading to a recessive or dominant being transmitted, respectively). The LINx pin is internally pulled to VS via a 30 kΩ resistive path. TxDLx input signal is monitored with a time-out timer. If a dominant longer than $t_{TxDL_timeout}$ is requested (i.e. TxDLx is Low for longer than $t_{TxDL_timeout}$), the transmission is internally disabled. The reception from the LINx bus remains functional and the internally set LINx transceiver mode does not change. The transmission is again enabled when TxDLx becomes High. The TxDL dominant time-out feature can be disabled via SPI (a common setting for both LIN blocks).

Transmission onto the bus is blocked if VS supply falls below VS_MON level. VS monitoring does not influence the LIN reception or the TxDLx time-out detection. Indication of the VS monitoring is accessible through SPI bit $statVS_LOW$.

For applications with lower required bit rates, the transmitted LIN signal slope can be decreased by a dedicated SPI setting (“LIN low-slope mode”).

WU – Local Wakeup Input

WU pin is a high-voltage input typically used to monitor an external contact or switch. A stable logical level of the WU signal is ensured even without an external connection:

- if the WU level is High for longer than t_{WU_filt} , an internal pull-up current source is connected to WU
- if the WU level stays Low for longer than t_{WU_filt} , an internal pull-down current source is connected to WU

The logical level on pin WU can be polled through SPI or used as a wakeup source:

- **WU Signal Polling:** in Start-up, Normal, Standby and Flash modes, the current WU logical level is directly reflected in SPI bit $statWU$, available for readout
- **WU Edge Detection / Wake-up:** by setting SPI bits $modWU.1$ and $modWU.0$, edge detection is applied to WU signal. The device can be set to detect rising, falling or both edges on the WU signal. When the selected edge is detected, the event is latched in SPI bit $flagWakeWU$. In function of the current operating mode, edge on WU leads to an interrupt request (Start-up, Normal, Standby and Flash modes) or reset (Sleep mode). More details on the event handling, applicable also to WU edges, are given in the Event Flags and Interrupt Requests section.

Handling of the WU pin signal is illustrated in Figure 11.

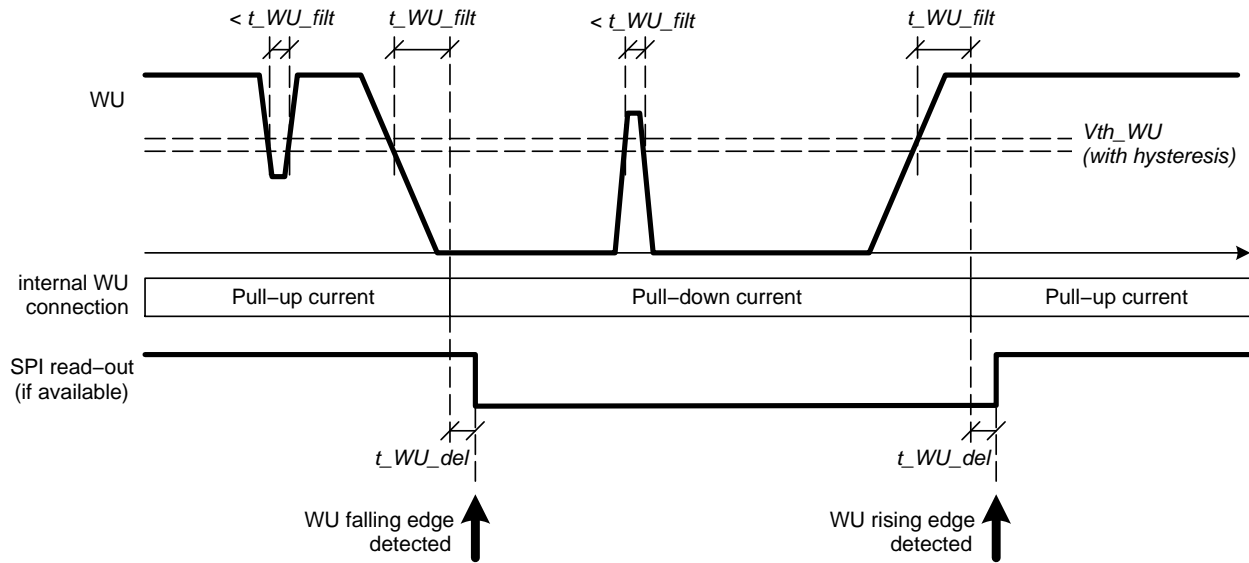


Figure 11. WU Pin Handling

NCV7471B, NCV7471C

Operating Modes

The principal operating modes of NCV7471B are shown in Figure 12 and described in the following paragraphs.

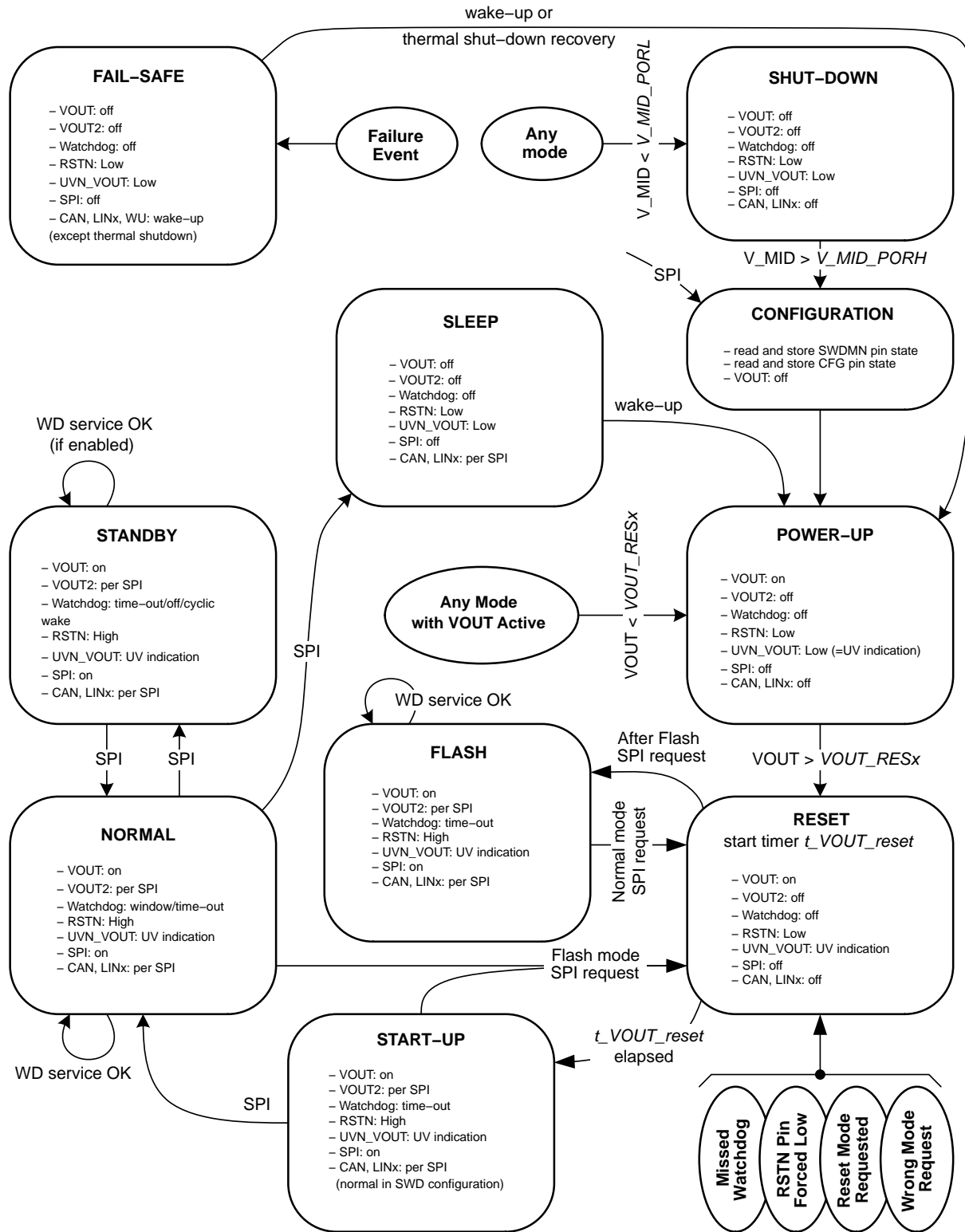


Figure 12. Operating Modes

Shut-Down Mode

The Shut-down mode is a passive state, in which all NCV7471B/C resources are inactive. The Shut-down mode provides a defined starting point for the circuit in case of supply under-voltage or the first supply connection.

Both on-chip power-supplies – VOUT and VOUT2 – are switched off and the CAN/LINx transceiver pins (CANH, CANL and LINx) remain passive so that they do not disturb the communication of other nodes connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high-impedant). Pins RSTN and UVN_VOUT are forced Low – RSTN/UVN_VOUT Low level is guaranteed, when V_MID supply is above *V_MID_DigOut_Low* or VOUT pin is above *VOUT_DigOut_Low*. Pins RxDx are kept High (i.e. at VOUT level).

The Shut-down mode is entered asynchronously whenever the V_MID level falls below the power-on-reset level *V_MID_PORL*.

The Shut-down mode is left only when the V_MID supply exceeds the high power-on-reset level *V_MID_PORH*. When exiting the Shut-down mode, NCV7471B/C always enters the Configuration mode.

Configuration Mode

Configuration is a transient mode, in which NCV7471B/C reads logical input levels on pins SWDM and CFG. The SWDM and CFG values in Configuration mode define watchdog and fail-safe behavior of the chip, respectively.

After leaving the Configuration mode, the device configuration can be changed neither by the SPI communication nor by signal modifications on the SWDM and CFG pins and is kept until the next V_MID under-voltage. The application software can also force Configuration mode by an SPI request from Start-up or Normal mode. Table 8 summarizes the available configurations and their characteristics. After reading both pins' levels, NCV7471B/C automatically transitions into the Power-up mode. Because the SMPS is off in Configuration mode, SPI-initiated transition from a functional mode to Configuration may result in a short dip on VOUT, which is not disturbing the device operation and which is recovered immediately after the Configuration mode is left.

CFG pin connection details can be found in the product's application note.

Two SPI bits are foreseen to reflect the state of SWDM and CFG pins:

- statSWDM bit latches the SWDM pin logical value read during Configuration mode. The bit remains unchanged until the Configuration mode is entered again.
- statCFG bit either latches the CFG value read in Configuration mode and remains unchanged afterwards (in Config 1,2,3,4), or keeps reflecting the current CFG signal throughout the IC operation (in SW Development).

Table 8. POSSIBLE CONFIGURATIONS (“X” Means “Don’t care”)

| FastFSON SPI bit | Values Latched in Configuration Mode | | Resulting Configuration | Behavior | |
|---------------------|---|-----|----------------------------|--|--|
| | SWDM | CFG | | At Watchdog Failure | At RSTN Clamped Low |
| 1 | 0 | 1 | Config 1 | 1 st failure activates FSOx; Fail-safe mode not entered | FSOx activated; external reset controls the operating mode |
| 1 | 0 | 0 | Config 2 | 1 st failure puts the chip into Fail-safe mode | FSOx activated; Fail-safe mode entered |
| 0 | 0 | 1 | Config 3 | 2 nd failure activates FSOx; Fail-safe mode not entered | FSOx activated; external reset controls the operating mode |
| 0 | 0 | 0 | Config 4 | 2 nd failure activates FSOx and puts the chip into Fail-safe mode | FSOx activated; Fail-safe mode entered |
| X | 1 | X | SW Development | No FSOx activation; no Fail-safe mode entry; stored in SPI, can lead to interrupt (if enabled) | External reset controls the operating mode; no FSOx activation |

Power-Up Mode

The Power-up mode ensures correct activation of the on-chip VOUT DC/DC converter or recovery of VOUT after an under-voltage event.

In the Power-up mode, the VOUT DC/DC converter is switched on (or kept on) while VOUT2 regulator remains in the previous state (e.g. VOUT2 is off coming from the Shut-down and Configuration modes). The CAN/LINx transceiver pins (CANH, CANL and LINx) remain passive so that they do not disturb the communication of other nodes

connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high-impedant). Pins RSTN and UVN_VOUT are forced Low. Pins RxDx are kept High (i.e. at VOUT level).

The Power-up mode is entered from the Configuration mode or after a wakeup from Sleep mode (in both cases, VOUT DC/DC converter needs to be activated). It will be also entered from any state with VOUT already active (Normal, Standby, Reset, Start-up, Flash) if the VOUT level

falls below the *VOUT_RESx* level (the valid *VOUT_RESx* level is set via SPI).

The Power-up mode is correctly left when *VOUT* exceeds the SPI-selected *VOUT_RESx* level. An overload/short-circuit failure is detected if *VOUT* does not reach the failure threshold *VOUT_FAIL* within time *t_VOUT_powerup*. NCV7471B then goes to the Fail-safe mode. *VOUT* staying between *VOUT_FAIL* and *VOUT_RESx* levels will keep the device in the Power-up mode, unless the thermal shutdown temperature is reached (e.g. because of *VOUT* overload).

Reset Mode

The Reset mode is a transient mode providing a defined RSTN pulse for the application microcontroller.

VOUT supply is kept on, while *VOUT2* regulator remains in its previous state. The CAN/LINx transceiver pins (CANH, CANL and LINx) are passive so that they do not disturb the communication of other nodes connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high-impedant). Pin RSTN is forced Low while pin UVN_VOUT indicates the *VOUT* under-voltage with respect to the highest reset level. Pins Rx/Dx are kept High (i.e. at *VOUT* level).

Reset mode will be entered as a consequence of one of the following events:

- Power-up mode is exited
- RSTN pin is forced Low externally
- Flash mode has been requested via SPI
- Flash mode exit has been requested via SPI
- Reset mode has been requested via SPI
- An un-authorized operating mode has been requested via SPI
- Watchdog has been missed in Config 1 or Config 3

Normally, the Reset mode is left after a defined time *t_VOUT_reset* when the RSTN pin is internally released to High – the chip then goes to the Start-up mode. Overdriving the RSTN pin to Low externally will extend the Reset mode duration. If RSTN is still forced Low externally even after time *t_VOUT_Clamped_Low* elapses, a “RSTN clamped Low” event is detected. The reaction depends on the chip configuration (SW Development or Config 1/2/3/4). “RSTN clamped Low” can lead to FSOx signal activation, Fail-safe mode entry or just to the Reset mode being kept as long as RSTN is driven Low – see Table 9.

If the Reset mode is entered due to external RSTN Low pulse during Start-up mode, FSOx outputs are activated (unless the device is in the SW Development configuration). This condition fosters that the external MCU sends at least one correct watchdog message before applying an external reset.

Information about the cause of a reset pulse is stored in the SPI registers and can be read by the application software. The “Reset source” information is kept unchanged until the next reset event.

Start-Up Mode

During the Start-up mode, the microcontroller supplied by *VOUT* is expected to initialize correctly and to perform successful communication via the SPI interface.

Start-up mode is the first mode in which SPI is enabled and the watchdog is started. The application software is able to read any SPI register. Write access to SPI depends on the FSO_internal flag (i.e. whether a failure condition preceded the Start-up mode – see the FSO1/2/3 – Fail-safe Outputs section for details):

- In case FSO_internal = 0 (inactive), any SPI register can be written and all features can be configured in the Start-up mode (e.g. CAN/LIN transceivers can be activated, *VOUT2* can be activated)
- In case FSO_internal = 1 (active), all SPI write frames will be ignored by the chip, with the exception of the watchdog service frame (write access to the MODE_CONTROL register).

The watchdog is activated and works in the timeout mode. A correct watchdog service is expected from the MCU before the watchdog period elapses. The correct watchdog-serving SPI message should arrive in time and should contain either a request to enter Normal mode or a request to enter the Flash mode. The Start-up mode is then exited into the requested mode.

If the microcontroller software fails to serve the watchdog in time, the chip detects the “1st Watchdog Missed” event which is handled according the configuration (SW Development or Config 1/2/3/4) – see the FSO1/2/3 – Fail-safe Outputs section.

In the SW Development configuration, the following exceptions are applied for the Start-up mode:

- the device remains in the Start-up mode as long as the watchdog is not served correctly – thus also in case no microprocessor is connected.
- when entering the Start-up mode, CAN and both LIN transceivers are automatically put to their Normal mode

As a result, device in SW Development mode keeps on providing *VOUT* supply and full CAN and LIN functionality even if no application software is available or if no microprocessor is connected. In addition, no RSTN pulses are generated and FSOx pins remain inactive.

Normal Mode

The Normal mode allows using all NCV7471B/C resources (*VOUT2*, CAN transceiver, LINx transceivers) which can be monitored and configured by the microcontroller via the SPI interface. The watchdog is working in the window mode with selectable period which can be changed at each watchdog-service SPI message.

VOUT is kept on. INTN pin provides the Interrupt Requests (IRQ's) depending on the device status and the interrupt mask settings. The application software can poll all SPI status bits or enable the corresponding interrupt requests. Pin RSTN remains High while pin UVN_VOUT

indicates the VOUT under-voltage with respect to the highest reset level. WU pin and transceivers can be configured for wake-up recognition which is then signalled as an interrupt request.

In a software-controlled way, the microcontroller can either keep NCV7471B/C in the Normal mode or request a transition into another mode (including Reset and Configuration).

Standby Mode

Standby is the first low-power mode of NCV7471B/C. It is entered after the corresponding SPI request is made in the Normal mode. In the Standby mode, the application microcontroller remains supplied by VOUT DC/DC converter and can continue the SPI communication. VOUT remains monitored by the reset and failure comparators. The functionality of the LINx blocks remains fully available while the CAN transceiver is limited – it can be put to Receive-only, Wakeup or Off mode. Active CAN transmission is not available.

Three types of wakeup can be used during the Standby mode – a local wakeup through the WU pin change, a bus wakeup (via a CAN or LINx bus) and a cyclic wakeup generated by the watchdog timer. A detected wakeup will cause an interrupt request through INTN pin.

During Standby mode, at least one of the following conditions must be fulfilled:

- Watchdog is requested to be on
- Cyclic wakeup is enabled
- CAN wakeup is enabled
- LIN wakeup is enabled at least on one of the LINx channels

If none of the above conditions is respected, all CAN and LIN wakeups will be automatically enabled as well as WU wakeup on both edges. Note, that allowing only the local WU wakeup is not sufficient for successful Standby mode entry without watchdog. This SPI setting condition is monitored and fostered throughout the Standby mode duration.

Standby will be kept as long as the microcontroller can correctly serve the watchdog and the interrupts according the SPI settings. Standby is left either by an SPI request for a mode change or by a reset event.

Sleep Mode

Sleep mode is the second low-power mode of NCV7471B/C. The microcontroller is not supplied and most resources are inactive beside the blocks needed for wakeup detection.

Sleep mode can be entered from Normal mode by the corresponding SPI request. Immediately after the Sleep mode entry, RSTN and UVN_VOUT pins are pulled Low in order to stop the microcontroller software. Both power supplies – VOUT and VOUT2 – are switched off; SPI and watchdog are de-activated. Depending on the SPI settings

prior to the Sleep mode entry, CAN and LINx transceivers can be either switched off or configured for bus wakeup detection.

Two types of wakeup can be used during the Sleep mode – a local wakeup through the WU pin change, and a bus wakeup (via a CAN or LINx bus). A detected wakeup will cause entry into Power-up mode.

When Sleep mode is requested, at least one of the following conditions must be fulfilled:

- CAN wakeup is enabled
- LIN wakeup is enabled at least on one of the LINx channels

If none of the above conditions is respected, all CAN and LIN wakeups will be automatically enabled as well as WU wakeup on both edges. Note, that allowing only the local WU wakeup is not sufficient. Sleep mode can be only left through a wakeup or V_MID under-voltage.

Fail-Safe Mode

Fail-safe mode ensures a defined reaction of NCV7471B/C to a failure event. Both power supplies – VOUT and VOUT2 – are switched off, and the Fail-safe outputs are activated. RSTN and UVN_VOUT pins are pulled Low in order to ensure that the microcontroller software execution stops immediately.

Fail-safe mode will be entered as a consequence of one of the following events:

- Watchdog has been missed in Config 2 or Config 4
- “RSTN clamped Low” has been detected in Config 2 or Config 4
- “RSTN clamped High” has been detected
- VOUT power supply has not reached the failure level VOUT_FAIL after $t_{VOUT_powerup}$ – this situation can be encountered during failed chip start-up or during too long and deep under-voltage
- Fail-safe mode has been requested via SPI (in SW Development only)
- Thermal shut-down has been encountered

All CAN and LINx transceivers are automatically configured to wakeup detection; wakeup from WU pin is also enabled on both edges. A detected bus or WU wakeup will bring NCV7471B/C into Power-up mode. Only in case of a thermal shut-down, no wakeups are detected and the Fail-safe mode is exited as soon as the junction temperature decreases below the warning level.

Throughout the Fail-safe mode, some SPI settings and status bits are preserved, and become effective after Fail-safe mode recovery. Namely CONTROL2 register (with SMPS mode settings and VOUT reset level settings), STATUS1 register (with wake-up flags and FSO flags) and GENERAL PURPOSE register are not reset when Fail-safe is entered, and keep their previous content. Fail-safe

recovery is therefore different compared to wakeup from Sleep mode, after which CONTROL2 is reset.

Flash Mode

Flash mode offers a relaxed watchdog timing enabling transfer of bigger amounts of data between the microcontroller software and, e.g., an external programmer connected to a CAN or LIN bus. The watchdog is running in time-out mode and its period can be selected from the full range of available values including longer times compared to Normal mode. The control of other resources – power supplies, transceivers, WU pin, interrupt requests, etc. – remains identical to Normal mode.

Flash mode can be entered by a specific SPI request in Start-up or Normal mode. The entry into Flash is accompanied by a reset pulse with “Flash requested” flag. Similarly, Flash mode can be left by an SPI request which will result in a reset pulse with “Flash exit requested” flag. Reset-source information in the SPI flags then allows the application to branch in function of the Flash mode. The handling of Flash mode requests is shown in Figure 13.

In SW Development configuration, CAN and both LIN transceivers are automatically put to their Normal mode when the device enters Flash operating mode.

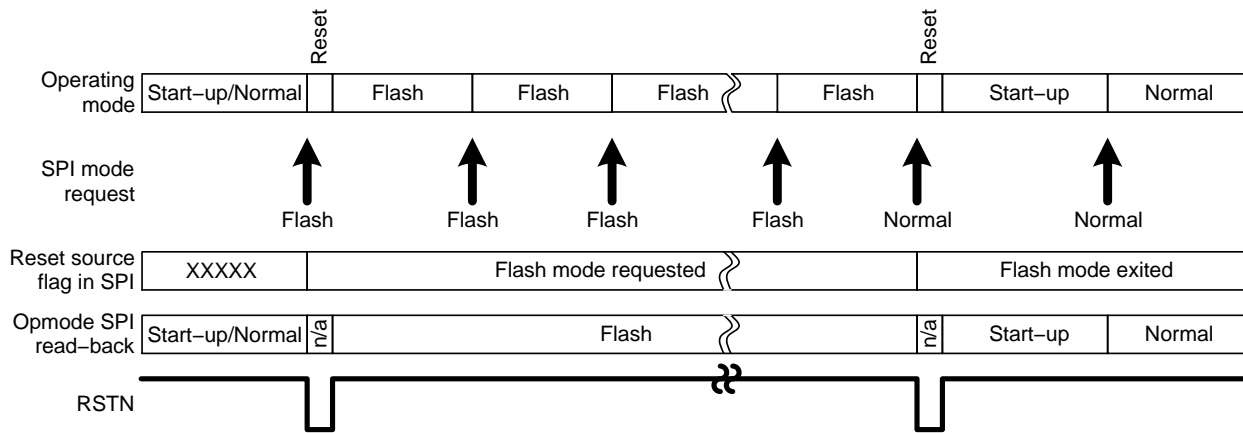


Figure 13. Flash Mode Sequence

Watchdog

The NCV7471B/C watchdog timer monitors the correct function of the application software – the microcontroller is required to send correct and timely watchdog-service (or “WD trigger”) SPI messages. A failure in the watchdog service is handled in function of the chip’s configuration (see the Configuration Mode section): it leads to a reset, to the Fail-safe mode entry or – in the SW Development configuration – generates an interrupt event (maskable).

The available modes of the watchdog timer are shown in Figure 14, with the watchdog period specified in Figure 15:

- Time-out mode watchdog:** the microcontroller is expected to send the watchdog-service SPI message any time before the watchdog period elapses. The time-out watchdog mode is automatically used during Start-up and Flash modes. It can be used in Standby and Normal modes. In Standby and Flash modes, the watchdog period can be selected from a broader range of values compared to the Normal mode.

- Window mode watchdog:** the microcontroller must send the required SPI message during an “open window” – this window is situated between 50% and 100% of the watchdog period. A watchdog-service SPI message sent before or after the open window is treated as a watchdog failure. The window watchdog can be used during the Normal mode.
- Off:** the watchdog will be inactive by default in Shut-down, Configuration, Power-up, Reset, and Fail-safe modes. It can be requested to be off in the Standby mode.
- Timer Wakeup:** in the Standby mode, the watchdog timer can be configured to generate wakeup events. In the Standby mode an interrupt request will be generated with a period defined by the watchdog setting.

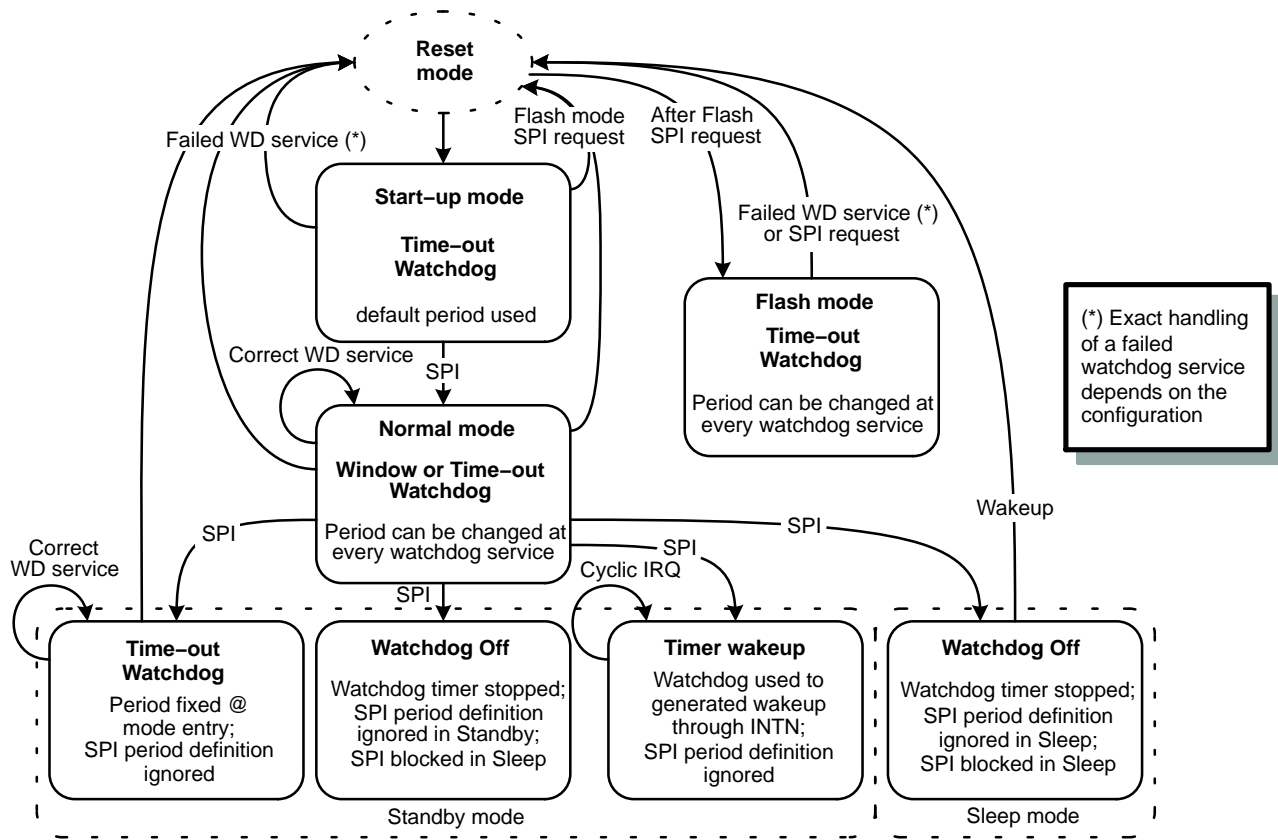


Figure 14. Watchdog Modes

A watchdog-service corresponds to a write access to SPI CONTROL0 register, containing watchdog mode, watchdog period and operating mode settings. The CSN rising edge of the CONTROL0 SPI write access is considered as the watchdog trigger moment. The watchdog service is evaluated as successful if all below conditions are fulfilled:

- The write SPI frame is valid
- The watchdog trigger moment falls into the correct watchdog trigger interval (see Figure 15) – in the case of the time-out watchdog, it arrives before the watchdog period expires; in the case of the window watchdog, it arrives during the second half of the window interval. In both cases, tolerance of the watchdog timing parameters shall be taken into account.
- The requested watchdog mode and the requested operating mode form an allowed combination

The watchdog period value written during a successful watchdog service is immediately used during the subsequent operation.

In the SW Development configuration, a failed watchdog service does not lead either to Reset or to Fail-safe mode:

- A failed WD service event is stored into the corresponding SPI register
- If the event is not masked, an interrupt request is generated.
- If a time-out watchdog is missed in the Start-up operating mode, Start-up mode is kept, and the watchdog is restarted with the default time-out period.
- If a too early window WD service is encountered in the Normal mode, a new watchdog period will be immediately started with the newly written settings; Normal mode is preserved
- If a window-watchdog is missed in the Normal mode (no service arrives), a new watchdog period will be immediately started with the current settings; Normal mode is preserved
- If a time-out watchdog is missed in the Standby mode, a new time-out watchdog period is immediately started with the same period; Standby mode is preserved

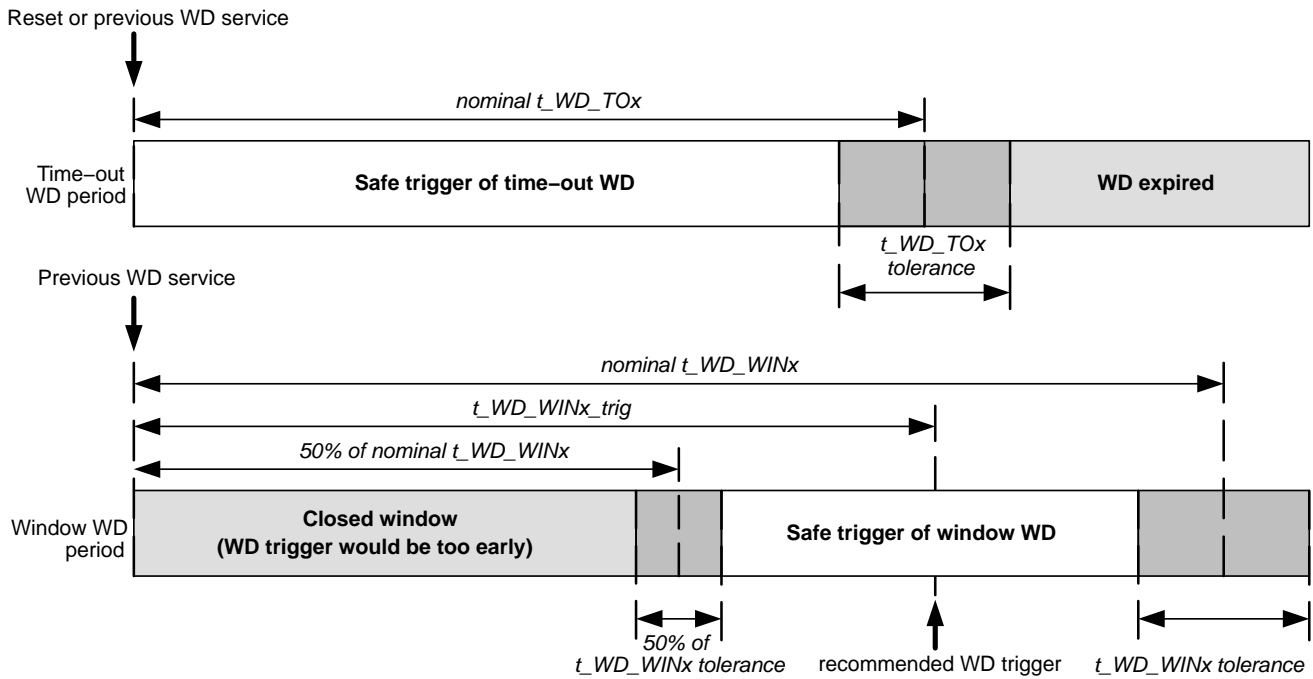


Figure 15. Structure of the Time-out and Window Watchdog Period

System Reset

A reset to the application microcontroller is signaled by Low level on the RSTN pin. RSTN pin is a bidirectional digital pin using an open-drain output structure with an internal pull-up resistor. An external reset source can overrule the High level generated by NCV7471B on RSTN pin. The RSTN logical level is then a superposition of the internally and externally driven reset request.

The RSTN pin level is compared with the internally driven RSTN signal – the comparison is used to control the operating mode of the circuit and to monitor a clamped condition of the RSTN pin – see Table 9.

With the exception of the SW Development configuration, applying an external reset during the Start-up mode will result in the FSO outputs activation. This condition fosters that the external MCU sends at least one correct watchdog message before applying an external reset.

Table 9. RSTN PIN FUNCTION (“X” Means “Don’t Care”)

| | RSTN | | Configuration | Mode | Action |
|---------------------------------|-------------------|-------------------|-------------------|---------------------------------------|---|
| | internally driven | sensed at the pin | | | |
| RSTN pin follows internal drive | Low | Low | X | X | Follow normal state diagram |
| | High | High | X | X | Follow normal state diagram |
| RSTN pin clamped High | Low | High | X | Configuration, Power-up, Reset, Sleep | Go to Fail-safe after $t_{RSTN_ClampedHigh}$ |
| RSTN pin clamped Low | High | Low | X | Normal, Standby, Flash | Go to Reset mode after t_{RSTN_filt} |
| | | | Config 1, 2, 3, 4 | Start-up | Go to Reset mode after t_{RSTN_filt} ; activate FSO |
| | | | SW Development | Start-up | Go to Reset mode after t_{RSTN_filt} ; do NOT activate FSOx |
| | | | Config 1 and 3 | Trying to exit Reset mode | Keep Reset mode; activate FSOx after $t_{RSTN_ClampedLow}$ |
| | | | Config 2 and 4 | Trying to exit Reset mode | Keep Reset mode Go to Fail-safe after $t_{RSTN_ClampedLow}$ |
| | | | SW Development | Trying to exit Reset mode | Keep Reset mode do NOT go to Fail-safe do NOT activate FSOx |

Event Flags and Interrupt Requests

An interrupt request can be signaled by the NCV7471B/C to the attached microcontroller via the open-drain output pin INTN. The active level of the INTN pin is logical Low. Pin INTN is provided with an internal pull-up resistor. An additional external pull-up is recommended – see Figure 2. The interrupt request generation is available during the Start-up, Normal, Standby and Flash modes.

The following events are handled by the interrupt sub-system:

- CAN, LIN and WU wakeups (cannot be masked)
- Timer wakeup in Standby mode (cannot be masked)
- VOUT2 supply crossing the under-voltage level in either direction if VOUT2 is on
- VOUT2 supply crossing the over-voltage level in either direction
- TxD dominant time-out for CAN or LINx (valid only if the respective transceiver is configured in its normal mode)
- The junction temperature crosses the thermal warning level in either direction
- Internal DC/DC converter signals changing their status – these events indicate entering or leaving limit conditions for both stages of the converter (run-state of the boost, overload of the boost or buck, out-of-regulation state of buck)

- Watchdog missed in SW Development configuration

If an event is encountered, it always causes the corresponding SPI flag go High. If the event is masked by the SPI interrupt mask setting (the corresponding mask bit is Low), pin INTN will not be forced Low and no interrupt request will be issued. The interrupt flag remains available for later readout until the next read-and-clear access through the SPI interface. TxD dominant time-out flags will remain set even after a read&clear access if the excessively long dominant signal is still present on the corresponding TxD pin. Note, that wakeup events cannot be masked. An overview of event flags is given in Table 10.

In case an un-masked interrupt event takes place, not only the corresponding event flag is set High, but also INTN pin is driven Low for t_{INTN_active} , indicating an interrupt request to the microcontroller. The microcontroller software is expected to read and clear the interrupt status register, otherwise the interrupt request remains pending (with the exception of flagRES_SWD). Pending or new interrupt requests will lead to a new INTN Low pulse no sooner than $t_{INTN_inactive}$ after the previous pulse. In this way, it is ensured that multiple new or pending interrupts will not slow-down the execution of the application software. Control of the INTN pin in conjunction with the internal flags is illustrated in Figure 16.

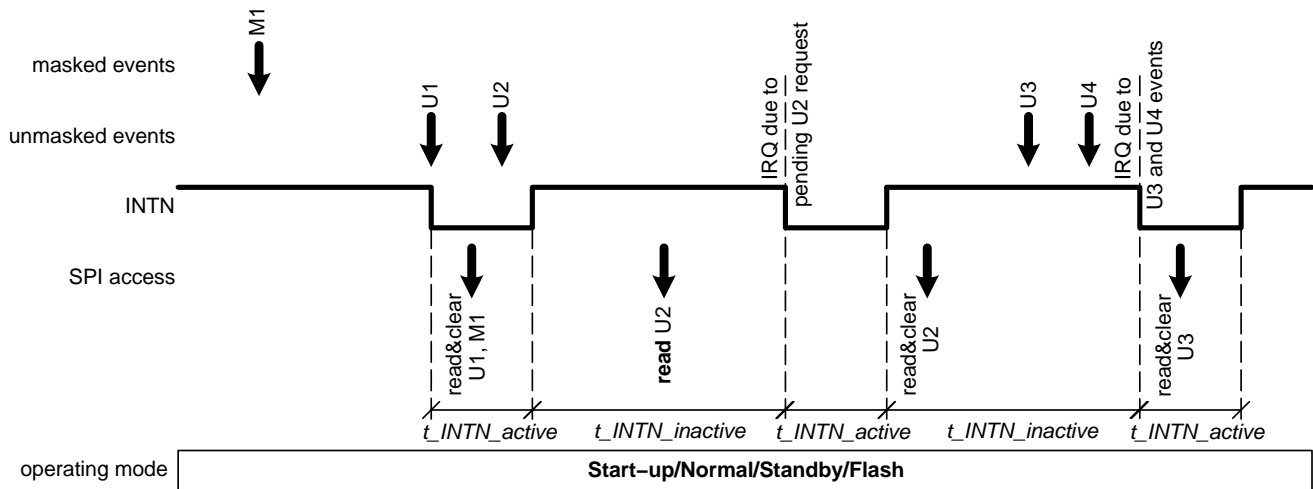


Figure 16. Interrupt Request Handling in Start-up, Normal, Standby and Flash Modes

In order to prevent that a pending interrupt request gets ignored by the application software, NCV7471B/C offers the following mechanisms:

- All event flags are preserved when transitioning from Start-up to Normal mode – see Figure 17.
- All event flags are preserved when transitioning from Standby to Normal mode – see Figure 17.
- All event flags are preserved when transitioning from Normal to Standby mode. If Standby mode is requested while an un-masked interrupt is pending, a new

interrupt request is issued according the $t_{INTN_inactive}$ timing – see Figure 18.

- If Sleep mode is requested while a wakeup flag is pending, the chip immediately performs a “wakeup from Sleep” mode sequence – see Figure 19. In this way, the information on the pending wakeup is not missed by the application.

Any transition through the Reset mode erases all SPI event flags, except the wakeup flags, and sets all maskable events to masked (i.e. not causing an interrupt request).

Table 10. EVENT FLAGS SUMMARY

| | Event Flag Bit | Related Status Bit (Note 1) | Related Interrupt Mask Bit | Set Condition | Reset Condition |
|----------------------|----------------------|-----------------------------|--|--|---|
| TxDx Time-out | flagTO_TxDC | none | intenTO_TxDC | TxDx (Note 2) pin is kept Low for longer than the time-out period and corresponding transceiver in normal mode | read&clear access to register STATUS0 and {TxDx (Note 2) dominant time-out condition disappeared or transceiver mode other than "normal"} |
| | flagTO_TxDL1 | | intenTO_TxDL1 | | |
| | flagTO_TxDL2 | | intenTO_TxDL2 | | |
| SMPS | flagBUCK_NOREG | statBUCK_NOREG | intenBUCK_NOREG | BUCK SMPS stage enters or leaves range of no regulation (i.e. extreme switching duty cycle); indicates (in)ability to reach nominal VOUT | read&clear access to register STATUS0 |
| | flagBUCK_OL | statBUCK_OL | intenBUCK_OL | BUCK SMPS stage enters or leaves over-load condition (i.e. current limitation encountered or disappeared) | |
| | flagBOOST_RUN | statBOOST_RUN | intenBOOST_RUN | BOOST SMPS stage changes activity – it starts or stops | |
| | flagBOOST_OL | statBOOST_OL | intenBOOST_OL | BOOST SMPS stage enters or leaves over-load condition (i.e. current limitation encountered or disappeared) | |
| flagTWAR | statTWAR | intenTWAR | junction temperature crosses the warning level in either direction | | |
| flagRES_SWD (Note 4) | none | intenRES_SWD | incorrect watchdog service encountered and device in SW Development configuration | | |
| VOUT2 | flagVOUT2_UV | statVOUT2_UV | intenVOUT2_UV | VOUT2 under-voltage detector changes state in either direction and VOUT2 is switched on | |
| | flagVOUT2_OV | statVOUT2_OV | intenVOUT2_OV | VOUT2 over-voltage detector changes state in either direction | |
| | flagSPIFail (Note 5) | none | intenSPIFail | SPI frame failure occurs: – number of SPI clocks different from 0 or 16, or – SCK High when CSN changes state | |
| Wakeup | flagWakeWU | none | none | WU wakeup detected (Note 3) | Read&clear access to register STATUS1 |
| | flagWakeCAN | | | CAN wakeup detected (Note 3) | |
| | flagWakeLIN1 | | | LIN1 wakeup detected (Note 3) | |
| | flagWakeLIN2 | | | LIN2 wakeup detected (Note 3) | |
| | flagWakeTimer | | | Timer wakeup detected (Note 3) | |

1. When a related status bit exists, the event is linked to a change (in either direction) of the status bit. Even if the event flag is cleared, the corresponding status bit still indicates the current status of the observed feature and can be polled by SPI at any time.
2. "x" = "C", "L1 or "L2". In case of LIN transceivers, the time-out feature can be enabled/disabled by SPI.
3. The respective wakeup source must be enabled through the corresponding control SPI register – timer wakeup in CONTROL0; CAN, LIN1/2 and WU wakeups in CONTROL1
4. For a missed WD in SW Development, INTN pulse is generated only once per event – it is not repeated even if the corresponding flag is still set. New INTN pulse occurs only if WD is missed again in SW Development.
5. During VOUT power-up (e.g. when going from Shut-down mode, or when waking-up from Sleep or Fail-safe mode), flagSPIFail can be set because of transient toggling of internal CSN and SCK signals. It is therefore recommended to ignore flagSPIFail immediately after VOUT power-up, until the STATUS0 register is reset. Except flagSPIFail, the remaining SPI register content is not influenced by the possible internal toggling of CSN and SCK signals during power-up.

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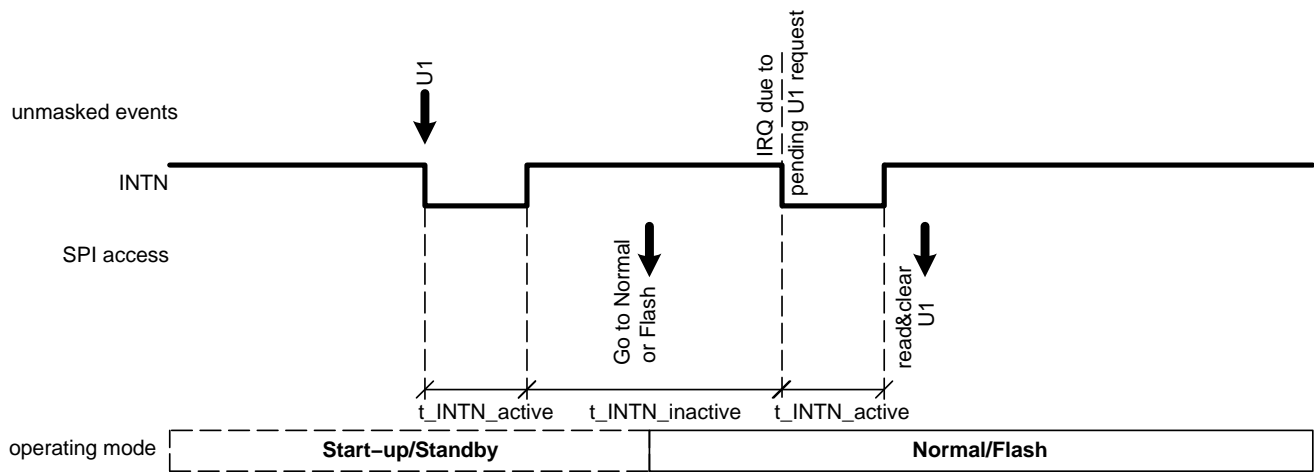


Figure 17. Interrupt Request Handling during a Transition to Normal Mode

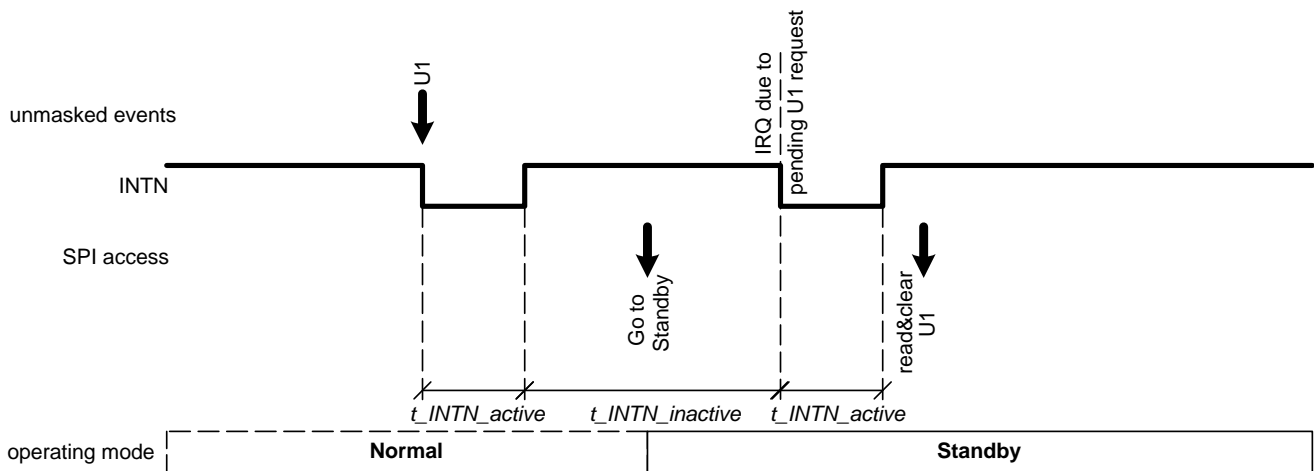


Figure 18. Transition to Standby Mode with a Pending Interrupt Request

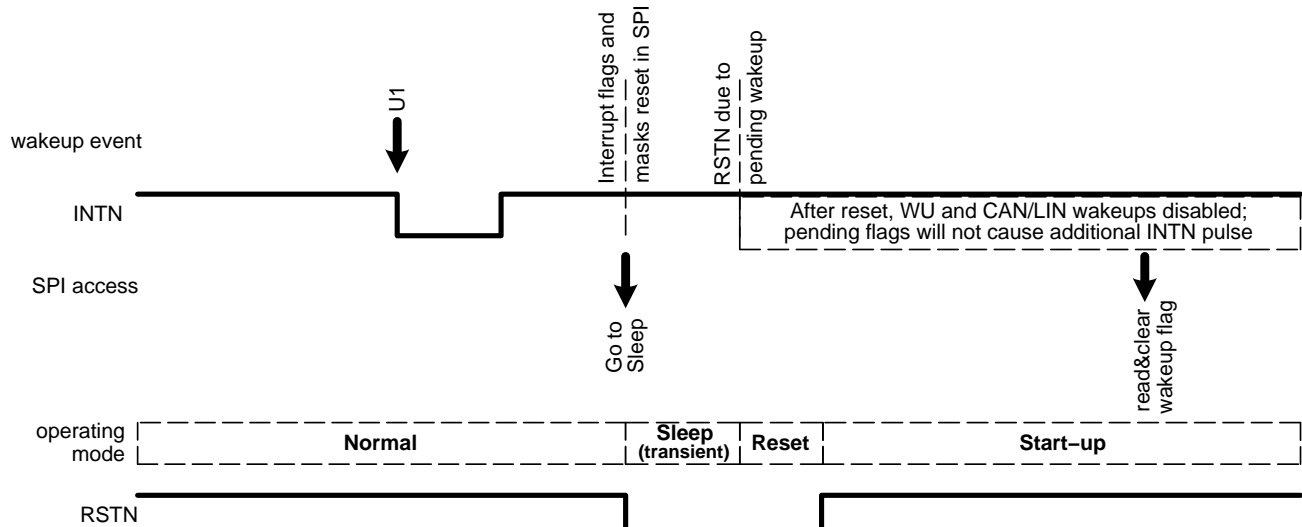


Figure 19. Attempted Transition to Sleep Mode with a Pending Wakeup Flag

Junction Temperature Monitoring

The device junction temperature is monitored in order to avoid permanent degradation or damage of the chip. Two distinct junction temperature thresholds are used:

- Thermal warning level T_{j_WAR} . The status of the current junction temperature compared with the T_{j_WAR} threshold is available in the corresponding SPI status register. A change of the junction temperature across the warning threshold in either direction sets the SPI bit flagTWAR. If not masked, an interrupt request can be generated in order to signal to the application that the junction temperature exceeded or cooled below the warning level.

- Thermal shut-down level T_{j_SD} . Junction temperature exceeding the shut-down level puts the chip into Fail-safe mode. In this specific case, no wakeups are detected in the Fail-safe mode; the mode is automatically left only when the junction cools down below the warning level, thus providing a thermal margin for the application software to cope with the event.

The junction temperature monitoring circuit is active in all operating modes with VOUT supply switched on (Power-up, Reset, Start-up, Standby, Flash) and also in the Fail-safe, provided that it has been entered as the consequence of a thermal shut-down. The function of the junction temperature monitoring of NCV7471B is shown in Figure 20.

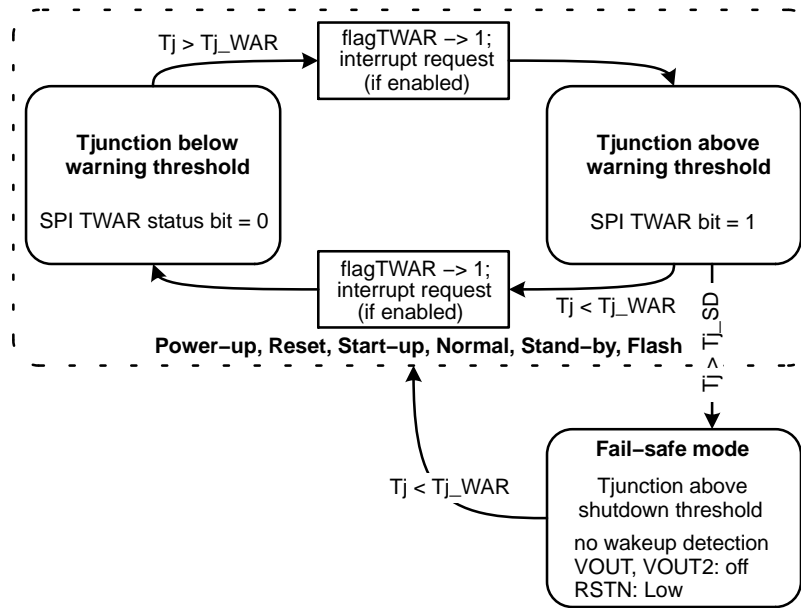


Figure 20. Junction Temperature Monitoring

FSO1/2/3 – Fail-Safe Outputs

NCV7471B/C offers three digital outputs dedicated to control a fail-safe circuitry in the application under specific failure conditions. All three outputs are high-voltage low-side open drain drivers simultaneously activated by a common internal signal FSO_internal and providing different behavior:

- FSO1 is constantly pulled Low if FSO_internal is active

- FSO2 provides 50% rectangular signal with 1.25 Hz frequency
- FSO3 provides 20% rectangular signal with 100 Hz frequency

Figure 21 illustrates the FSOx pins function with respect to the internal FSO_internal signal.

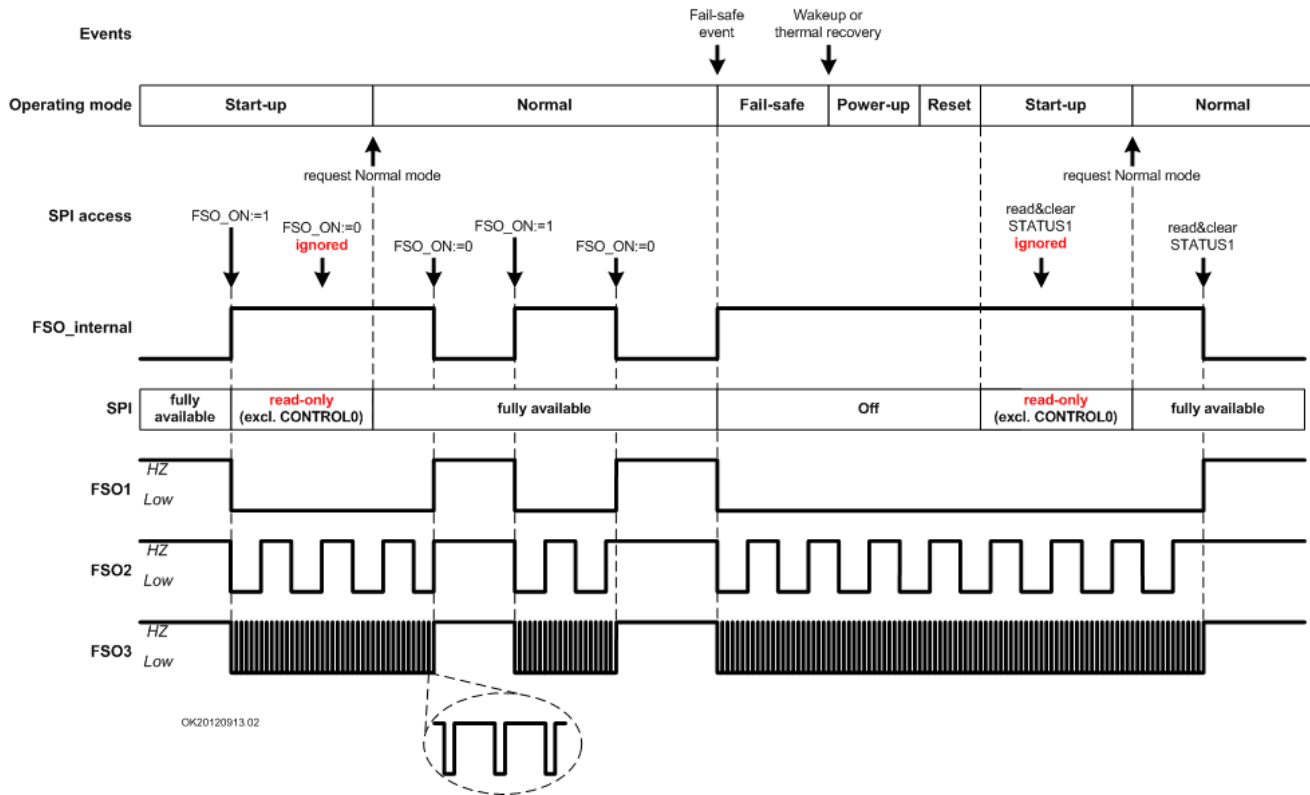


Figure 21. Operation of FSOx Pins

FSO_internal is set to High as soon as a failure condition is recognized or as soon as an SPI command is given to activate FSO. Overview of situations leading to FSO_internal activation is given in Table 11. The handling of the different failure conditions depends on the chip configuration (see the Configuration Mode section) – specifically in the SW development configuration, the watchdog-related failures and “RSTN clamped Low” failure do not lead either to the FSO_internal activation or to the Fail-safe mode entry.

FSO_internal signal will be reset (and the FSOx outputs are subsequently de-activated) under the following conditions:

- If FSO_internal was set by setting the FSO_ON SPI bit, it will be reset by writing “0” to FSO_ON SPI bit
- If FSO_internal was set because of a failure condition, a read-and-clear access to the flagFSO SPI status bits will reset it.

In Start-up mode, FSO_internal High level limits SPI functionality – no register can be written or read&cleared with the exception of CONTROL0 register. Attempts to perform a write or read&clear access to other registers will be ignored – including attempts to reset bit FSO_ON or the flagFSO.x bits. This condition ensures that the application software performs at least one successful watchdog service after a failure occurs.

Table 11. CONDITIONS FOR ACTIVATION OF FSO_INTERNAL SIGNAL (“X” Means “Don’t Care”)

| FSO Activation Event | Detected in Modes | Detected in Configurations | Fail-safe Mode Entered |
|--|---|----------------------------|------------------------|
| Thermal Shutdown ($T_j > T_{jsd}$) | Power-up Reset Start-up Normal Standby Flash | all | yes |
| Fatal VOUT failure ($V_{OUT} < V_{OUT_FAIL}$ for longer than $t_{V_{OUT_powerup}}$) | Power-up entered from all the modes | all | yes |
| VOUT undervoltage ($V_{OUT} < V_{OUT_RESx}$ for longer than $t_{V_{OUT_powerup}}$) | Power-up entered from Configuration, Sleep or Fail-safe | all | no |
| VOUT undervoltage ($V_{OUT} < V_{OUT_RESx}$ for longer than $t_{V_{OUT_UV_filt}}$) | Power-up entered from Start-up, Normal, Standby, Flash | all | no |
| RSTN Clamped High | Reset | all | yes |
| External RSTN without previous WD service | Start-up | Config 1,2,3,4 | no |
| RSTN Clamped Low | when trying to leave Reset | Config 1,3 | no |
| | | Config 2,4 | yes |
| 1 st Watchdog Missed | Start-up Normal Flash Standby (if WD on) | Config 1 | no |
| | | Config 2 | yes |
| 2 nd Watchdog Missed | Start-up Normal Flash Standby (if WD on) | Config 3 | no |
| | | Config 4 | yes |
| SPI control bit FSO set | Start-up Normal Standby Flash | all | no |

SWDM and CFG Digital Inputs

SWDM and CFG pins are high-voltage compliant digital inputs enabling NCV7471B/C flexibility with respect to the fail-safe behavior. Their logical value (compared to a low-voltage digital threshold) is sensed and latched exclusively in the Configuration operating mode – i.e. when the chip leaves the Shut-down mode. Subsequently, the latched values are not changed by any signal on SWDM or CFG pin or by any SPI communication.

Latched active level on SWDM pin (i.e. High input level in the Configuration mode) causes the chip to enter the SW development configuration regardless the state of CFG pin. When the latched SWDM value is inactive (i.e. Low in the Configuration mode), the latched CFG value then controls whether a failure condition (missed watchdog or RSTN clamped Low) results in the Fail-safe entry or only in a reset pulse generation. More details are given in the Configuration Mode and FSO1/2/3 – Fail-Safe Outputs sections.

SPI – Serial Peripheral Interface

SPI Frame Format

The Serial Peripheral Interface ensures control of NCV7471B operating modes, configuration of its functions and read-out of internal status and system information. The serial communication is achieved via SPI frames shown in Figure 22.

As long as the CSN chip select is High, the SCK and SDI inputs are not relevant and the SDO output is kept high-impedant. The signals on the SDI and SCK inputs are taken into account only when CSN chip select input is set to Low. Data incoming on pin SDI are then sampled at the falling edge of SCK clock signal; output data are shifted to pin SDO at the rising edge of SCK clock signal. Bits are transmitted MSB (most significant bit) first.

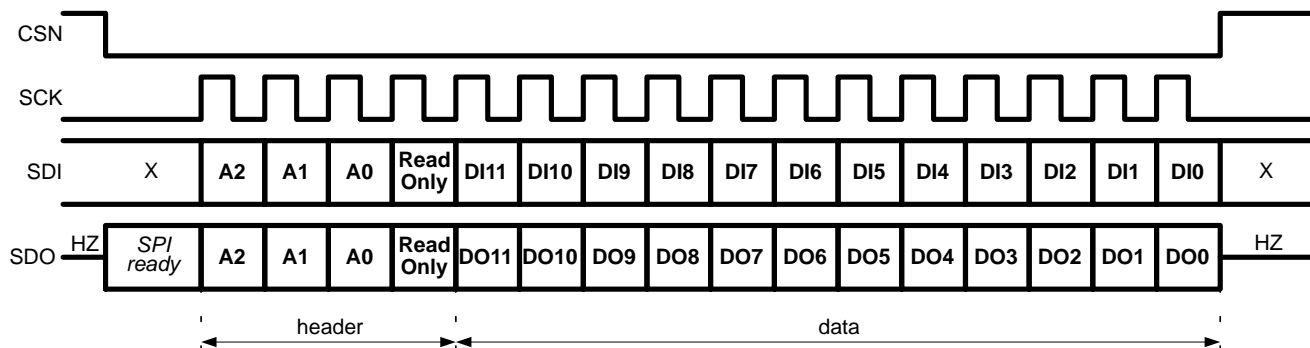


Figure 22. SPI Frame Format

One frame consists of exactly sixteen bits transferred from the microcontroller to NCV7471B/C through input pin SDI. The input bits are interpreted as follows:

- Immediately after CSN falling edge, SDO pin shows an internal “SPI ready” flag. Under normal conditions, when the inter-frame space is respected, the “SPI ready” flag is set to High and the device is available for SPI communication. If the SPI inter-frame space is violated, the previous SPI data might not be processed at the moment of the next CSN Low level; this situation is signaled by Low “SPI ready” flag. If the application software still attempts to perform SPI communication, incoming data will be completely ignored and the SDO signals “Low” throughout the SPI frame. The status of the flag is latched at the CSN falling edge – the application software might use short Low pulses on CSN (without SCK) in order to poll the flag.
- Four most significant bits form the header of the SPI frame. During the reception of the header bits, the SDI signal is looped back to the SDO pin starting with the first rising edge of SCK – except for the internal delay, signals SDO and SDI are equal during the header transmission. The header bits have the following function:
 - ♦ Bits A2, A1, and A0 form a 3-bit address of an internal SPI register. NCV7471B contains eight twelve-bit registers addressable by these three header bits.

- ♦ Bit “ReadOnly” contains the “read-only” flag. If ReadOnly=High, the current SPI frame represents a read-only access to the SPI register. If ReadOnly=Low, then the current SPI frame represents either a write or read-and-clear access to an SPI register – the distinction between “write” and “read-and-clear” access depends on the specific register.
- Bits DI11–DI0 are the SPI data. In case of a read-only or read-and-clear access, these bits are ignored. In case of a write-frame, these bits are taken as the new SPI register content at the moment of the CSN rising edge (when the frame is considered finished). Regardless the access type, the output data DO11–DO0 represent the SPI register content as valid at the beginning of the SPI frame. The output bits are shifted-out at the rising edge of the SCK clock so that they can be sampled by the microcontroller at the SCK falling edge. The following checks are performed on every SPI frame:
 - The SCK clock input must be Low at both edges of the CSN chip select signal
 - There must be exactly sixteen SCK clock cycles when CSN=Low (or no SCK edge if only the “SPI ready” flag is polled).

If any of the above conditions is not fulfilled, the SPI frame is considered incorrect and the “SPI Fail” event is internally generated.

SPI Register Mapping

Table 12. SPI REGISTERS MAPPING

| Address | | | Register Name | Register Content | | | | | | | | | | | | |
|---------|----|----|-----------------|------------------|---------------|----------------|-----------------|---------------|----------------|---------------|------------|--------------|--------------|---------------|---------------|--------|
| A2 | A1 | A0 | | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | CONTROL0 | OPMODE.2 | OPMODE.1 | OPMODE.0 | WD_MOD.1 | WD_MOD.0 | WD_PER.2 | WD_PER.1 | WD_PER.0 | CHECKSUM | reserved | reserved | reserved | input |
| 0 | 0 | 1 | CONTROL1 | reserved | enVOUT2 | modWU.1 | modWU.0 | modCAN.1 | modCAN.0 | enLIN_LSLP | disTO_TxDL | modLIN2.1 | modLIN2.0 | modLIN1.1 | modLIN1.0 | output |
| 0 | 1 | 0 | CONTROL2 | reserved | reserved | reserved | reserved | reserved | FSO_ON | FAST_FSO | VOUT_RES.1 | VOUT_RES.0 | modDCDC.1 | modDCDC.0 | enBOOST | |
| 0 | 1 | 1 | CONTROL3 | intenTO_TxDC | intenTO_TxDL1 | intenTO_TxDL2 | intenBUCK_NOREG | intenBUCK_OL | intenBOOST_RUN | intenBOOST_OL | intenTWAR | intenRES_SWD | ntenVOUT2_UV | intenVOUT2_OV | intenSPIFail | |
| 1 | 0 | 0 | STATUS0 | flagTO_TxDC | flagTO_TxDL1 | flagTO_TxDL2 | flagBUCK_NOREG | flagBUCK_OL | flagBOOST_RUN | flagBOOST_OL | flagTWAR | flagRES_SWD | flagVOUT2_UV | flagVOUT2_OV | flagSPIFail | |
| 1 | 0 | 1 | STATUS1 | reserved | reserved | reserved | flagFSO.3 | flagFSO.2 | flagFSO.1 | flagFSO.0 | flagWakeWU | flagWakeCAN | flagWakeLIN1 | flagWakeLIN2 | flagWakeTimer | |
| 1 | 1 | 0 | STATUS2 | reserved | statVS_LOW | statBUCK_NOREG | statBUCK_OL | statBOOST_RUN | statBOOST_OL | statSWDM | statCFG | statWU | statTWAR | statVOUT2_UV | statVOUT2_OV | |
| 1 | 1 | 1 | GENERAL PURPOSE | GPD.11 | GPD.10 | GPD.9 | GPD.8 | GPD.7 | GPD.6 | GPD.5 | GPD.4 | GPD.3 | GPD.2 | GPD.1 | GPD.0 | |

NOTE: "reserved" bits in input data are ignored; they are set to Low in output data.

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Table 13. SPI REGISTERS INITIALIZATION

| Address | | | Register Name | Initialization | | ReadOnly bit | |
|---------|----|----|-----------------|---|---|---|--|
| A2 | A1 | A0 | | Initialized in (Note 6) | Initial content | Low (Note 7) | High |
| 0 | 0 | 0 | CONTROL0 | Reset mode (except Flash mode entry) | Watchdog set to time-out @ 256 ms nominal | Mode and Watchdog settings (bits DI11–DI4) written into the register if checksum (bit DI3) is OK. Input bits DI2–DI0 ignored. | Input data ignored; current register content sent to SPI output |
| 0 | 0 | 1 | CONTROL1 | Power-up mode | all bits Low (Note 9) | Bits DI11–DI0 written into the register | |
| | | | | Reset mode | all bits Low (Note 9) | | |
| 0 | 1 | 0 | CONTROL2 | Configuration | all bits Low | Bits DI11–DI0 written into the register | |
| | | | | Sleep | all bits Low | | |
| 0 | 1 | 1 | CONTROL3 | Reset mode | all bits Low | Bits DI11–DI0 written into the register | |
| 1 | 0 | 0 | STATUS0 | Reset mode | all bits Low | read&clear access; all bits reset to Low (Note 8); input data ignored | |
| 1 | 0 | 1 | STATUS1 | Configuration mode | all bits Low | read&clear access; all bits reset to Low; input data ignored | |
| 1 | 1 | 0 | STATUS2 | n.a. | Reflects status of internal blocks | input data ignored | |
| 1 | 1 | 1 | GENERAL PURPOSE | Configuration mode | register filled with device ID data | Bits DI11–DI0 written into the register | |

6. In modes not explicitly listed in “Initialized in” column, the register content is preserved
7. Regardless the access type (the “ReadOnly” bit), the current register content is always sent to the SPI output
8. Bits containing TxD dominant timeout flags will remain set if the excessively long dominant signal persists on the respective TxDx pin
9. Exception: in SW Development configuration, CONTROL1 bits modCAN.x, modLIN1.x and modLIN2.x are all set to “High”, corresponding to the default “Normal” mode of all transceivers

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CONTROL0 Register (Address 000)

By a write access to the CONTROL0 register (“ReadOnly” = Low), the application software can control the operating mode of NCV7471B/C and the watchdog settings. A write access represents a watchdog service. An operating mode change is therefore always synchronized with the watchdog trigger message. In order to provide more safety to the mode control, the input data are protected with a check-sum (input bit DI3). The checksum must correspond to the following formula (symbol “⊕” denoting the exclusive-or operation):

$$DI3 = DI11 \oplus DI10 \oplus DI9 \oplus DI8 \oplus DI7 \oplus DI6 \oplus DI5 \oplus DI4$$

In case of incorrect checksum in written data, the device reacts identically to a wrong opmode situation. During a read-only access to the CONTROL0 register (“ReadOnly” = High), the input data are completely ignored and no check is performed on them.

The output data of the CONTROL0 register – regardless the access type – indicate the current operating mode, the current watchdog settings and the cause of the last reset.

The initialization of the CONTROL0 register content is performed after every reset, when the watchdog type is fixed to time-out, and the watchdog period to nominally 256 ms.

Table 14. CONTROL0 REGISTER: OPMODE.x Encoding

| OPMODE.2 | OPMODE.1 | OPMODE.0 | OPMODE.x in Input Data | | | | | OPMODE.x in Output Data |
|----------|----------|----------|------------------------|--|-----------------------|----------------------|--|-------------------------|
| | | | Requested Mode | Reaction in Start-up | Reaction in Normal | Reaction in Standby | Reaction in Flash | Current Mode |
| 0 | 0 | 0 | forbidden | “Wrong Opmode” Reset | | | | Start-up |
| 0 | 0 | 1 | Normal | go to Normal | keep Normal | go to Normal | return from Flash via Reset and Start-up | Normal |
| 0 | 1 | 0 | Standby | “Wrong Opmode” Reset | go to Standby | keep Standby | “Wrong Opmode” Reset | Standby |
| 0 | 1 | 1 | Sleep | “Wrong Opmode” Reset | go to Sleep | “Wrong Opmode” Reset | | not used |
| 1 | 0 | 0 | Flash | go to Flash via Reset | go to Flash via Reset | “Wrong Opmode” Reset | keep Flash | Flash |
| 1 | 0 | 1 | Fail-safe | in SW development configuration, go to Fail-safe; otherwise “Wrong Opmode” Reset | | | | not used |
| 1 | 1 | 0 | Reset | go to Reset | | | | not used |
| 1 | 1 | 1 | Configuration | go to Configuration | go to Configuration | “Wrong Opmode” Reset | | not used |

Table 15. CONTROL0 REGISTER: WD_MOD.x Encoding

| WD_MOD.1 | WD_MOD.0 | Watchdog Timer Mode | Limitations (if not respected, the write access is considered as a missed watchdog) |
|----------|----------|---------------------|---|
| 0 | 0 | Watchdog off | Can be used only with a Standby or a Sleep mode request |
| 0 | 1 | Window Watchdog | Can be used only for Normal mode request |
| 1 | 0 | Time-out Watchdog | Must be used with every Flash mode request; can be used with a Standby or Normal mode request; default in Start-up mode |
| 1 | 1 | Timer Wakeup | Can be used only with a Standby mode request |

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Table 16. CONTROL0 REGISTER: WD_PER.x Encoding

| WD_PER.2 | WD_PER.1 | WD_PER.0 | Watchdog Period | Nominal Duration | Note |
|----------|----------|----------|-----------------|------------------|---|
| 0 | 0 | 0 | WD_PER_0 | 8 ms | |
| 0 | 0 | 1 | WD_PER_1 | 16 ms | |
| 0 | 1 | 0 | WD_PER_2 | 32 ms | |
| 0 | 1 | 1 | WD_PER_3 | 64 ms | |
| 1 | 0 | 0 | WD_PER_4 | 128 ms | |
| 1 | 0 | 1 | WD_PER_5 | 256 ms | WD_PER_5 is automatically used in Start-up mode |
| 1 | 1 | 0 | WD_PER_6 | 512 ms | Can be used only for Standby and Flash modes (otherwise the watchdog SPI frame is considered wrong) |
| 1 | 1 | 1 | WD_PER_7 | 1024 ms | |

Table 17. CONTROL0 REGISTER: RES_SRC.x Encoding

| RES_SRC.3 | RES_SRC.2 | RES_SRC.1 | RES_SRC.0 | Cause of the Last RSTN Pulse | Reset Event Priority (Note 10) |
|-----------|-----------|-----------|-----------|---|--------------------------------|
| 0 | 0 | 0 | 0 | V_MID under-voltage recovery (V_IN connection) | 12 |
| 0 | 0 | 0 | 1 | External reset outside Start-up mode (not accompanied by FSO activation) | 10 |
| 0 | 0 | 1 | 0 | Recovery from Fail-safe (through wakeup or thermal shutdown recovery) | 8 |
| 0 | 0 | 1 | 1 | Wakeup from Sleep | 7 |
| 0 | 1 | 0 | 0 | Flash mode requested | 6 |
| 0 | 1 | 0 | 1 | Flash mode exited | 5 |
| 0 | 1 | 1 | 0 | Reset mode requested | 4 |
| 0 | 1 | 1 | 1 | Configuration requested | 3 |
| 1 | 0 | 0 | 0 | Failed Watchdog (WD missed, wrong WD mode or period requested) – will not be used in SW Development configuration (Note 11) | 2 |
| 1 | 0 | 0 | 1 | Wrong operating mode requested; wrong checksum during write access to the Mode Control register | 1 |
| 1 | 0 | 1 | 0 | External reset in Start-up mode (accompanied by FSO activation if not in SW Development configuration) | 9 |
| 1 | 0 | 1 | 1 | reserved | – |
| 1 | 1 | 0 | 0 | reserved | – |
| 1 | 1 | 0 | 1 | reserved | – |
| 1 | 1 | 1 | 0 | reserved | – |
| 1 | 1 | 1 | 1 | VOUT under-voltage recovery | 11 |

10. The “Reset Event Priority” reflects the order, in which the reset events are processed by the on-chip digital. In case more events occur simultaneously, the one with the lower priority number would be stored in CONTROL0 register.

11. WD period and WD mode settings are not checked in the following situations: Configuration mode request, Reset mode request, Flash exit (i.e. Normal mode request in the course of Flash mode)

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CONTROL1 Register (Address 001)

CONTROL1 register defines the mode of individual CAN and LINx transceivers, of the VOUT2 regulator and the WU pin. The encoding of the CONTROL1 bits is defined in Table 18.

Table 18. CONTROL1 REGISTER ENCODING

| enVOUT2 | | VOUT2 control |
|------------|-----------|--|
| 0 | | VOUT2 regulator is OFF |
| 1 | | VOUT2 regulator is ON |
| modWU.1 | modWU.0 | WU mode control |
| 0 | 0 | WU wakeup detection disabled |
| 0 | 1 | WU monitored for falling edge |
| 1 | 0 | WU monitored for rising edge |
| 1 | 1 | WU monitored for both edges |
| modCAN.1 | modCAN.0 | CAN transceiver mode |
| 0 | 0 | CAN transceiver in Off mode |
| 0 | 1 | CAN transceiver in Wakeup mode |
| 1 | 0 | CAN transceiver in Receive-only mode |
| 1 | 1 | CAN transceiver in Normal mode |
| enLIN_LSLP | | LIN slope control – common for both LIN channels |
| 0 | | LIN transmission with normal bus signal slopes (according LIN2.1 specification) |
| 1 | | LIN transmission with slow bus signal slopes (for limited bit-rate) |
| disTO_TxDL | | LIN dominant time-out control – common for both LIN channels |
| 0 | | Dominant time-out applied on TxDL pins |
| 1 | | Dominant time-out not-applied on TxDL pins – unlimited dominant symbols can be transmitted |
| modLINx.1 | modLINx.0 | LINx transceiver mode (x=1,2) |
| 0 | 0 | LINx transceiver in Off mode |
| 0 | 1 | LINx transceiver in Wakeup mode |
| 1 | 0 | LINx transceiver in Receive-only mode |
| 1 | 1 | LINx transceiver in Normal mode |

CONTROL1 register is initialized at every reset event with all-zeros content

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CONTROL2 Register (Address 010)

Content of CONTROL2 register is defined in Table 19. The CONTROL2 register content is initialized to all–zeros content in the Configuration and Sleep modes.

Table 19. CONTROL2 REGISTER ENCODING

| Bit | | Definition |
|-------------------|-------------------|--|
| FSO_ON | | If High, FSOx outputs are forced active |
| FAST_FSO | | If High, already the 1 st missed watchdog will be treated as a failure; the exact reaction depends on the configuration |
| VOUT_RES.1 | VOUT_RES.0 | Selection of VOUT under–voltage threshold for RSTN Pin |
| 0 | 0 | VOUT_RES4 threshold selected (the lowest threshold) for RSTN indication |
| 0 | 1 | VOUT_RES3 threshold selected for RSTN indication |
| 1 | 0 | VOUT_RES2 threshold selected for RSTN indication |
| 1 | 1 | VOUT_RES1 threshold selected for RSTN indication |
| modDCDC.1 | modDCDC.0 | DCDC Converter mode selection |
| 0 | 0 | DCDC Converter switching with fixed frequency |
| 0 | 1 | Converter switching frequency modulated with modulation depth dmod_DCDC_1 |
| 1 | 0 | Converter switching frequency modulated with modulation depth dmod_DCDC_2 |
| 1 | 1 | Converter switching frequency modulated with modulation depth dmod_DCDC_3 |
| enBOOST | | If High, BOOST (step–up) stage of the DCDC converter is enabled |

CONTROL3 Register (Address 011)

The individual bits in the CONTROL3 register determine whether the corresponding interrupt event leads to an interrupt request via INTN pin or if it is only stored as a flag for later SPI retrieval. If the bit is High, the interrupt request

is enabled. All bits of the CONTROL3 register are reset to Low at every reset event (i.e. all interrupt sources are disabled).

Table 20. CONTROL3 REGISTER ENCODING

| Bit | Definition |
|-----------------|---|
| intenTO_TxDC | Enables interrupt after dominant time–out on TxDC |
| intenTO_TxDL1 | Enables interrupt after dominant time–out on TxDL1 |
| intenTO_TxDL2 | Enables interrupt after dominant time–out on TxDL2 |
| intenBUCK_NOREG | Enables interrupt after a change of the internal converter signal indicating, that the buck stage cannot reach the output nominal voltage (typically due to too low line voltage) |
| intenBUCK_OL | Enables interrupt after a change of the internal converter signal indicating, that the buck stage is overloaded |
| intenBOOST_RUN | Enables interrupt when the boost stage is activated or de–activated – indicating a change in supply line conditions |
| intenBOOST_OL | Enables interrupt after a change of the internal converter signal indicating, that the boost stage is overloaded |
| intenTWAR | Enables interrupt when the junction temperature crosses the thermal warning level (in either direction) |
| intenRES_SW | In SW Development configuration only – incorrect watchdog service will lead to an interrupt request (outside SW Development configuration, this event would lead to reset). |
| intenVOUT2_UV | Enables interrupt when VOUT2 crosses its under–voltage level (in either direction). Event registered only if VOUT2 is on. |
| intenVOUT2_OV | Enables interrupt when VOUT2 crosses its over–voltage level (in either direction). |
| intenSPIFail | Enables interrupt when an SPI frame failure is encountered |

STATUS0 Register (Address 100)

STATUS0 bits latch information on individual events which can potentially lead to interrupt requests. All bits have their position corresponding to the CONTROL3 register bits. The details of the STATUS0 bits are given in Table 21.

A read-and-clear access to STATUS0 register is considered “interrupt service” for all pending interrupt requests. A read-only access does not change the flags and the active interrupt requests remain pending.

Specifically, flags corresponding to dominant time-outs can be cleared only when the respective time-out disappeared; otherwise, they will remain set even after read&clear access and, if enabled, the interrupt linked to them will remain pending.

STATUS0 register is reset to all-zeros content at every reset event.

Table 21. STATUS0 REGISTER ENCODING

| Bit | Definition |
|----------------|---|
| flagTO_TxDC | TxDC dominant time-out occurred. The bit can be cleared only when the time-out condition disappeared (or when the CAN transceiver mode was changed to other than “CAN Normal”). |
| flagTO_TxDL1 | TxDL1 dominant time-out occurred. The bit can be cleared only when the time-out condition disappeared (or when the LIN1 transceiver mode was changed to other than “LIN Normal”). |
| flagTO_TxDL2 | TxDL2 dominant time-out occurred. The bit can be cleared only when the time-out condition disappeared (or when the LIN2 transceiver mode was changed to other than “LIN Normal”). |
| flagBUCK_NOREG | Flags a change of the internal converter signal indicating, that the buck stage cannot reach the output nominal voltage (typically due to too low line voltage) |
| flagBUCK_OL | Flags a change of the internal converter signal indicating, that the buck stage is overloaded |
| flagBOOST_RUN | Boost stage toggled its state (was activated or de-activated) – indicating a change in supply line conditions |
| flagBOOST_OL | Flags a change of the internal converter signal indicating, that the boost stage is overloaded |
| flagTWAR | Junction temperature crossed the thermal warning level (in either direction) |
| flagRES_SWD | In SW Development configuration only – incorrect watchdog service occurred |
| flagVOUT2_UV | VOUT2 crossed its under-voltage level (in either direction). Event registered only if VOUT2 is on. |
| flagVOUT2_OV | VOUT2 crossed its over-voltage level (in either direction). |
| flagSPIFail | SPI frame failure was encountered (Note 12) |

12. During VOUT power-up (e.g. when going from Shut-down mode, or when waking-up from Sleep or Fail-safe mode), flagSPIFail can be set because of transient toggling of internal CSN and SCK signals. It is therefore recommended to ignore flagSPIFail immediately after VOUT power-up, until the STATUS0 register is reset. Except flagSPIFail, the remaining SPI register content is not influenced by the possible internal toggling of CSN and SCK signals during power-up.

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STATUS1 Register (Address 101)

STATUS1 register contains flags for fail-safe events and wakeups. A specific bit (flag) is set High when the corresponding event was recognized and is set to Low only when the STATUS1 register is read and cleared. The

STATUS1 register is initialized in Configuration mode to all-zeros content. It is not reset in Reset or Start-up mode in order to preserve the wakeup and failure flags coming from Sleep or Fail-safe mode. Encoding of the FSO-related flag bits is defined in Table 22.

Table 22. STATUS1 REGISTER: flagFSO.x Encoding

| flagFSO.3 | flagFSO.2 | flagFSO.1 | flagFSO.0 | Failure event leading to FSOx activation |
|-----------|-----------|-----------|-----------|---|
| 0 | 0 | 0 | 0 | no failure, FSOx inactive (unless over-ruled by FSO_ON bit) |
| 0 | 0 | 0 | 1 | FSOx active due to missed watchdog; without entry into Fail-safe mode |
| 0 | 0 | 1 | 0 | FSOx active due to "RSTN clamped Low"; without entry into Fail-safe mode |
| 0 | 0 | 1 | 1 | FSOx active due to external reset in Start-up mode; without entry into Fail-safe mode (not detected in SW Development configuration) |
| 0 | 1 | 0 | 0 | reserved |
| 0 | 1 | 0 | 1 | reserved |
| 0 | 1 | 1 | 0 | reserved |
| 0 | 1 | 1 | 1 | reserved |
| 1 | 0 | 0 | 0 | FSOx active; coming from Fail-safe mode requested by SPI |
| 1 | 0 | 0 | 1 | FSOx active; coming from Fail-safe mode caused by missed watchdog |
| 1 | 0 | 1 | 0 | FSOx active; coming from Fail-safe mode caused by "RSTN clamped Low" |
| 1 | 0 | 1 | 1 | FSOx active; coming from Fail-safe mode caused by "RSTN clamped High" |
| 1 | 1 | 0 | 0 | FSOx active; coming from Fail-safe mode caused by thermal shutdown |
| 1 | 1 | 0 | 1 | FSOx active; coming from Fail-safe mode caused by VOUT undervoltage time-out (short-circuit detected) or FSOx active due to VOUT undervoltage |
| 1 | 1 | 1 | 0 | reserved |
| 1 | 1 | 1 | 1 | reserved |

Wakeup flag bits are summarized in Table 23. Detection of individual wakeup events is controlled by transceiver mode settings (for LIN and CAN wakeup), WU pin mode settings (for WU wakeup) and watchdog settings (for timer wakeup). A wakeup event is indicated either by an interrupt

request (in Normal or Standby mode) or by a reset pulse (wakeups from Sleep mode). In Normal and Standby mode, a wakeup causes pending interrupt request until a read-and-clear access to STATUS1 register.

Table 23. STATUS1 REGISTER: Wakeup Flags

| Bit | Definition |
|---------------|--|
| flagWakeWU | Wakeup on WU pin was detected (for non-zero setting of modWU.x SPI bits) |
| flagWakeCAN | Wakeup on CAN bus was detected (CAN transceiver in "CAN Wakeup" mode) |
| flagWakeLIN1 | Wakeup on LIN1 bus was detected (LIN1 transceiver in "LIN Wakeup" mode) |
| flagWakeLIN2 | Wakeup on LIN2 bus was detected (LIN2 transceiver in "LIN Wakeup" mode) |
| flagWakeTimer | Wakeup by timer ("Timer wakeup" selected through CONTROL0 register) |

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STATUS2 Register (Address 110)

STATUS2 register bits reflect the state of several internal blocks of the device. Read-and-clear or write access does not change the register content. The STATUS2 bits are defined in Table 24.

Table 24. STATUS2 REGISTER ENCODING

| Bit | Definition |
|----------------|---|
| statVS_LOW | Indication of the VS monitoring output. If $VS < VS_MON$, then $statVS_LOW = 1$ |
| statBUCK_NOREG | Indication of the buck DCDC stage not being able to reach the nominal VOUT voltage |
| statBUCK_OL | Indication of the buck DCDC stage overload |
| statBOOST_RUN | Indication that the boost DCDC stage is running (boost stage must be enabled and the input voltage requires step-up operation) |
| statBOOST_OL | Indication of the boost DCDC stage overload |
| statSWDM | Logical level of the SWDM pin latched during Configuration mode |
| statCFG | Logical level on the CFG pin latched during Configuration mode (in Config 1,2,3,4) or Current logical level on CFG pin (in SW Development) |
| statWU | Logical level on the WU pin |
| statTWAR | Output of the thermal warning comparator (if High, junction temperature is above the warning level) |
| statVOUT2_UV | Output of the VOUT2 under-voltage comparator (if High, VOUT2 is below the under-voltage level). Available only if VOUT2 regulator is on. |
| statVOUT2_OV | Output of the VOUT2 over-voltage comparator (if High, VOUT2 is above the over-voltage level) |

GENERAL PURPOSE Register (Address 111)

General Purpose register allows storing general 12-bit information in the NCV7471B/C memory. The register is initialized only in Configuration mode, when a device version ID is loaded. Any data written to the register overwrite the initial content and are kept throughout the

operation of the device until device enters Shut-down mode or until Configuration is requested.

The device ID is:

- 0x384 for NCV7471B
- 0x3C4 for NCV7471C

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Table 25. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Units |
|-------------------------|---|----------|-----------|-------|
| Vmax_VS | Maximum voltage at VS pin | -0.3 | 40 | V |
| Vmax_VS_VOUT2 | Maximum voltage at VS_VOUT2 pin | -0.3 | 40 | V |
| Vmax_BOOST | Maximum voltage at BOOST pin | -0.3 | V_MID+2 | V |
| Vmax_V_MID | Maximum voltage at V_MID pin | -0.3 | 40 | V |
| Vmax_BUCK | Maximum DC voltage at BUCK pin Maximum transient voltage on BUCK pin (Note 13) | -1 -3 | V_MID+0.3 | V |
| Vmax_VOUT | Maximum voltage at VOUT pin | -0.3 | 6 | V |
| Vmax_VOUT2 | Maximum voltage at VOUT2 pin | -1 | 40 | V |
| Vmax_VCC_CAN | Maximum voltage at VCC_CAN pin | -0.3 | 6 | V |
| Vmax_CANH, Vmax_CANL | Maximum voltage at CAN bus pins (0 < VCC_CAN < 5.25 V; no time limit) | -50 | 50 | V |
| Vmax_CANH-CANL | Maximum voltage between CAN bus pins | -50 | 50 | V |
| Vmax_LINx | Maximum voltage at LIN bus pins | -45 | 45 | V |
| Vmax_FSOx | Maximum voltage at FSOx pins | -0.3 | 40 | V |
| Vmax_WU | Maximum voltage at WU pin | -40 | 40 | V |
| Vmax_CFG; Vmax_SWDM | Maximum voltage at CFG and SWDM pins | -0.3 | 40 | V |
| Vmax_digIn | Maximum voltage at digital input and open-drain pins (TxDLx, TxDC, SCK, SDI, INTN, RSTN, UVN_VOUT) | -0.3 | 6 | V |
| Vmax_digOut | Maximum voltage at digital push-pull output pins (RxDLx, RxDC, SDO) | -0.3 | VOUT+0.3 | V |
| Vmax_CSN | Maximum voltage at CSN pin | -0.3 | 40 | V |
| Tjunc_max | Junction temperature | -40 | +170 | °C |
| V_ESD | System ESD on pins CANH, CANL, LIN1, LIN2, VOUT2, VS, VS_VOUT2, WU as per IEC 61000-4-2: 330 Ω / 150 pF | ≥ ±6 | | kV |
| | Human body model on pins CANH, CANL, LIN1, LIN2 stressed towards GND with 1500 Ω / 100 pF | ≥ ±6 | | kV |
| | Human body model on pins VS, VS_VOUT2, WU stressed towards GND with 1500 Ω / 100 pF | ≥ ±4 | | kV |
| | Human body model on all pins as per JESD22-A114 / AEC-Q100-002 | ≥ ±2 | | kV |
| | Charge device model on all pins as per JESD22-C101 / AEC-Q100-011 | ≥ ±500 | | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

13. BUCK pin tolerates transient voltage excursions below -1 V, caused by the buck-converter switching and the non-ideal characteristics of diode D2 (see Figure 2). It is not implied that a hard voltage source of less than -1 V can be connected to the pin externally.

Table 26. THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Units |
|------------------|-------------------------------------|-------|-------|
| R _{θJC} | Thermal resistance junction-to-case | 3.9 | °C/W |

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Table 27. OPERATING RANGES

| Symbol | Parameter | Min | Max | Units |
|-----------------------|---|-------|------------|-------|
| Vop_V_IN_boostbuck | V_IN operating voltage for boost/buck operation | 2.5 | 28 | V |
| Vop_V_IN_buck | V_IN operating voltage for buck-only operation | 6 | 28 | V |
| Vop_VS | Operating voltage at VS pin | 6 | 28 | V |
| Vop_VS_VOUT2 | Operating DC voltage at VS_VOUT2 pin | 6 | 28 | V |
| Vop_BOOST | Operating voltage at BOOST pin | 0 | V_MID+V_D1 | V |
| Vop_V_MID | Operating voltage at V_MID pin | 5.5 | 28 | V |
| Vop_BUCK | Operating voltage at BUCK pin | -V_D2 | V_MID | V |
| Vop_VOUT | Regulated voltage at VOUT2 supply output | 4.9 | 5.1 | V |
| Vop_VOUT2 | Regulated voltage at VOUT2 supply output | 4.9 | 5.1 | V |
| Vop_VCC_CAN_normal | Operating voltage at VCC_CAN pin for normal and receive only CAN modes | 4.75 | 5.25 | V |
| Vop_VCC_CAN_lowpower | Operating voltage at VCC_CAN pin for wakeup and off CAN modes | 0 | 5.25 | V |
| Vop_CANH, Vop_CANL | Operating voltage at CAN bus pins | 0 | VCC_CAN | V |
| Vop_LINx | Operating voltage at LIN bus pins | 0 | VS | V |
| Vop_FSOx | Operating voltage at FSOx pins | 0 | VS | V |
| Vop_WU | Operating voltage at WU pin | 0 | VS | V |
| Vop_CFG; Vop_SWDM | Operating voltage at CFG and SWDM pins | 0 | VS | V |
| Vop_digIO | Operating voltage at digital input and output pins (TxDLx, RxDLx, TxDC, RxDC, SCK, CSN, SDI, SDO, INTN, RSTN, UVN_VOUT) | 0 | VOUT | V |
| Tjunc_op | Junction temperature | -40 | +150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS

The characteristics defined in this section are guaranteed within the operating ranges listed in Table 27, unless stated otherwise. Positive currents flow into the respective pin.

Power Supply

Table 28. SUPPLY MONITORING ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|---------------|------|------|------|------|
| V_MID_PORH | V_MID threshold for the power-up of the circuit | V_MID rising | 3.3 | 3.7 | 4 | V |
| V_MID_PORL | V_MID threshold for the shut-down of the circuit | V_MID falling | 2.2 | 2.65 | 3 | V |
| VS_MON | Monitoring level on VS pin defining the operation of the LIN transceivers | VS falling | 3 | | 5.2 | V |
| VS_MON_hys | Hysteresis of the VS monitor | | | 0.12 | | V |
| t_VS_MON_filt | VS monitoring filter time | | | 16 | 25 | μs |
| VOUT_RES1 | VOUT monitoring threshold 1 | VOUT falling | 4.55 | 4.65 | 4.75 | V |
| VOUT_RES2 | VOUT monitoring threshold 2 | VOUT falling | 3.8 | 3.9 | 4.0 | V |
| VOUT_RES3 | VOUT monitoring threshold 3 | VOUT falling | 3.35 | 3.45 | 3.55 | V |
| VOUT_RES4 | VOUT monitoring threshold 4 | VOUT falling | 3.0 | 3.1 | 3.2 | V |
| VOUT_RES_hys | VOUT monitoring threshold hysteresis | | 0.03 | 0.1 | 0.14 | V |
| VOUT_FAIL | VOUT failure threshold | VOUT rising | | 2 | | V |
| t_VOUT_UV_filt | Undervoltage detection filter time | | | 16 | 25 | μs |
| t_VOUT_powerup | VOUT undervoltage time-out for short-circuit recognition w.r.t. VOUT_FAIL threshold | | 1.35 | 1.5 | 1.65 | s |
| t_VOUT_reset | RSTN pulse extension | | 4.5 | 5 | 5.5 | ms |
| VOUT2_UV | VOUT2 under-voltage threshold | VOUT2 falling | 4.45 | 4.65 | 4.75 | V |
| VOUT2_UV_hys | VOUT2 under-voltage threshold hysteresis | | | 0.1 | | V |
| t_VOUT2_UV_filt | Undervoltage detection filter time | | | 16 | 25 | μs |
| VOUT2_OV | VOUT2 over-voltage threshold | | | 7 | | V |
| VOUT2_OV_hys | VOUT2 over-voltage threshold hysteresis | | | 0.1 | | V |
| t_VOUT2_OV_filt | Overvoltage detection filter time | | | 32 | 50 | μs |

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Table 29. DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|--|---------------|-----------|---------------|----------|
| VOUT | DCDC output voltage | NCV7471B/C in Normal or Standby; Suitable external components for the required load current and input voltage used. | 4.9 | 5.0 | 5.1 | V |
| I_OUT | DCDC output current available for ex- ternal loads (see Figure 2) | NCV7471B/C in Normal or Standby; function of external components | | | 500 | mA |
| Imaxpeak_BOOST | Maximum peak-current detection threshold in BOOST stage | $T_j \leq 0^\circ\text{C}$ $T_j > 0^\circ\text{C}$ | 1.6 1.6 | | 2.2 2.0 | A |
| Imaxpeak_BUCK | Maximum peak-current detection threshold in BUCK stage | | 0.8 | | 1.0 | A |
| V_MID_reg | Middle voltage level | Boosting active – NCV7471B – NCV7471C | 10.5 6.175 | 11 6.5 | 11.5 6.825 | V |
| Ron_BOOST | On-resistance of the boost-stage switch | | | | 0.45 | Ω |
| Ron_BUCK | On-resistance of the buck-stage switch | | | | 0.6 | Ω |
| V_MID_Ron | V_MID level for parametrical on-resist- ance of the converter switches | | 5 | | | V |
| fsw_DCDC | Constant switching frequency | | 450 | 485 | 520 | kHz |
| fmod_DCDC | Modulation frequency | Modulation enabled via SPI | 7 | 10 | 13 | kHz |
| dmod_DCDC_1 | Modulation depth 1 | | | 10 | | % |
| dmod_DCDC_2 | Modulation depth 2 | | | 20 | | % |
| dmod_DCDC_3 | Modulation depth 3 | | | 30 | | % |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 30. VOUT2 REGULATOR ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|--|--|------|------|------------|------|
| VOUT2 | VOUT2 regulator output voltage | VOUT2 regulator active; $I_{load}(VOUT2) \leq 5\text{ mA}$ | 4.95 | 5.0 | 5.05 | V |
| | | VOUT2 regulator active; $I_{load}(VOUT2) \leq 50\text{ mA}$ | 4.9 | 5.0 | 5.1 | V |
| VOUT2_drop | Drop-out voltage between VS_VOUT2 and VOUT2 | $I_{load}(VOUT2) = 50\text{ mA};$ $T_j \leq 25^\circ\text{C}$ $T_j > 25^\circ\text{C}$ | | 0.35 | 0.6 0.7 | V |
| Ilim_VOUT2 | VOUT2 current limitation | VOUT2 regulator active | | | -80 | mA |

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Table 31. CURRENT CONSUMPTIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--|---|-----|-----|---------------------------------|------|
| I _{VS} (Note 14) | VS consumption in LIN normal mode | LIN1 and LIN2 in Normal mode; recessive on both LIN buses | | | 3.2 | mA |
| | VS consumption with LIN in Wakeup or Off mode | LIN1 and LIN2 in LIN-wakeup or Off mode; no activity on both LIN buses; T _j ≤ 85°C | | | 8 | μA |
| I _{VS_VOUT2} (Note 14) | VS_VOUT2 consumption if VOUT2 is on | VOUT2 regulator is active | | | 30 μA + 1.1 x I(VOUT2) | – |
| | VS_VOUT2 consumption if VOUT2 is off | VOUT2 regulator is off; VS_VOUT2 ≤ 13.5 V; T _j ≤ 85°C | | | 1 | μA |
| I _{VCC_CAN} (Note 14) | VCC_CAN consumption for dominant transmission | CAN in Normal mode driving dominant on the CAN bus; 60 Ω load on the CAN pins | | | 75 | mA |
| | VCC_CAN consumption for recessive transmission | CAN in Receive-only mode or CAN in Normal mode with recessive on the bus | | | 10 | mA |
| | VCC_CAN consumption in CAN Wakeup mode | CAN Wakeup mode (CAN supplied from V _{MID}); Device in Standby or Sleep mode; no wakeup detected; VCC_CAN ≤ 5.1 V; T _j ≤ 85°C | | | 2 | μA |
| I _{IN} (Notes 14, 16) | DCDC input current in Standby or Normal mode | NCV7471B/C in Standby or Normal mode; V _{IN} (Note 15) = 13.5 V; T _j ≤ 85°C; no external VOUT load enBoost = Low; CAN in Off mode | | 70 | 95 | μA |
| | DCDC input current in Sleep mode | NCV7471B/C in Sleep mode; 5.5 V ≤ V _{IN} (Note 15) ≤ 18 V; T _j ≤ 85°C; enBoost = Low; CAN in Off mode | | 55 | 70 | μA |
| | I _{IN} adder for CAN wakeup | NCV7471B/C in Normal, Standby or Sleep mode; 5.5 V ≤ V _{IN} (Note 15) ≤ 18 V; T _j ≤ 85°C; CAN in Wakeup mode | | 10 | | μA |
| | I _{IN} adder for BOOST stage | NCV7471B/C in Standby or Normal mode; 5.5 V ≤ V _{IN} (Note 15) ≤ 18 V; T _j ≤ 85°C; enBoost = High; Boost-stage not switching | | 10 | | μA |

14. The supply currents are depicted in Figure 2.

15. V_{IN} is the DCDC input voltage – see Figure 2.

16. I_{IN} is the total DCDC input current, covering the quiescent consumption of the device (through pins BOOST, V_{MID}, BUCK and VOUT), the current into the external load, and the losses associated with the DCDC conversion.

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CAN Transceiver

Table 32. CAN TRANSCEIVER ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|--------------|----------|------------|---------|
| CAN TRANSMITTER DC CHARACTERISTICS | | | | | | |
| Vo(reces)(CANH) | recessive bus voltage at pin CANH | V(TxDC) = VOUT, no load, transmitter on | 2 | 2.5 | 3 | V |
| Vo(reces)(CANH) | recessive bus voltage at pin CANH | no load, transmitter off | -0.1 | 0 | 0.1 | V |
| Vo(reces)(CANL) | recessive bus voltage at pin CANL | V(TxDC) = VOUT, no load, transmitter on | 2 | 2.5 | 3 | V |
| Vo(reces)(CANL) | recessive bus voltage at pin CANL | no load, transmitter off | -0.1 | 0 | 0.1 | V |
| Io(reces)(CANH) | recessive output current at pin CANH | -35 V < V(CANH) < 35 V (Note 17), 0 V < VCC_CAN < 5.25 V | -2.5 | - | 2.5 | mA |
| Io(reces)(CANL) | recessive output current at pin CANL | -35 V < V(CANL) < 35 V (Note 17), 0 V < VCC_CAN < 5.25 V | -2.5 | - | 2.5 | mA |
| Vo(dom)(CANH) | dominant output voltage at pin CANH | V(TxDC) = 0 V 42.5 Ω < RL < 65 Ω | 3 | 3.6 | 4.25 | V |
| Vo(dom)(CANL) | dominant output voltage at pin CANL | V(TxDC) = 0 V 42.5 Ω < RL < 65 Ω | 0.5 | 1.4 | 1.75 | V |
| Vo(dif)(bus_dom) | differential bus output voltage (V(CANH) - V(CANL)) | V(TxDC) = 0 V 42.5 Ω < RL < 65 Ω | 1.5 | 2.25 | 3 | V |
| Vo(dif)(bus_dom_arb) | differential bus output voltage (V(CANH) - V(CANL)) | V(TxDC) = 0 V, RL = 2240 Ω Guaranteed by design | 1.5 | | 5 | V |
| Vo(sym)(bus_dom) | bus output voltage symmetry (V(CANH) + V(CANL)) | V(TxDC) = 0 V, TxDC = square wave up to 1 MHz | 0.9 | | 1.1 | VCC_CAN |
| Vo(dif)(bus_rec) | differential bus output voltage (V(CANH) - V(CANL)) | V(TxDC) = VOUT, recessive, no load | -120 | 0 | 50 | mV |
| Io(SC)(CANH) | short-circuit output current at pin CANH | V(TxDC) = 0 V V(CANH) = -3 V, -3 V < V(CANH) < 18 V | -100 -100 | -70 - | -45 1 | mA |
| Io(SC)(CANL) | short-circuit output current at pin CANL | V(TxDC) = 0 V V(CANL) = 36 V, -3 V < V(CANL) < 18 V | 45 -1 | 70 - | 100 100 | mA |
| CAN RECEIVER DC CHARACTERISTICS | | | | | | |
| Vi(dif)(th) | Differential receiver threshold voltage | -12 V < V(CANH) < 12 V, -12 V < V(CANL) < 12 V | 0.5 | 0.7 | 0.9 | V |
| Vi(rec)(bus_rec) | Differential receiver input voltage for recessive state | -12 V < V(CANH) < 12 V, -12 V < V(CANL) < 12 V | -3 | | 0.5 | V |
| Vi(rec)(bus_dom) | Differential receiver input voltage for dominant state | -12 V < V(CANH) < 12 V, -12 V < V(CANL) < 12 V | 0.9 | | 8 | V |
| Vihcm(dif)(th) | Differential receiver threshold voltage for high common mode | -35 V < V(CANH) < 35V, -35 V < V(CANL) < 35 V (Note 17) | 0.4 | 0.7 | 1 | V |
| Ri(cm)CANH | Common mode input resistance at pin CANH | | 15 | 26 | 37 | kΩ |
| Ri(cm)CANL | Common mode input resistance at pin CANL | | 15 | 26 | 37 | kΩ |
| Ri(cm)(m) | Matching between pin CANH and pin CANL common mode input resistance | V(CANH) = V(CANL) | -3 | 0 | 3 | % |

17. In production, the parameter is measured for common-mode range from -30 V to +35 V. The common mode range down to -35 V is guaranteed by design.

18. Bus load RL = 60 Ω, CL = 100 pF; C(RxDC) = 15 pF

19. Tested with TTL thresholds on TxDC/RxDC; assuming TxDC/RxDC fall/rise edges below 10 ns.

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Table 32. CAN TRANSCEIVER ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|------|------|------|------|
| CAN RECEIVER DC CHARACTERISTICS | | | | | | |
| Ri(dif) | Differential input resistance | | 25 | 50 | 75 | kΩ |
| CI(CANH) | input capacitance at pin CANH | V(TxDC) = VCC_CAN, not tested in production | – | 7.5 | 20 | pF |
| CI(CANL) | input capacitance at pin CANL | V(TxDC) = VCC_CAN, not tested in production | – | 7.5 | 20 | pF |
| CI(dif) | differential input capacitance | V(TxDC) = VCC_CAN, not tested in production | – | 3.75 | 10 | pF |
| ILI_CANH | Input leakage current at pin CANH | 0 Ω < R(VCC_CAN to GND) < 1 MΩ, V(CANH) = V(CANL) = 5 V | –5 | 0 | 5 | μA |
| ILI_CANL | Input leakage current at pin CANL | | –5 | 0 | 5 | μA |
| Vi(dif)(th) | Differential receiver threshold voltage for the wakeup detection | –12 V < V(CANH) < 12 V, –12 V < V(CANL) < 12 V | 0.4 | 0.8 | 1.15 | V |
| Vi(rec)(bus_rec) | Differential receiver input voltage for recessive state for wakeup detection | –12 V < V(CANH) < 12 V, –12 V < V(CANL) < 12 V | –3 | | 0.4 | V |
| Vi(rec)(bus_dom) | Differential receiver input voltage for dominant state for wakeup detection | –12 V < V(CANH) < 12 V, –12 V < V(CANL) < 12 V | 1.05 | | 8 | V |
| CAN TRANSCEIVER DYNAMIC CHARACTERISTICS | | | | | | |
| td(TxDC–BusOn) | delay TxDC to bus active | C _L = 100 pF between CANH – CANL | 5 | 85 | 110 | ns |
| td(TxDC–BusOff) | delay TxDC to bus inactive | C _L = 100 pF between CANH – CANL | 5 | 30 | 110 | ns |
| td(BusOn–RxDC) | delay bus active to RxDC | C(RxDC) = 15 pF | 5 | 55 | 110 | ns |
| td(BusOff–RxDC) | delay bus inactive to RxDC | C(RxDC) = 15 pF | 5 | 100 | 110 | ns |
| tdPD(TxDC–RxDC)dr | Propagation delay TxDC to RxDC | (Note 18) | 45 | | 245 | ns |
| tdPD(TxDC–RxDC)rd | Propagation delay TxDC to RxDC | (Note 18) | 45 | | 230 | ns |
| t_CAN_wake_dom | Dominant time for CAN wakeup | LP mode Vdif(dom) > 1.4 V | 0.5 | 2.5 | 5 | μs |
| | | LP mode Vdif(dom) > 1.2 V | 0.5 | 3 | 5.8 | μs |
| t_CAN_wake_rec | Recessive time for CAN wakeup | | 0.5 | 2.5 | 5 | μs |
| t_CAN_wake_timeout | Maximum length of the CAN wakeup pattern | | 0.9 | 1 | 1.1 | ms |
| T_TxDC_timeout | TxDC dominant time for time out | V(TxDC) = 0 V | 2.9 | 3.7 | 4.5 | ms |
| CAN TRANSCEIVER DYNAMIC CHARACTERISTICS | | | | | | |
| tBIT(RxDC500) | Bit time on RxDC pin | Tbit = 500 ns (Note 18, 19) | 400 | | 550 | ns |
| tBIT(RxDC200) | Bit time on RxDC pin | Tbit = 200 ns (Note 18, 19) | | 156 | | ns |
| tBIT(Vi(dif)500) | Bit time on CAN bus | Tbit = 500 ns (Note 18, 19) | 435 | | 530 | ns |
| tBIT(Vi(dif)200) | Bit time on CAN bus | Tbit = 200 ns (Note 18, 19) | | 172 | | ns |
| ΔtREC500 | Receiver timing symmetry | Tbit = 500 ns; ΔtREC = tBIT(RxDC) – tBIT(Vi(dif)) (Note 18, 19) | –65 | | 40 | ns |
| ΔtREC200 | Receiver timing symmetry | Tbit = 200 ns; ΔtREC = tBIT(RxDC) – tBIT(Vi(dif)) (Note 18, 19) | | –16 | | ns |

17. In production, the parameter is measured for common-mode range from –30 V to +35 V. The common mode range down to –35 V is guaranteed by design.

18. Bus load R_L = 60 Ω, C_L = 100 pF; C(RxDC) = 15 pF

19. Tested with TTL thresholds on TxDC/RxDC; assuming TxDC/RxDC fall/rise edges below 10 ns.

NCV7471B, NCV7471C

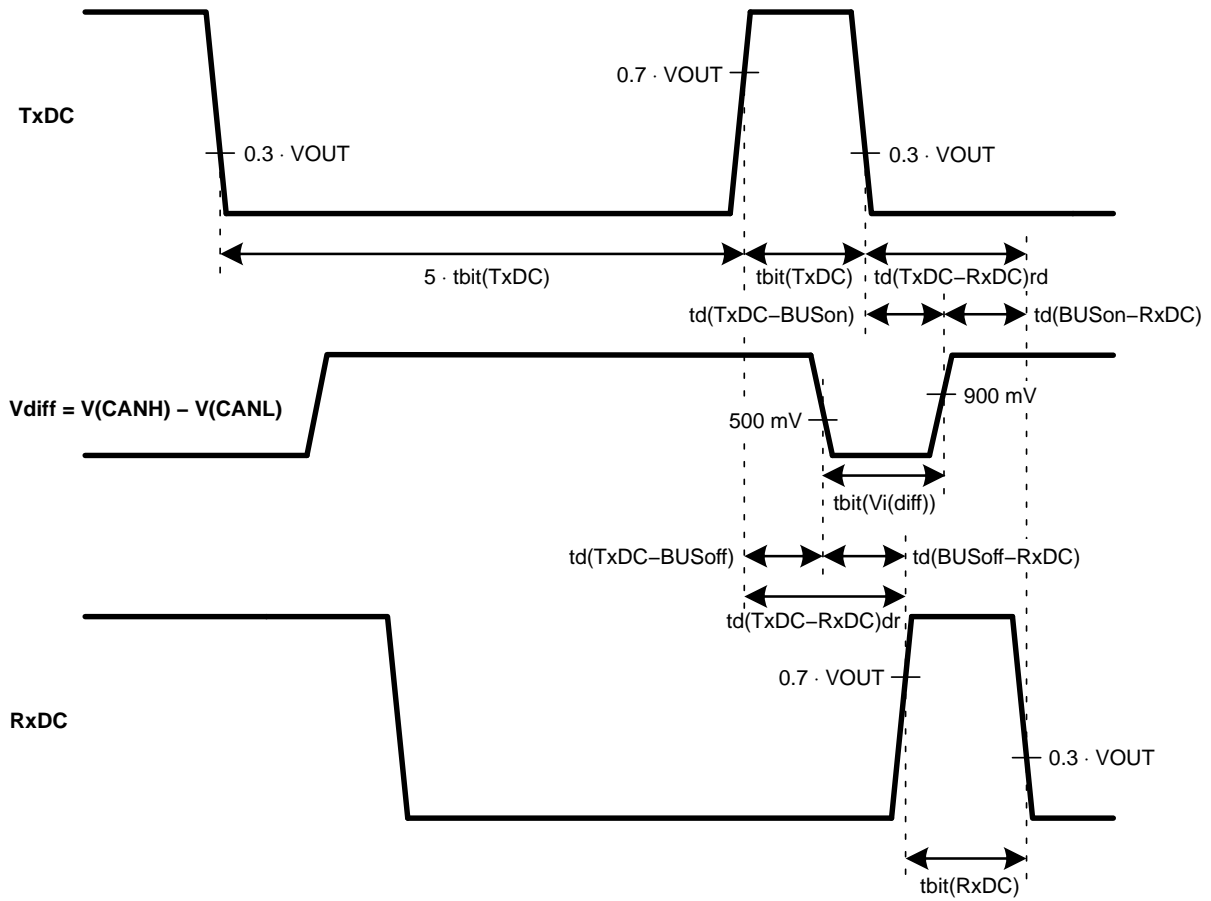


Figure 23. Definition of CAN Dynamic Parameters

NCV7471B, NCV7471C

LIN Transceivers

Table 33. LINx TRANSCIEVER ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|----------|-----|----------|------|
| LINx TRANSMITTER DC CHARACTERISTICS | | | | | | |
| VLIN_dom_LoSup | LIN dominant output voltage | TxDLx = Low; VS = 7.3 V | | | 1.2 | V |
| VLIN_dom_HiSup | LIN dominant output voltage | TxDLx = Low; VS = 18 V | | | 2.0 | V |
| VLIN_REC | LIN recessive output voltage | TxDLx = High; I(LIN) = 0 mA | VS – 1.2 | | VS – 0.3 | V |
| ILIN_lim | Short circuit current limitation | VLIN = VS = 18 V | 40 | | 200 | mA |
| Rslave | Internal pull-up resistance | LIN Normal or Receive-only mode | 20 | 33 | 47 | kΩ |
| LINx RECEIVER DC CHARACTERISTICS | | | | | | |
| Vbus_dom | Bus voltage for dominant state | | | | 0.4 | VS |
| Vbus_rec | Bus voltage for recessive state | | 0.6 | | | VS |
| Vrec_dom | Receiver threshold | LIN bus going from recessive to dominant | 0.4 | | 0.6 | VS |
| Vrec_rec | Receiver threshold | LIN bus going from dominant to recessive | 0.4 | | 0.6 | VS |
| Vrec_cnt | Receiver center voltage | (Vrec_dom + Vrec_rec)/2 | 0.475 | | 0.525 | VS |
| Vrec_hys | Receiver hysteresis | Vrec_rec – Vrec_dom | 0.05 | | 0.175 | VS |
| ILIN_off_dom | LIN output current, bus in dominant state | Normal LIN Mode, Driver Off; VS = 12 V; VLIN = 0 V | –1 | | | mA |
| ILIN_off_dom_slp | LIN output current, bus in dominant state | LIN Wake Mode, VS = 12 V; VLIN = 0 V | –20 | –15 | –2 | μA |
| ILIN_off_rec | LIN output current, bus in recessive state | Driver Off; VS < 18 V; VS < VLIN < 18 V | | | 1 | μA |
| ILIN_no_GND | LIN current with missing GND | VS = GND = 12 V; 0 V < VLIN < 18 V | –1 | | 1 | mA |
| ILIN_no_VS | LIN current with missing VS | VS = GND = 0 V; 0 V < VLIN < 18 V | | | 5 | μA |
| LINx TRANSCIEVER DYNAMIC CHARACTERISTICS | | | | | | |
| D1 | Duty Cycle 1 = tBUS_REC(min) / (2 x TBit) | THREC(max) = 0.744 x VS THDOM(max) = 0.581 x VS TBit = 50 μs V(VS) = 7 V to 18 V | 0.396 | | 0.5 | |
| D2 | Duty Cycle 2 = tBUS_REC(max) / (2 x TBit) | THREC(min) = 0.422 x VS THDOM(min) = 0.284 x VS TBit = 50 μs V(VS) = 7.6 V to 18 V | 0.5 | | 0.581 | |
| D3 | Duty Cycle 3 = tBUS_REC(min) / (2 x TBit) | THREC(max) = 0.778 x VS THDOM(max) = 0.616 x VS TBit = 96 μs V(VS) = 7 V to 18 V | 0.417 | | 0.5 | |
| D4 | Duty Cycle 4 = tBUS_REC(max) / (2 x TBit) | THREC(min) = 0.389 x VS THDOM(min) = 0.251 x VS TBit = 96 μs V(VS) = 7.6 V to 18 V | 0.5 | | 0.590 | |
| T_fall | LIN falling edge | Normal Mode; VS = 12 V | | | 22.5 | μs |
| T_rise | LIN rising edge | Normal Mode; VS = 12 V | | | 22.5 | μs |
| T_sym | LIN slope symmetry | Normal Mode; VS = 12 V | –4 | 0 | 4 | μs |
| Trec_prop_down | Propagation delay of receiver | Falling edge; C(RxDLx) = 20 pF | 0.1 | | 6 | μs |
| Trec_prop_up | | Rising edge; C(RxDLx) = 20 pF | 0.1 | | 6 | μs |
| Trec_sym | Propagation delay symmetry | Trec_prop_down – Trec_prop_up; C(RxDLx) = 20 pF | –2 | | 2 | μs |
| t_LIN_wake | Dominant duration for wakeup | LIN in wakeup mode | 30 | 90 | 150 | μs |

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Table 33. LINx TRANSCEIVER ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------------|--|-----|-----|-----|------|
| LINx TRANSCEIVER DYNAMIC CHARACTERISTICS | | | | | | |
| T_TxDLx_timeout | TxDLx dominant time-out | TxDLx = Low; LIN dominant time-out enabled | 6 | 13 | 20 | ms |
| C_LINx | Capacitance of the LINx pins | Guaranteed by design; not tested in production | | 15 | 25 | pF |

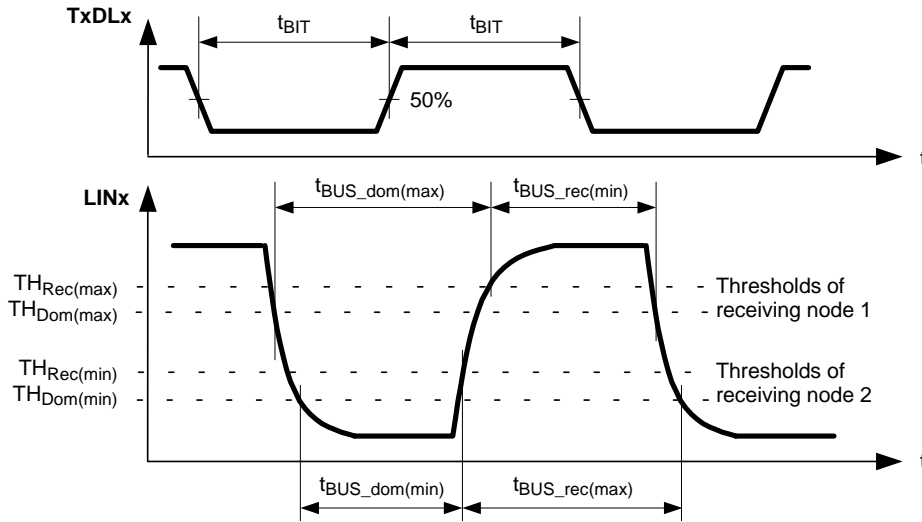


Figure 24. Definition of LINx Duty Cycle Parameters

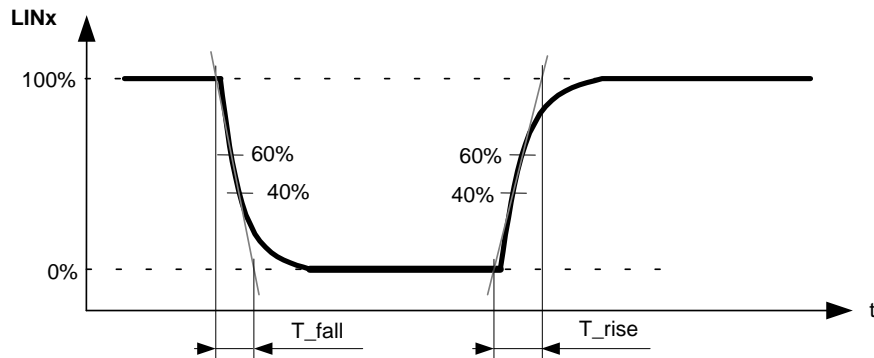


Figure 25. Definition of LINx Edge Parameters

NCV7471B, NCV7471C

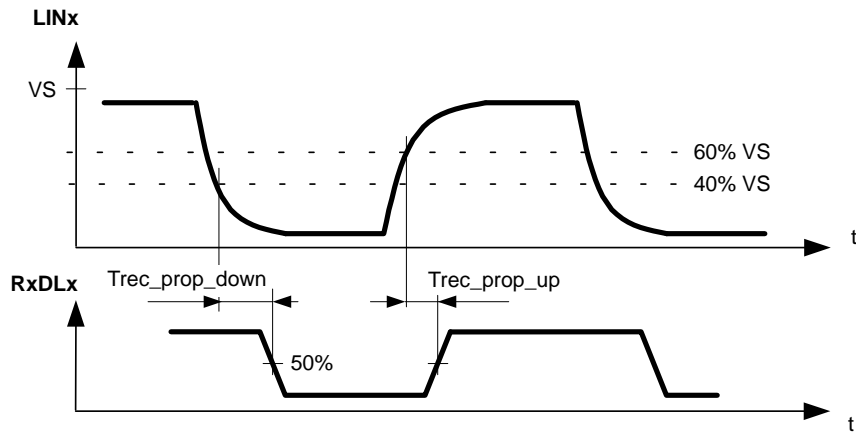


Figure 26. Definition of LINx Receiver Timing Parameters

Digital Control Timing and SPI Timing

Table 34. DIGITAL CONTROL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|--------------------------|-------|------|--------|------|
| t_WD_TO t_WD_WIN | Duration of the total watchdog period | WD_PER_0 selected in SPI | 7.2 | 8 | 8.8 | ms |
| | | WD_PER_1 selected in SPI | 14.4 | 16 | 17.6 | ms |
| | | WD_PER_2 selected in SPI | 28.8 | 32 | 35.2 | ms |
| | | WD_PER_3 selected in SPI | 57.6 | 64 | 70.4 | ms |
| | | WD_PER_4 selected in SPI | 115.2 | 128 | 140.8 | ms |
| | | WD_PER_5 selected in SPI | 230.4 | 256 | 281.6 | ms |
| | | WD_PER_6 selected in SPI | 460.8 | 512 | 563.2 | ms |
| | | WD_PER_7 selected in SPI | 921.6 | 1024 | 1126.4 | ms |
| f_FSO2 | FSO2 toggling frequency | FSO_internal = 1 | 1.125 | 1.25 | 1.375 | Hz |
| dc_FSO2 | FSO2 duty cycle | | 45 | 50 | 55 | % |
| f_FSO3 | FSO3 toggling frequency | | 90 | 100 | 110 | Hz |
| dc_FSO3 | FSO3 duty cycle | | 18 | 20 | 22 | % |
| t_INTN_active | Active (Low) pulse on INTN pin | | 0.9 | 1 | 1.1 | ms |
| t_INTN_inactive | Minimum time between two consecutive interrupt requests | | 4.5 | 5 | 5.5 | ms |
| t_RSTN_filt | RSTN input signal filter time | | 1 | | 10 | μs |
| t_RSTN_Clamped_High | Timeout for "RSTN clamped High" detection | | 0.9 | 1 | 1.1 | ms |
| t_RSTN_Clamped_Low | Timeout for "RSTN clamped Low" detection | | 225 | 250 | 275 | ms |

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Table 35. SPI INTERFACE TIMING CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|------------|-----|-----|-----|------|
| tCSN_SCK | First SPI clock edge after CSN active | | 100 | | | ns |
| tSCK_CSN | Last SPI clock edge to CSN inactive | | 100 | | | ns |
| tCSN_SDO | SDO output stable after CSN active | | | | 100 | ns |
| tCSN_High | Inter-frame space (CSN inactive) | | 10 | | | μs |
| tSCK_High | Duration of SPI clock High level | | 100 | | | ns |
| tSCK_Low | Duration of SPI clock Low level | | 100 | | | ns |
| tSCK_per | SPI clock period | | 250 | | | ns |
| tSDI_set | Setup time of SDI input towards SPI clock | | 50 | | | ns |
| tSDI_hold | Hold time of SDI input towards SPI clock | | 50 | | | ns |
| tSCK_SDO | delay of SDO output stable after an SPI clock edge | | | | 50 | ns |

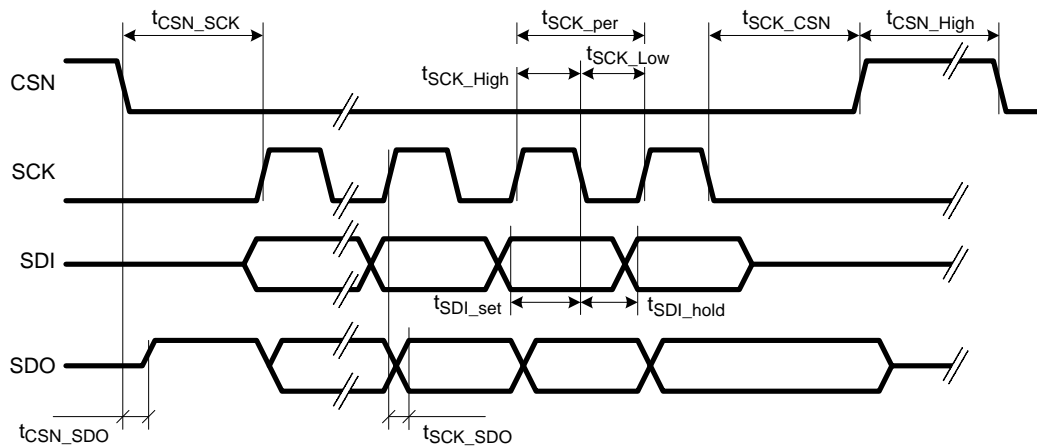


Figure 27. Definition of SPI Timing Parameters

Thermal Protection

Table 36. THERMAL PROTECTION CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|--|------------|-----|-----|-----|------|
| Tj_WAR | Junction temperature for thermal warning | | 130 | 140 | 150 | °C |
| Tj_SD | Junction temperature for thermal shut-down | | 150 | 160 | 170 | °C |

Digital IO Pins

Table 37. ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIGITAL INPUTS/OUTPUTS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--------------------------------------|--|-----|-----|------|------|
| VinL_pinx | Low-level input threshold | pinx = SDI, SCK, CSN, TxDC, TxDL1/2, RSTN | 0 | | 0.8 | V |
| VinH_pinx | High-level input threshold | | 2 | | VOUT | V |
| Rpullup_pinx | Integrated pull-up resistor to VOUT | pinx = CSN, TxDC, TxDL1/2, INTN, RSTN, UVN_VOUT | 55 | 100 | 185 | kΩ |
| Rpulldown_pinx | Integrated pull-down resistor to GND | pinx = SDI, SCK | 55 | 100 | 185 | kΩ |
| IoutL_pinx | Low-level output driving current | pinx is logical Low; forced Vpinx = 0.4 V; pinx = SDO, RxDC, RxDL1/2, RSTN, INTN, UVN_VOUT | 2 | 6 | 12 | mA |

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Table 37. ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIGITAL INPUTS/OUTPUTS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|--|-----|-----|-----|------|
| I _{OUTH_pinx} | High-level output driving current | pinx is logical High; forced V _{pinx} = V _{OUT} -0.4 V; pinx = SDO, RxDC, RxDL1/2 | -12 | -6 | -2 | mA |
| I _{leak_HZ_pinx} | Leakage in the tristate | pinx in HZ state; forced 0 V < V _{pinx} < V _{OUT} ; pinx = SDO | -10 | | 10 | μA |
| I _{leak_OD} | Leakage of an open-drain output | open-drain pinx in High state; forced V _{pinx} = V _{OUT} ; pinx = INTN, RSTN, UVN_VOUT | -10 | | 10 | μA |
| V _{MID_DigOut_Low} | V _{MID} value guaranteeing Low level on RSTN and UVN_VOUT pins | Shut-down mode; RSTN and UVN_VOUT connected to fixed 5 V through a 10 kΩ resistor. | | | 1.9 | V |
| V _{OUT_DigOut_Low} | V _{OUT} value guaranteeing Low level on RSTN and UVN_VOUT pins | If V _{MID} > V _{MID_DigOut_Low} or V _{OUT} > V _{OUT_DigOut_Low} , then RSTN and UVN_VOUT stay below 400 mV Not tested in production; guaranteed by design | | | 2.7 | V |

CFG and SWDM Pins

Table 38. ELECTRICAL CHARACTERISTICS OF CFG AND SWDM INPUTS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------|---|-----|-----|----------------|------|
| V _{inL_HV_pinx} | Low-level input threshold | pinx = CFG, SWDM | 0 | | 0.8 | V |
| V _{inH_HV_pinx} | High-level input threshold | | 2 | | V _S | V |
| R _{pulldown_HV_pinx} | Internal pull-down to GND | pinx = CFG, SWDM; V _{CFG} < 0.8 V | 55 | 100 | 185 | kΩ |
| R _{pullup_HV_pinx} | Internal pull-up to 3 V (typ.) | pinx = CFG; V _{CFG} > 2 V | 55 | 100 | 185 | kΩ |

FSO Pins

Table 39. FSOx PIN ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|-------------------------------------|--|-----|-----|-----|------|
| I _{FSOx_inactive} | FSOx current in inactive state | FSOx inactive (no failure), or HZ-part of the FSO2/3 pattern. 0 V < V(FSOx) < 28 V | -2 | | 2 | μA |
| V _{FSOx_active} | Voltage drop at FSOx when active | FSO1 active or Low-part of the FSO2/3 pattern; I(FSOx) = 5 mA | | | 0.4 | V |
| | | FSO1 active or Low-part of the FSO2/3 pattern; I(FSOx) = 10 mA | | | 0.8 | V |

WU Pin

Table 40. WU PIN ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-----------------------------|-------------|------|-----|------|------|
| V _{th_WU} | WU pin threshold | | 2 | | 4 | V |
| V _{hys_WU} | WU pin threshold hysteresis | | 0.03 | | 0.25 | V |
| t _{WU_filt} | WU wakeup filter time | | 10 | | 50 | μs |
| I _{pu_WU} | Pull-up current on WU pin | V(WU) = 4 V | -11 | | -3 | μA |
| I _{pd_WU} | Pull-down current on WU pin | V(WU) = 2 V | 3 | | 11 | μA |

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Table 41. ISO11898–2: 2016 PARAMETER CROSS REFERENCE TABLE

| ISO 11898–2:2016 Specification | | NCV7471B/C Datasheet |
|---|------------------------------|--|
| Parameter | Notation | Symbol |
| Dominant output characteristics | | |
| Single ended voltage on CAN_H | V_{CAN_H} | $V_{o(dom)}(CANH)$ |
| Single ended voltage on CAN_L | V_{CAN_L} | $V_{o(dom)}(CANL)$ |
| Differential voltage on normal bus load | V_{Diff} | $V_{o(dif)}(bus_dom)$ |
| Differential voltage on effective resistance during arbitration | V_{Diff} | $V_{o(dif)}(bus_dom_arb)$ |
| Optional: Differential voltage on extended bus load range | V_{Diff} | NA |
| Driver symmetry | | |
| Driver symmetry | V_{SYM} | $V_{o(sym)}(bus_dom)$ |
| Driver output current | | |
| Absolute current on CAN_H | I_{CAN_H} | $I_{o(SC)}(CANH)$ |
| Absolute current on CAN_L | I_{CAN_L} | $I_{o(SC)}(CANL)$ |
| Receiver output characteristics, bus biasing active | | |
| Single ended output voltage on CAN_H | V_{CAN_H} | $V_{o(reces)}(CANH)$ |
| Single ended output voltage on CAN_L | V_{CAN_L} | $V_{o(reces)}(CANL)$ |
| Differential output voltage | V_{Diff} | $V_{o(dif)}(bus_rec)$ |
| Receiver output characteristics, bus biasing inactive | | |
| Single ended output voltage on CAN_H | V_{CAN_H} | $V_{o(reces)}(CANH)$ |
| Single ended output voltage on CAN_L | V_{CAN_L} | $V_{o(reces)}(CANL)$ |
| Differential output voltage | V_{Diff} | $V_{o(dif)}(bus_rec)$ |
| Optional transmit dominant timeout | | |
| Transmit dominant timeout, long | t_{dom} | $T_TxDC_timeout$ |
| Transmit dominant timeout, short | t_{dom} | $T_TxDC_timeout$ |
| Static receiver input characteristics, bus biasing active | | |
| Recessive state differential input voltage range | V_{Diff} | $V_{i(rec)}(bus_rec)$ |
| Dominant state differential input voltage range | V_{Diff} | $V_{i(rec)}(bus_dom)$ |
| Static receiver input characteristics, bus biasing inactive | | |
| Recessive state differential input voltage range | V_{Diff} | $V_{i(rec)}(bus_rec)$ |
| Dominant state differential input voltage range | V_{Diff} | $V_{i(rec)}(bus_dom)$ |
| Receiver input resistance | | |
| Differential internal resistance | R_{Diff} | $R_{i(dif)}$ |
| Single ended internal resistance | R_{CAN_H} R_{CAN_L} | $R_{i(cm)}(CANH)$ $R_{i(cm)}(CANL)$ |
| Receiver input resistance matching | | |
| Matching a of internal resistance | m_R | $R_{i(cm)}(m)$ |
| Implementation loop delay requirement | | |
| Loop delay | t_{Loop} | $t_{dPD}(TxDC-RxDC)_{dr}$ $t_{dPD}(TxDC-RxDC)_{rd}$ |
| Optional implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s | | |
| Transmitted recessive bit width @ 2 Mbit/s | $t_{Bit}(Bus)$ | $t_{BIT}(V_{i(dif)}500)$ |
| Received recessive bit width @ 2 Mbit/s | $t_{Bit}(RXD)$ | $t_{BIT}(RxDC500)$ |
| Receiver timing symmetry @ 2 Mbit/s | Δt_{Rec} | Δt_{REC500} |

NCV7471B, NCV7471C

Table 41. ISO11898–2: 2016 PARAMETER CROSS REFERENCE TABLE

| Parameter | Notation | Symbol |
|---|--|--|
| Optional implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s | | |
| Transmitted recessive bit width @ 5 Mbit/s | $t_{\text{Bit(Bus)}}$ | NA |
| Transmitted recessive bit width @ 5 Mbit / s | $t_{\text{Bit(RXD)}}$ | NA |
| Received recessive bit width @ 5 Mbit / s | Δt_{Rec} | NA |
| Maximum ratings of $V_{\text{CAN_H}}$, $V_{\text{CAN_L}}$ and V_{Diff} | | |
| Maximum rating V_{Diff} | V_{Diff} | $V_{\text{max_CANH-CANL}}$ |
| General maximum rating $V_{\text{CAN_H}}$ and $V_{\text{CAN_L}}$ | $V_{\text{CAN_H}}$ $V_{\text{CAN_L}}$ | $V_{\text{max_CANH}}$ $V_{\text{max_CANL}}$ |
| Optional: Extended maximum rating $V_{\text{CAN_H}}$ and $V_{\text{CAN_L}}$ | $V_{\text{CAN_H}}$ $V_{\text{CAN_L}}$ | NA |
| Maximum leakage currents on CAN_H and CAN_L, unpowered | | |
| Leakage current on CAN_H, CAN_L | $I_{\text{CAN_H}}$, $I_{\text{CAN_L}}$ | ILI_CANH ILI_CANL |
| Bus biasing control timings | | |
| CAN activity filter time, long | t_{Filter} | $t_{\text{CAN_wake_dom}}$, $t_{\text{CAN_wake_rec}}$ |
| CAN activity filter time, short | t_{Filter} | NA |
| Optional: Wake-up timeout, short | t_{Wake} | NA |
| Optional: Wake-up timeout, long | t_{Wake} | $T_{\text{CAN_wake_timeout}}$ |
| Timeout for bus inactivity (Required for selective wake-up implementation only) | t_{Silence} | |
| Bus Bias reaction time (Required for selective wake-up implementation only) | t_{Bias} | |

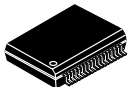
Table 42. DEVICE ORDERING INFORMATION

| Part Number | Description | Package Type | Shipping† |
|----------------|---|--------------------|--------------------|
| NCV7471BDQ5R2G | System Basis Chip with Dual LIN, HS-CAN/CANFD, 11 V Boost and 5 V / 500 mA Buck DC/DC; FSOx outputs active during VOUT undervoltage | SSOP36-EP GREEN | 1500 / Tape & Reel |
| NCV7471CDQ5R2G | System Basis Chip with Dual LIN, HS-CAN/CANFD, 6.5 V Boost and 5 V / 500 mA Buck DCDC; FSOx outputs active during VOUT undervoltage | SSOP36-EP GREEN | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

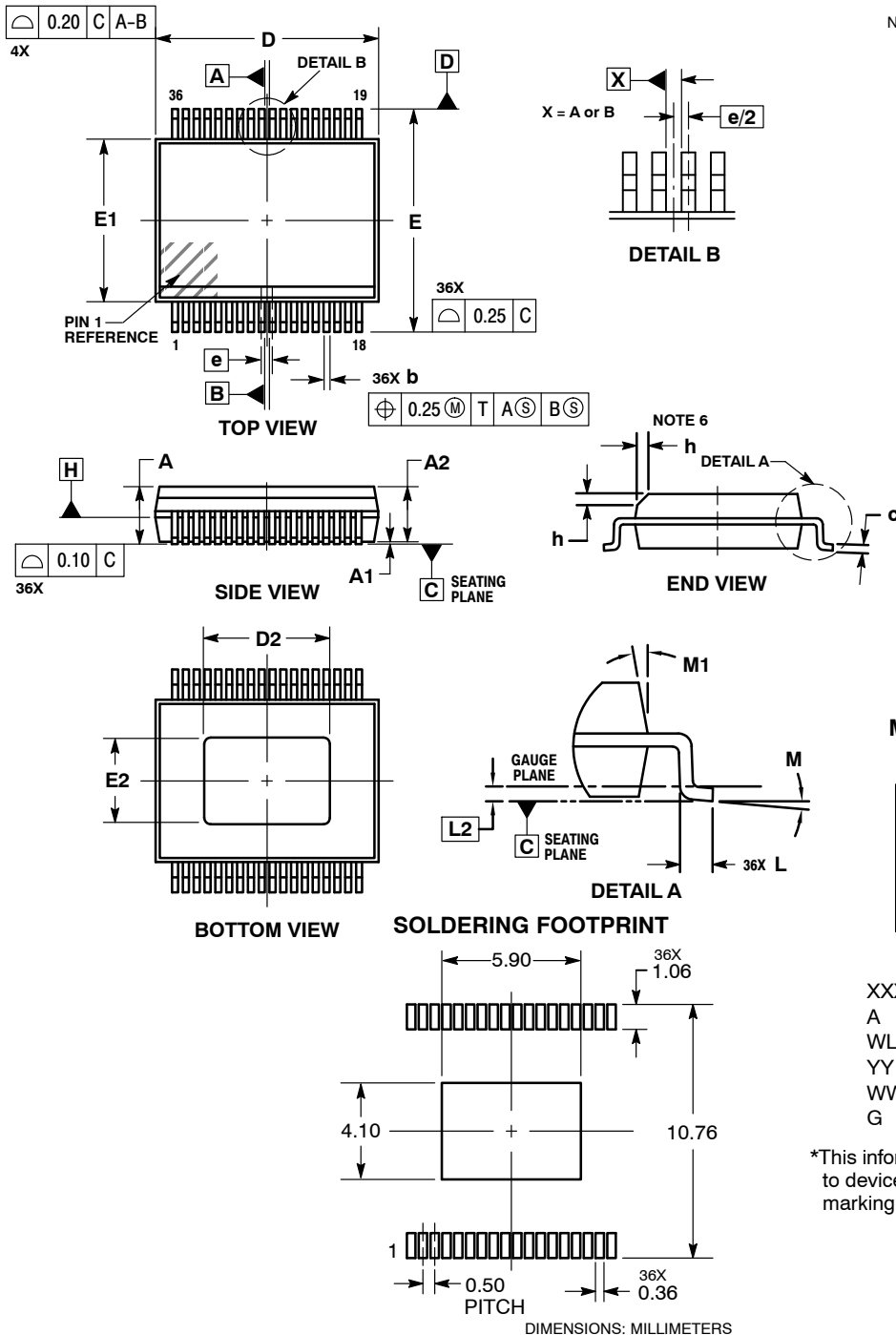
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SCALE 1:1

SSOP36 EP
CASE 940AB
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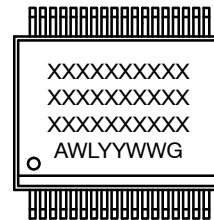


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOCATED WITHIN THE INDICATED AREA.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 2.65 |
| A1 | --- | 0.10 |
| A2 | 2.15 | 2.60 |
| b | 0.18 | 0.30 |
| c | 0.23 | 0.32 |
| D | 10.30 BSC | |
| D2 | 5.70 | 5.90 |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| E2 | 3.90 | 4.10 |
| e | 0.50 BSC | |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |
| M1 | 5° | 15° |

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
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