

Evaluating the **ADF5709** 9.85 GHz to 20.5 GHz, Wideband, MMIC VCO

FEATURES

Self contained evaluation board containing the **ADF5709**
wideband, MMIC VCO

Externally powered by a single 5 V supply

EVALUATION KIT CONTENTS

EV-ADF5709 evaluation board

EQUIPMENT NEEDED

5 V power supply

Low noise, variable, 0 V to 23 V power supply

Signal source analyzer

Spectrum analyzer

ONLINE RESOURCES

ADF5709 data sheet

GENERAL DESCRIPTION

The EV-ADF5709 evaluates the performance of the ADF5709 wideband, voltage controlled oscillator (VCO). Figure 1 shows a photograph of the EV-ADF5709. The EV-ADF5709 contains the ADF5709, external supply headers, supply decoupling capacitors, a VTUNE Subminiature Version A (SMA) connector, and a 2.92 mm, RF output K connector. No software interface is required to control the ADF5709 while the device is operating as a standalone VCO in open-loop mode.

For full details on the ADF5709, see the ADF5709 data sheet, which must be consulted in conjunction with this user guide when using the EV-ADF5709.

EVALUATION BOARD PHOTOGRAPH

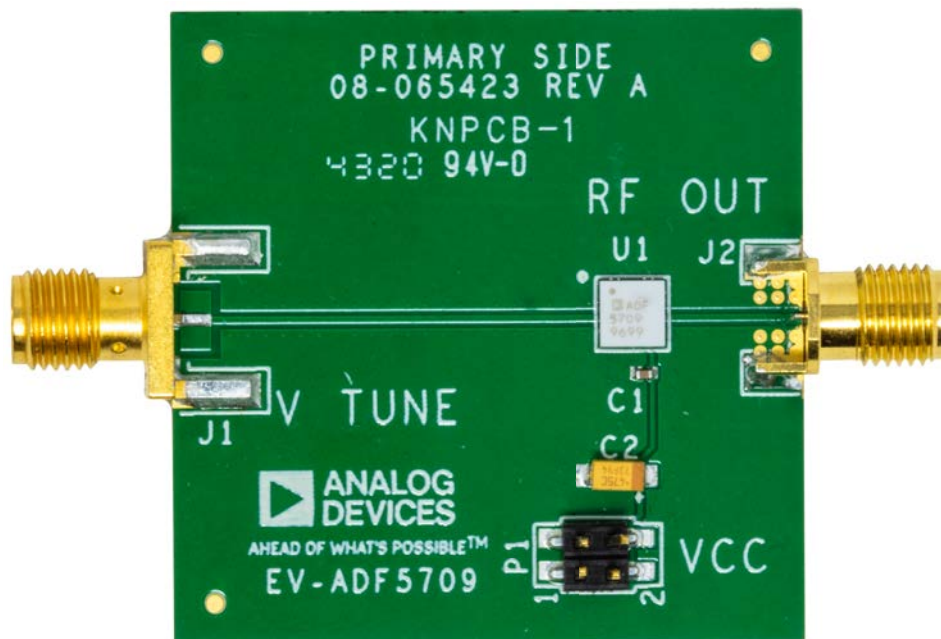


Figure 1.

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REVISION HISTORY

12/2020—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

To configure the EV-ADF5709 for the first time, perform the following steps:

1. Verify that the analog power supply used to power the EV-ADF5709 can output 5 V and 90 mA of compliance current.
2. Disable the power supply output for now or damage may occur.
3. Connect positive and negative hook clip leads from the 5 V power supply unit to the VCC and ground header pins, respectively.
4. Connect the low noise, variable power supply to the VTUNE SMA connector on the tuning port (J1) using a double shielded Bayonet Neill–Concelman (BNC) cable and a BNC to SMA adapter. Torque this connection to 8 in/lb using an SMA torque wrench.
5. Connect a 50 Ω RF cable capable of mating to the 2.92 mm K connector at J2 and torque this connection to 8 in/lb. Connect the other end of the cable to a spectrum analyzer.
6. Enable the 5 V power supply. Approximately 70 mA is drawn from the supply if the EV-ADF5709 is operating properly.
7. Enable the variable power supply and adjust the tuning voltage to a value within the -0.5 V to $+23$ V range of the VCO.
8. Verify that the output frequency observed on the spectrum analyzer is in the region of the expected frequency corresponding to the V_{TUNE} voltage applied by referring to the output frequency (f_{OUT}) vs. V_{TUNE} plot in the [ADF5709](#) data sheet. An example output frequency is shown in Figure 3 in the Evaluation and Test section.

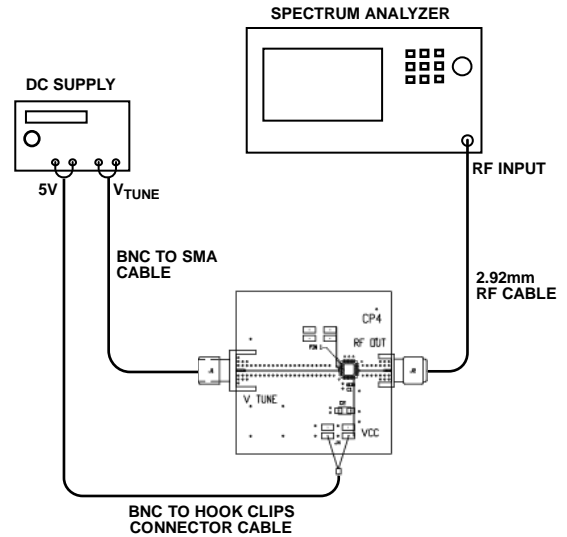


Figure 2. Board Setup

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EVALUATION BOARD HARDWARE

The EV-ADF5709 schematic, silkscreen, and bill of materials are available in the Evaluation Board Schematic and Artwork section and Ordering Information section. The Gerber fabrication files are available on the [ADF5709](#) product page.

POWER SUPPLIES

The EV-ADF5709 is powered by a 5 V dc (90 mA) power supply connected to the 4-pin header. The supply path from the header to the ADF5709 includes decoupling capacitors for supply noise mitigation. To improve the power supply performance, users can connect a power supply through external regulators, such as the [LT3042](#) or the [ADM7150](#). The evaluation boards for the LT3042 and the ADM7150 can be purchased on the Analog Devices, Inc., website.

VCO

The ADF5709 is a wideband, monotonic VCO that generates a frequency range of 9.85 GHz to 20.5 GHz and operates from a single 5 V supply. A tuning voltage of -0.5 V to $+23$ V is applied to the VTUNE port of the EV-ADF5709 to control the output frequency.

BUFFER AMPLIFIER

An internal cascode buffer amplifier stage is contained within the ADF5709 VCO that provides stable output power across the 9.85 GHz to 20.5 GHz frequency range. This buffer amplifier is powered internally by the 5 V power supply. An ac coupling capacitor is connected between the buffer output and the RFOUT pin.

RF OUTPUT

The EV-ADF5709 has a single RF output port (J2). J2 is a single-ended RF output that produces an RF output frequency ranging from 9.85 GHz to 20.5 GHz.

LOOP FILTER

The EV-ADF5709 does not incorporate a loop filter design. All loop filter components must be placed on a separate evaluation board containing the interfacing phase-locked loop (PLL) chip. For optimal loop stability, place the first pole of the loop filter as close as possible to the charge pump output of the interfacing PLL chip. Place the last pole as close as possible to the VTUNE SMA input connection of the EV-ADF5709, which the PLL chip connects to, to filter high frequency noise. The placement of any additional poles that exist between the first and last pole of the loop filter are not as critical.

Because the tuning voltage of the ADF5709 ranges from -0.5 V to $+23$ V, an active loop filter design is required, unless the interfacing PLL chip can output this voltage range. A PLL evaluation board typically includes placements for the operational amplifier, bias circuitry, and any additional components.

DEFAULT CONFIGURATION

All components necessary for local oscillator generation are inserted on the EV-ADF5709.

EVALUATION AND TEST

To configure the EV-ADF5709 for the first time, follow Step 1 to Step 8 in the Evaluation Board Setup Procedure section. To evaluate and test the performance of the EV-ADF5709, perform the following steps, which show an example V_{TUNE} voltage and the resulting RF output frequency:

1. Enable the variable power supply and adjust the tuning voltage to 6 V. A signal at approximately 13.5 GHz with between -2 dBm and 0 dBm of output power appears on a spectrum analyzer or signal source analyzer. This result is shown in Figure 3.
2. Verify that the phase noise at this output frequency of approximately 13.5 GHz matches the single sideband phase noise specification in the ADF5709 data sheet by using the signal source analyzer to measure the phase noise. Refer to Figure 4.
3. Repeat Step 1 and Step 2 for different V_{TUNE} voltages between -0.5 V and $+23$ V to compare with the f_{OUT} vs. V_{TUNE} plot in the ADF5709 data sheet.

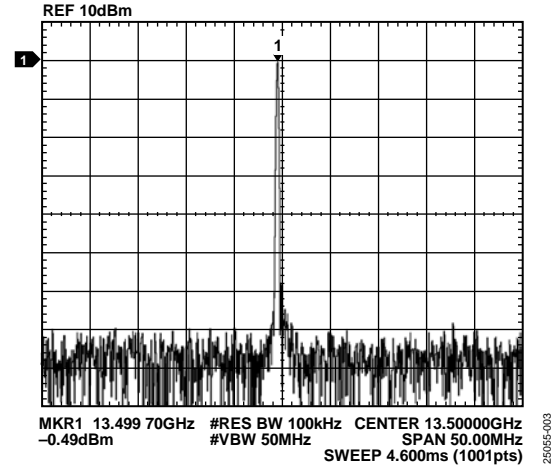


Figure 3. RF Output Frequency at $V_{TUNE} = 6$ V

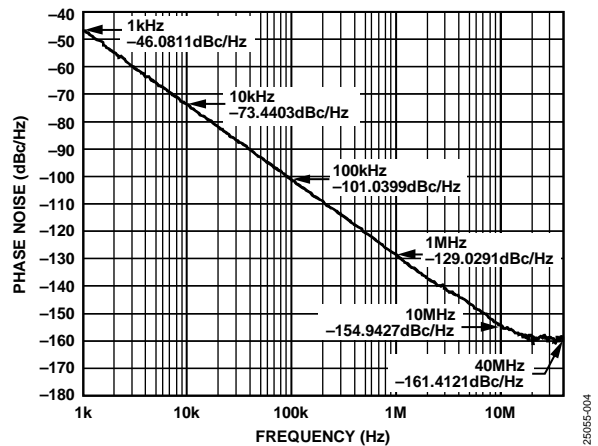


Figure 4. EV-ADF5709 Phase Noise at J2, VCO Band 1, $V_{TUNE} = 8.45$ V, 13.5 GHz

EVALUATION BOARD SCHEMATIC AND ARTWORK

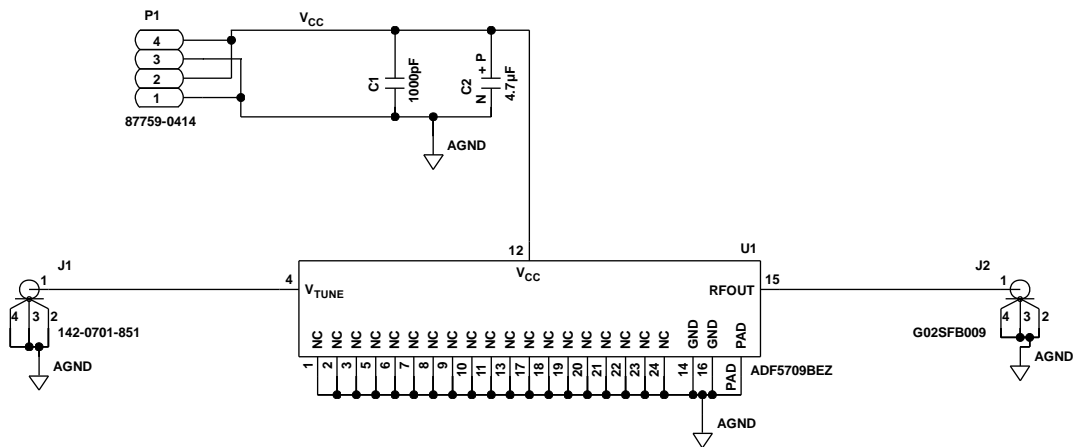


Figure 5. EV-ADF5709 Schematic

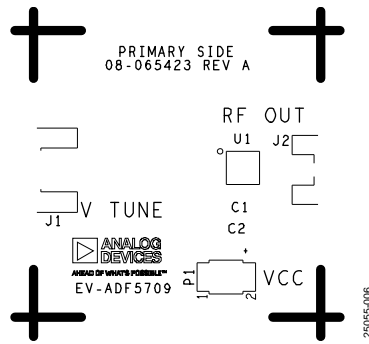


Figure 6. EV-ADF5709 Silkscreen

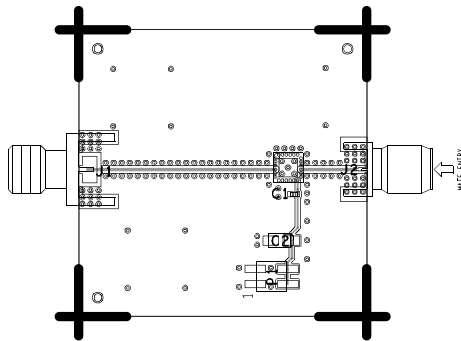


Figure 7. EV-ADF5709 Layer 1

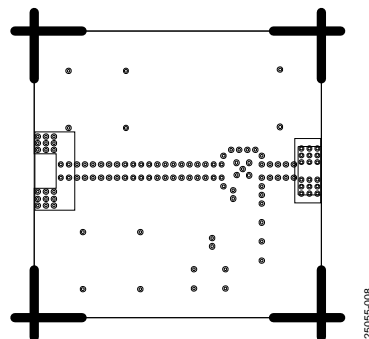


Figure 8. EV-ADF5709 Layer 2 (Ground)

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Reference Designator	Description	Value	Manufacturer	Part Number
C1	Ceramic capacitor, X7R, automotive grade	1000 pF	Samsung	CLO5B102JB5NNNC
C2	Tantalum capacitor, general-purpose	4.7 μ F	Murata	TAJA475M016RNJ
J1	SMA connector, end launch jack, 0 GHz to 18 GHz	Not Applicable	Cinch	142-0701-851
J2	SMA connector, end launch jack, 0 GHz to 40 GHz	Not Applicable	SRI	21-146-1000-01
P1	Dual row header connection	Not Applicable	Molex	87759-0414
U1	ADF5709 9.85 GHz to 20.5 GHz, wideband, MMIC VCO	Not Applicable	Analog Devices	ADF5709BEZ



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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