NCP6915

6 Channels PMIC with One DCDC Converter and 5 LDOs

The NCP6915 integrated circuit is part of the ON Semiconductor mini power management IC family. It is optimized to supply battery powered portable application sub−systems such as camera function, microprocessors ... etc. This device integrates one high efficiency 600 mA Step−down DCDC converter with DVS (Dynamic Voltage Scaling) and 5 low dropout (LDO) voltage regulators in WLCSP16 package.

Features

- One DCDC Converter:
  - Peak Efficiency 96%
  - Programmable Output Voltage from 0.8 V to 2.3 V by 50 mV Steps
  - 600 mA Output Current Capability
- Five Low Noise − Low Dropout Regulators
  - Programmable Output Voltage from 1.7 V to 3.3 V for LDOs 1, 2, 3
  - Programmable Output Voltage from 1.2 V to 2.85 V for LDO 4 & 5
  - 200 mA Output Current Capability: LDO's 1, 2, 3 & 4
  - 300 mA Output Current Capability: LDO 5
  - 45 μVrms Low Output Noise
- Control
  - 400 kHz / 3.4 MHz I^2C Control Interface
  - Hardware Enable Pin
  - Customizable Power up Sequencer
- Extended Input Voltage Range 2.5 V to 5.5 V
  - Support of Newest Battery Technologies
- Optimized Power Efficiency
  - 82 μA Very Low Quiescent Current at no Load
  - Dynamic Voltage Scaling on DCDC Converter
  - Regulators can be Supplied from DCDC Converter Output
- Small footprint
  - Package WLCSP16 1.56 x 1.56 mm^2
  - DCDC Converter runs at 3.0 MHz using a 1 μH Inductor and 10 μF Capacitor or 2.2 μH Inductor and 4.7 μF Capacitor
- This is a Pb−Free Device

Typical Applications

- Cellular Phones
- Digital Cameras
- Personal Digital Assistant and Portable Media Player
- GPS

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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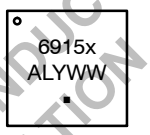
WLCSP16
CASE 567GF

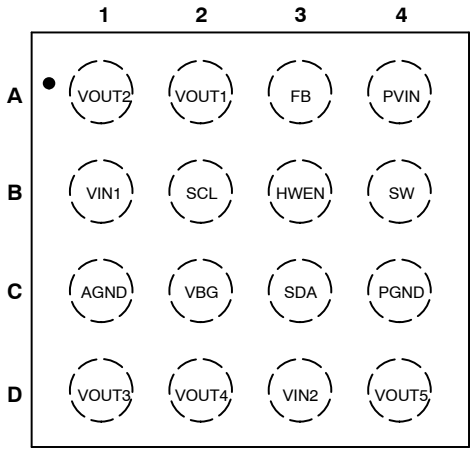
MARKING DIAGRAM*



6915x = Specific Device Code (x = A or B)
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

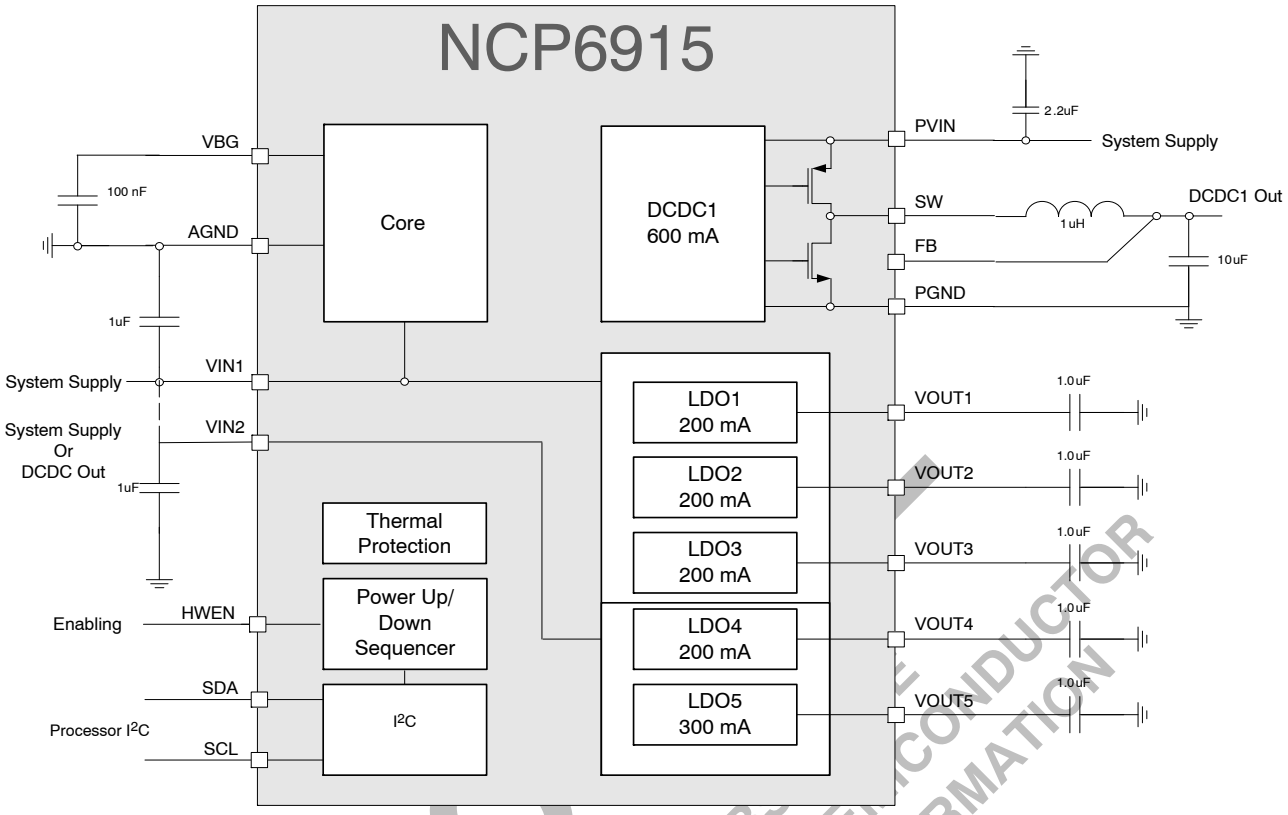


Figure 1. Functional Block Diagram

Table 1. PIN OUT DESCRIPTION

Pin	Name	Type	Description
POWER			
B1	VIN1	Power Input	Analog Supply. This pin is the device analog, digital and LDO 1, 2 & 3 supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close a possible to this pin.
C2	VBG	Analog Input	Reference Voltage. A 0.1 μF ceramic capacitor must bypass this pin to the ground
C1	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
B3	HWEN	Digital Input	Hardware Enable. Active high will enable the part; there is internal pull down resistor on this pin.
B2	SCL	Digital Input	I^2C interface **Clock**
C3	SDA	Digital Input/Output	I^2C interface **Data**
DCDC CONVERTER			
A4	PVIN	Power Input	DCDC Power Supply. This pin must be decoupled to ground by a 2.2 μF ceramic capacitor. This capacitor should be placed as close a possible to this pin.
B4	SW	Power Output	DCDC Switch Power pin connects power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
A3	FB	Analog Input	DCDC Feedback Voltage. Must be connected to the output capacitor. This is the input to the error amplifier.
C4	PGND	Power Ground	DCDC Power Ground. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane is recommended.
LDO REGULATORS			
B1	VIN1	Power Input	LDO 1,2 & 3 Power and Core supply (see Power table)
D3	VIN2	Power Input	LDO 4&5 Power Supply This pin requires a 1 μF decoupling capacitor.
A2	VOUT1	Power Output	LDO 1 Output Power. This pin requires a 1 μF decoupling capacitor.
A1	VOUT2	Power Output	LDO 2 Output Power. This pin requires a 1 μF decoupling capacitor.
D1	VOUT3	Power Output	LDO 3 Output Power. This pin requires a 1 μF decoupling capacitor.
D2	VOUT4	Power Output	LDO 4 Output Power. This pin requires a 1 μF decoupling capacitor.
D4	VOUT5	Power Output	LDO 5 Output Power. This pin requires a 1 μF decoupling capacitor.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and power pins: AVIN, PVIN, SW, VIN1, VIN2, VOUT1, VOUT2, VOUT3, VOUT4, VOUT5, FB, VBG Pins	V_A	−0.3 to +6.0	V
Digital pins: SCL, SDA, HWEN Pin: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A +0.3 ≤ 6.0 10	 V mA
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 1)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN1} PV_{IN}	Core Power Supply, DCDC power supply and LDOs 1, 2 & 3		2.5		5.5	V
V_{IN2}	LDOs 4 & 5 Input Voltage range		1.7		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 3)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Case		–	80	–	°C/W
P_D	Power Dissipation Rating (Note 5)	T_A = 25°C	–	1250	–	mW
		T_A = 85°C	–	500	–	mW
L	Inductor for DCDC converter (Note 2)		1		2.2	μH
Co	Output Capacitor for DCDC Converter (Note 2)			10		μF
	Output Capacitors for LDO (Note 2)		0.65	1		μF
C_{BG}	Output Capacitors for V_{BG}			100		nF
Cpvin	Input Capacitor for DCDC Converter (Note 2)			2.2		μF
Cvin1	Input Capacitor for Vin1 (Note 2)			1		μF
Cvin2	Input Capacitor for Vin2 (Note 2)			1		μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Refer to the Application Information section of this data sheet for more details.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. The $R_{\theta CA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2” x 2” NCPXXXEVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
5. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC} \text{ with } \left(R_{\theta JA} = R_{\theta JC} + R_{\theta CA}\right)$$

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2 V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 7).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS VIN1, VIN2, PVIN						
I_Q	Operating quiescent current	DCDC on – no load – no switching LDOs off T_A = up to +85°C	–	32	–	μA
		DCDC on – no load – no switching LDOs on – no load T_A = up to +85°C	–	82	–	
		DCDC Off LDOs on – no load T_A = up to +85°C	–	65	–	
I_{SLEEP}	Product sleep mode current	HWEN on All DCDC and LDOs off V_{IN} = 2.5 V to 5.5 V T_A = up to +85°C	–	7	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
7. Refer to the Application Information section of this data sheet for more details.
8. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2 V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 7).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS VIN1, VIN2, PVIN						
I_{OFF}	Product off current	HWEN off I^2C interface disabled V_{IN} = 2.5 V to 5.5 V T_A = up to +85°C	–	0.3	–	μA
DCDC CONVERTER						
PV_{IN}	Input Voltage Range		2.5	–	5.5	V
I_{OUTMAX}	Maximum Output Current	(Note 8)	0.6	–	–	A
Δ_{VOUT}	Output Voltage DC Error	Io = 300 mA, PWM mode	−1.5	0	1.5	%
DC_{OUT}	DCDC Output voltage	Programmable 50 mV steps (Note 8)	0.8		2.3	V
F_{SW}	Switching Frequency		2.7	3	3.3	MHz
I_{PK}	Peak Inductor Current	Open loop 2.5 V ≤ PV_{IN} ≤ 5.5 V	1.0	1.3	1.6	A
	Load Regulation	I_{OUT} from 300 mA to I_{OUTMAX}	–	−0.5	–	%/A
	Line Regulation	I_{OUT} = 300 mA 2.5 V ≤ V_{IN} ≤ 5.5 V	–	0	–	%/V
D	Maximum Duty Cycle		–	100	–	%
t_{START}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage, Vout = 1.2 V.	–	128		μs
$R_{DISDCDC}$	DCDC Active Output Discharge		–	8	–	Ω
LDO1, LDO2, LDO3						
V_{IN1}	LDO1, LDO2, LDO3 input voltage Range		2.5	–	5.5	V
$I_{OUTMAX1,2,3}$	Maximum Output Current		200	–	–	mA
$I_{SC1,2,3}$	Short Circuit Protection		–	500		mA
	Foldback Current			130		mA
$V_{out1,2,3}$	Output voltage	Programmable, see table. (Note 8)	1.7		3.3	V
t_{START1}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage.	–	128		μs
$\Delta V_{OUT1,2,3}$	Output Voltage Accuracy DC	$I_{OUT1,2,3}$ = 150 mA	−2	V_{NOM}	+2	%
	Load Regulation	$I_{OUT1,2,3}$ = 0 mA to 200 mA	–	0.4	–	%
	Line Regulation	V_{IN1} = (Vout + Drop) to 5.5 V $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 200 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	$I_{OUT1,2,3}$ = 200 mA, V_{OUT} = 3.3 V − 2%		160		mV
		$I_{OUT1,23}$ = 200 mA, V_{OUT} = 2.8 V − 2%	–	185		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
7. Refer to the Application Information section of this data sheet for more details.
8. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2 V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 7).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO1, LDO2, LDO3						
PSRR	Ripple Rejection	F = 1 kHz, 100 mV peak to peak $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 5 mA	–	–70	–	dB
		F = 10 kHz, 100 mV peak to peak $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 5 mA	–	–60	–	
Noise		10 Hz → 100 kHz, 5 mA $V_{OUT1,2,3}$ = 2.8 V	–	45	–	μV
$R_{DISLDO1,2,3}$	LDO Active Output Discharge		–	25	–	Ω
LDO4 and LDO5						
V_{IN2}	LDO4 and LDO5 Input Voltage		1.7	–	5.5	V
$I_{OUTMAX4}$	Maximum Output Current		200	–	–	mA
$I_{OUTMAX5}$	Maximum Output Current		300	–	–	mA
I_{SC4}	Short Circuit Protection		–	500	–	mA
I_{SC5}	Short Circuit Protection			600	–	mA
I_{SC4}	Foldback Protection			130	–	mA
I_{SC5}	Foldback Protection			190	–	mA
$V_{out4,5}$	LDO 4&5 Output voltage	Programmable, see table. (Note 8)	1.2	–	2.85	V
t_{START2}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage.	–	128		μs
ΔV_{OUT4}	Output Voltage Accuracy	I_{OUT4} = 200 mA	–2	V_{NOM}	+2	%
ΔV_{OUT5}	Output Voltage Accuracy	I_{OUT5} = 300 mA	–2	V_{NOM}	+2	%
	Load Regulation	I_{OUT4} = 0 mA to 200 mA I_{OUT5} = 0 mA to 300 mA	–	0.4	–	%
	Line Regulation	V_{IN2} = (Vout + Drop) to 5.5 V V_{OUT4} = 2.8 V, V_{OUT5} = 1.8 V I_{OUT4} = 200 mA, I_{OUT5} = 300 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	$I_{OUT4,5}$ = 200 mA $V_{OUT4,5}$ = 2.8 V − 2%	–	165		mV
		I_{OUT5} = 300 mA V_{OUT5} = 1.8 V − 2%		290		
PSRR	Ripple Rejection	F = 1 kHz, 100 mV peak to peak $I_{OUT4=}$ 5 mA, I_{OUT5} = 5 mA	–	–70	–	dB
		F = 10 kHz, 100 mV peak to peak $I_{OUT4,5}$ = 5 mA	–	–60	–	
Noise		10 Hz → 100 kHz, 5 mA $V_{OUT4,5}$ = 2.8 V	–	45	–	μV
$R_{DISLDO4,5}$	LDO 4&5 Active Output Discharge		–	25	–	Ω
HWEN						
V_{IH}	High level input Voltage Threshold		1.1	–	–	V
V_{IL}	Low level Voltage Threshold		–	–	0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HWEN						
I_{EN}				0.1	1	μA
I²C						
V_{I2C}	Voltage at SCL and SDA line		1.7	–	5.0	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 6)	–	–	0.5	V
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Note 6)	0.8 x V_{I2CC}	–	–	V
V_{I2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA (Note 8)	–	–	0.4	V
F_{SCL}	I²C clock frequency	(Note 8)	–	–	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	–	–	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	–	200	mV
T_{SD}	Thermal Shut Down Protection		–	150	–	°C
$T_{WARNING}$	Warning Rising Edge		–	135	–	°C
T_{SDR}	Thermal Shut Down Rearming		–	110	–	°C

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6. Devices that use non−standard supply voltages which do not conform to the intent I²C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
7. Refer to the Application Information section of this data sheet for more details.
8. Guaranteed by design and characterized.

DETAILED DESCRIPTION

The NCP6915 is optimized to supply the different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or mains powered applications.

The output voltage range, current capabilities and performance of the switched mode DCDC converter are well suited to supply the different peripherals in the system as well as to supply processor cores. To reduce overall power consumption of the application, Dynamic Voltage Scaling (DVS) is supported on the DCDC converter. For PWM operation, the converter runs on a local 3 MHz clock. A low power PFM mode is provided that ensures that even at low loads high efficiency can be obtained. All the switching components are integrated including the compensation networks and synchronous rectifier. Small sized 1 uH inductor and 10 uF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve on overall application standby current, the bias current of these regulators are made very low. The regulators have two separated input supply pin to be able to connect them independently to either the system supply voltage or to the output of the DCDC converter in the application. The regulators are bypassed with a small size 1.0 uF capacitor.

The IC is controlled through the I^2C interface that allows to program amongst others the output voltages of the different supply rails as well as to configure its behavior. In addition to this bus, a digital hardware enable control pin (HWEN) is provided.

Under Voltage Lockout

The core does not operate for voltages below the under voltage lockout (UVLO) threshold and all internal circuitry, both analog and digital, is held in reset.

NCP6915 functionality is guaranteed down to V_{UVLO} when the battery is falling. A hysteresis is implemented to avoid erratic on / off behavior of the IC. Due to its 200 mV hysteresis, when the battery is rising, re−start is guaranteed at 2.5 V.

Thermal Shutdown

Given the output power capabilities of the on chip step down converters and low drop out regulators the thermal capabilities of the device can be exceeded. A thermal protection circuit is therefore implemented to prevent the part from damage. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of NCP6915 are off.

When NCP6915 returns from thermal shutdown, it can re−start in two different configurations depending on REARM[7:6] bits ($09 register). If REARM[7:6] = 00 then NCP6915 re−starts with default register values, otherwise it re−starts with register values set prior to thermal shutdown.

In addition, a thermal warning is implemented which can inform the processor through an interrupt that NCP6915 is close to its thermal shutdown so that preventive action can be taken by software.

Active Output Discharge

By default, to prevent any disturbances on power−up sequence, output discharge is activated as soon as the input voltage is valid (upper than UVLO+ hyst).

After power up sequence and during ON state, output discharge can be independently enabled / disabled by appropriate settings in the DIS register (refer to the register definition section).

If a power down sequence, UVLO or thermal shutdown events occur, the output discharge paths are activated until the next PUS and ON state.

When the IC is turned off when VIN1 drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs turn to high impedance.

Enabling

The HWEN pin controls the device start up. If HWEN is raised, this starts the power up sequencer (PUS). If HWEN is made low, device enters in shutdown mode and all regulators will be turned off with inverted PUS of power up.

A built−in pull−down resistor disables the device if this pin is left unconnected.

When HWEN is high, the different power rails can be independently enabled / disabled by writing the appropriate bit in the ENABLE register.

Power Up Sequence and HWEN

When enabling part with HWEN pin, the part will be set with the default configuration factory programmed in the registers, if no I^2C programming has been done as described in the below table.

Table 5. DEFAULT POWER UP SEQUENCER

Device	Delay (in µs) from Tstart	Sequence	Default Assignment	Default Vprog	Default Mode and ON/OFF
NCP6915AFCCLT1G	128	To: 000	DCDC	1.2 V	Auto PFM/PWM OFF
	256	T1: 001	LDO1	2.8 V	OFF
	512	T2: 011	LDO2	2.8 V	OFF
	640	T3: 100	LDO3	1.8 V	OFF
	768	T4: 101	LDO4	2.8 V	OFF
	896	T5: 110	LDO5	1.8 V	OFF
NCP6915BFCCLT1G	128	To: 000	DCDC	2.1 V	Auto PFM/PWM ON
	384	T1: 001	LDO1	3.0 V	ON
	512	T2: 011	LDO2	2.8 V	OFF
	640	T3: 100	LDO3	2.8 V	OFF
	640	T4: 101	LDO4	1.8 V	ON
	256	T5: 110	LDO5	1.8 V	ON

NOTE: Additional power sequence are available. Please contact your ON Semiconductor representative for further information.

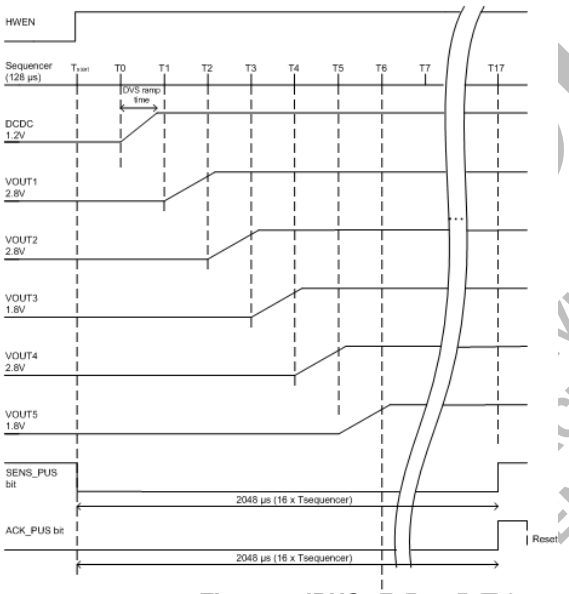


Figure 2. IPUS

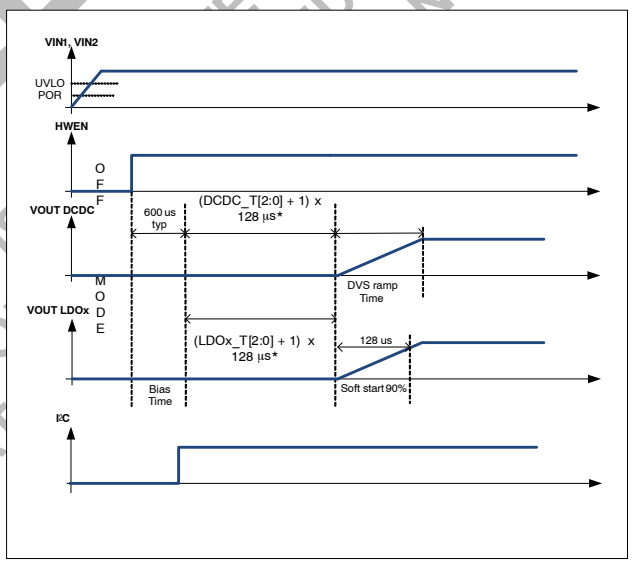


Figure 3. IPUS

The initial power up sequence (IPUS) is described in Figure 2.

Remark 1: T2 – T1 = 2x 128 µs in the default configuration. Can be reprogrammed at 128 µs by I^2C.

Remark 2: LDOs must be turned on sequentially to avoid inrush current on Vin source. So it's strongly recommended to turn them one by one, even if the default PUS sequence is changed by I^2C.

In order to power up the circuit, the input voltage VIN1 has to rise above the VUVLO threshold. This triggers the internal core circuitry power up including:

- Internal references
- Core circuitry "Wake Up Time"
- DCDC "Bias Time"

These delays are internals and cannot be bypassed.

As the default configuration factory is programmed with disable state for the DCDC and LDOs, an I^{2}C access must be done at the end of the bias time to enable the supplies.

In addition a user programmable delay will also take place between end of Core circuitry turn on (Bias time) and Start up time: The *PowerSupplies_T*[2..0] bits of TIME register will set this user programmable delay with a 128 µs resolution (note: please contact your ON Semiconductor representative for additional resolution options). The output discharge of the DCDC and LDOs are done during this time slot. NOTE: During the Bias time, the I^{2}C interface is not active during the first 50 µs. Any I^{2}C request to the IC during this time period will result in a NACK reply.

However, I^{2}C registers can be read and written while HWEN pin is still low (except blanking time of 50 µs typical). By programming the appropriate registers (see registers description section), the power up sequence default can be modified and set upon requirements (please contact your ON representative for additional PUS options)

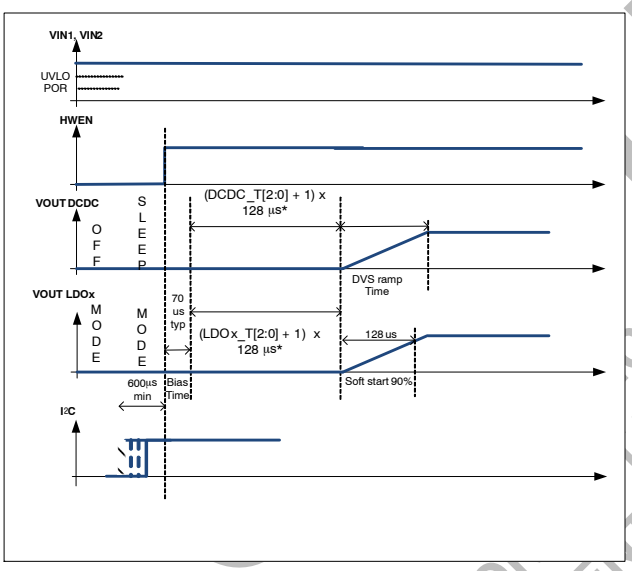


Figure 4. Sleep Mode PUS (SMPUS)

A third turn on sequence is also available by I^{2}C. Indeed each power supply can be turn off/on through I^{2}C register. In this case no biasing time is required except for DCDC bias time (32 µs typical).

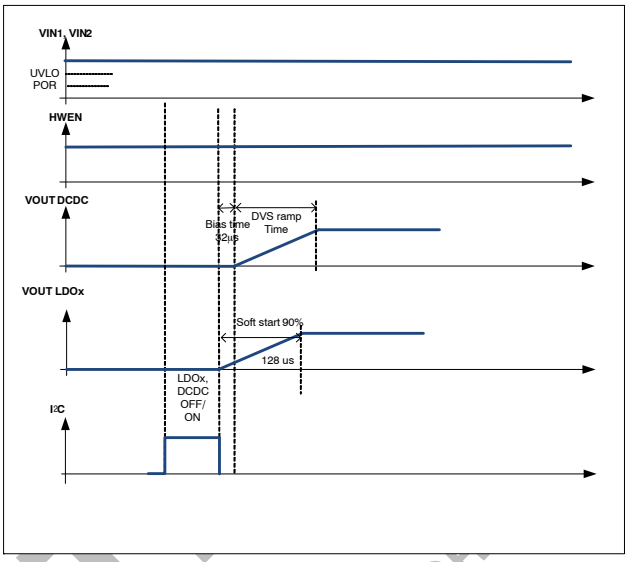


Figure 5. ON Mode PUS (OPUS)

Shutdown by HWEN

When HWEN is tied low, all supplies are disabled with reverted turn on sequence detailed in default Power Up Sequencer table. If different turn off sequence is required, a different programming can be done by I^{2}C.

DCDC Converter

The converter can operate in two modes: PWM mode and PFM mode. In PWM mode the converter operates at a fixed frequency and adapts its duty cycle to regulate to the desired output voltage. The advantage of this mode is that the EMI noise is predictable. However, at lower loadings the efficiency is degraded. In PFM mode some switching pulses are skipped to control the output voltage. This allows maintaining high efficiency even at low loadings. In addition, no high frequency clock is required which provides additional current savings. The switchover point between both modes is chosen depending on the supply conditions such that highest efficiency is obtained over the entire load range.

The switch over between PWM/PFM modes can occur automatically but the switcher can be set in auto switching mode PFM / PWM by I^{2}C programming.

A soft start is provided to limit inrush currents when enabling the converters. The soft start consists of ramping gradually the reference to the switcher.

Additional current limitation is provided by a peak current limiter that monitors and limits the current through the inductor.

DCDC converter output voltage can be set by I^{2}C

MODEDCDC bit is used to program switcher mode control

Table 6. MODEDCDC BIT DESCRIPTION

MODEDCDC	DCDC Mode Control
0	Mode is auto switching PFM / PWM (default)
1	Mode is PWM only

Dynamic Voltage Scaling (DVS)

Step down converters support dynamic voltage scaling (DVS). This means the output voltage can be reprogrammed based upon I²C commands to provide the different voltages required by the processor. The change between set points is managed in a smooth manner without disturbing the operation of the processor.

When programming a higher voltage, the reference of the switcher and therefore the output is raised in 50 mV/ 2.67 µs (default) steps such that the dV/dt is controlled. When programming a lower voltage the output voltage will decrease based on the output capacitor value and the load. The DVS system makes sure that the voltage ramp down will not exceed the steps settings.

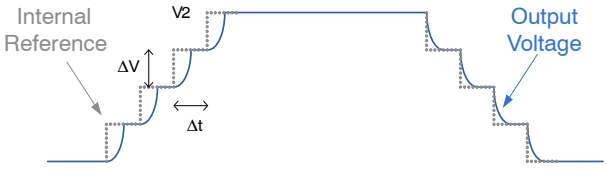


Figure 6. Dynamic Voltage Scaling Effect Timing

Programmability

DCDC converter has two different output voltages programmed by default in the DCDC_V1 and V2 bank. The DCDC output voltage can be changed from V1 to V2 with the DCDC_V2/V1 bit in $08 register.

Table 7. DCDC_V2/1 BIT DESCRIPTION

DCDC_V2/1	Bit Description
0	Output voltage is set to DCDC_V2
1	Output voltage is set to DCDC_V1 (Default)

The two DVS bits in register TIME determine ramp up time per each voltage step.

Table 8. DVS BIT DESCRIPTION

DVS [0]	Bit Description
0	2.67 µs per step (default)
1	10.67 µs per step

DCDC Step Down Converter and LDOs End of Turn on Sequence

To indicate the end of the power up sequence, a power good sense bit is available at the $0A address. (SEN_PG). Sense bit is set to 0 during power up sequence and 16 x digital clock (128 µs by default). The Power good sense bit is released to 1 after this sequence and trig ACK_PG interrupt. The interrupt is reset by a read or HWEN.

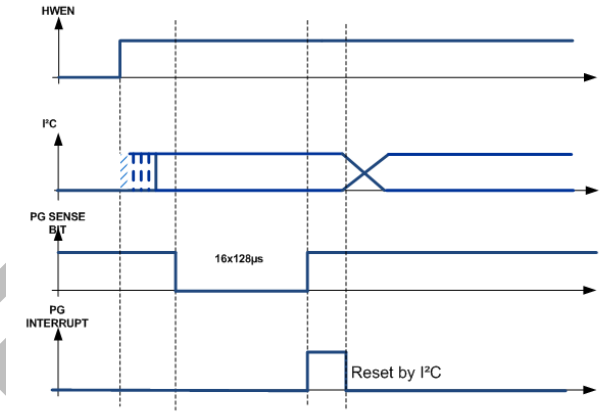


Figure 7. Power good behavior

Interrupt

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 9. INTERRUPT SOURCES

Register	$0B
UVLO	Under voltage threshold
PUS	End of power up sequence
WNRG	Thermal warning
TSD	Thermal shutdown

Individual bits generating interrupts will be set to 1 in the INT_ACK register (I²C read only register), indicating the interrupt source. INT_ACK register is reset by an I²C read. INT_SEN registers (read only registers) are real time indicators of interrupt sources.

Force Register Reset

The I²C registers are reset when the part is in Off Mode:

- Vin<UVLO or
- I²C and HWEN not present or
- Restart from TSD event (REARM_ TSD[7:6]=00, register $09)

TYPICAL OPERATING CHARACTERISTICS

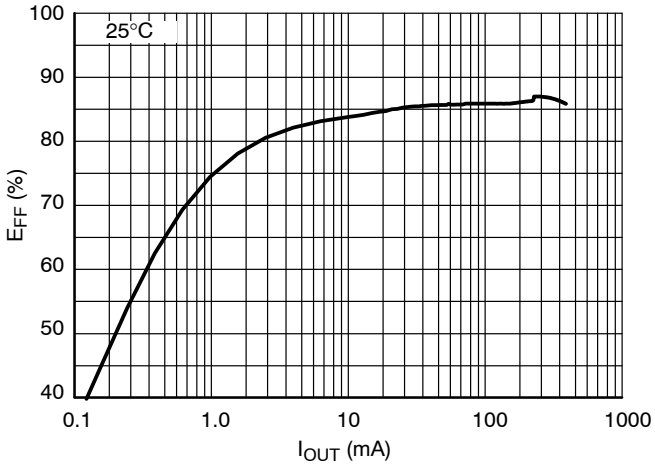


Figure 8. Efficiency versus Iout (Auto Mode) L= 1 µH (TOKO DFE2016), Vin = 5 V, Vout 1.2 V, Cin 2.2 µF, Cout 10 µF

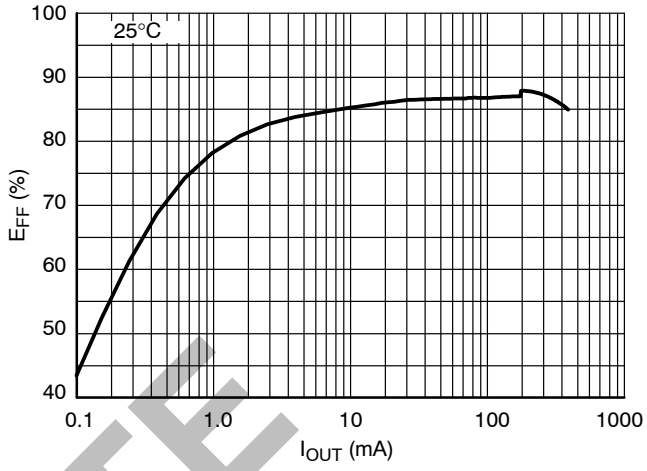


Figure 9. Efficiency versus Iout (Auto Mode) L= 1 µH (TOKO DFE2016), Vin = 3.6 V, Vout 1.2 V, Cin 2.2 µF, Cout 10 µF

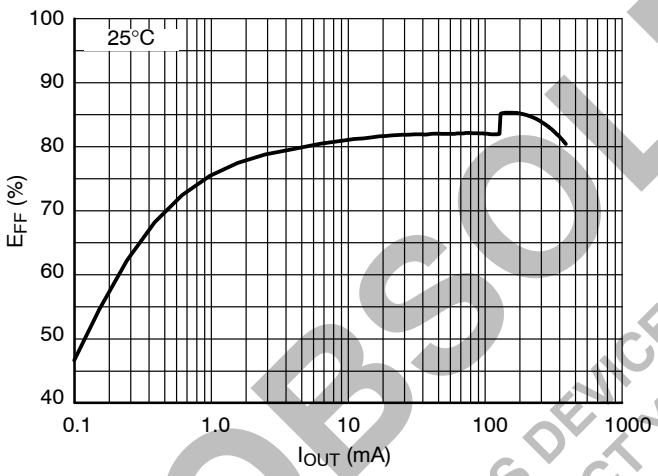


Figure 10. Efficiency versus Iout (Auto Mode) L= 1 µH (TOKO DFE2016), Vin = 2.9 V, Vout 1.2 V, Cin 2.2 µF, Cout 10 µF

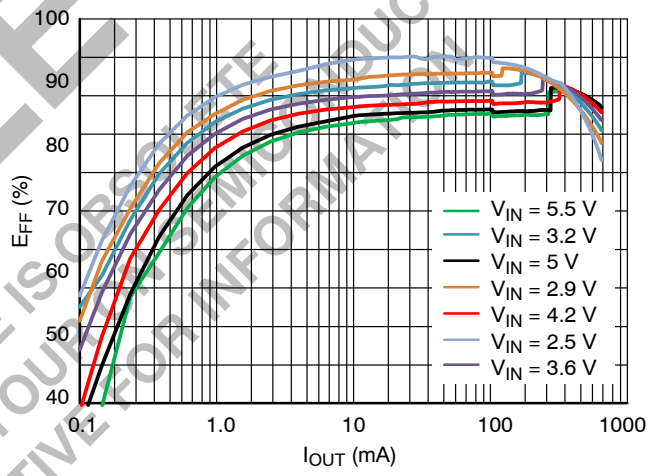


Figure 11. Efficiency versus Iout (auto mode) L= 1 µH (TOKO DFE2016), , Vout 2.3 V, Cin 2.2 µF, Cout 10 µF

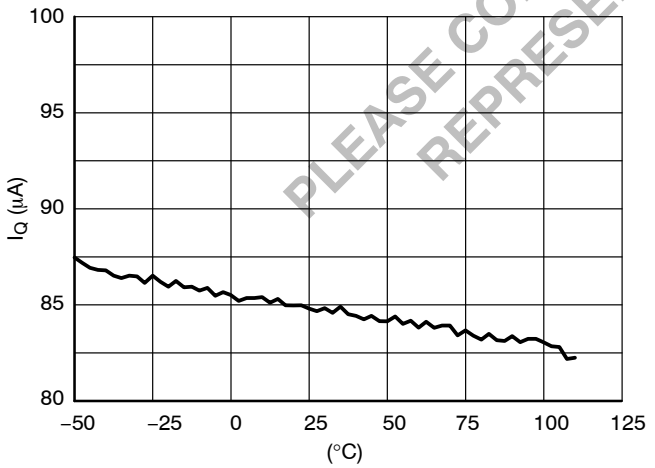


Figure 12. Quiescent current versus Vinx and PVIN Tied Together HWEN high, LDOs on, DCDC on, No Switching

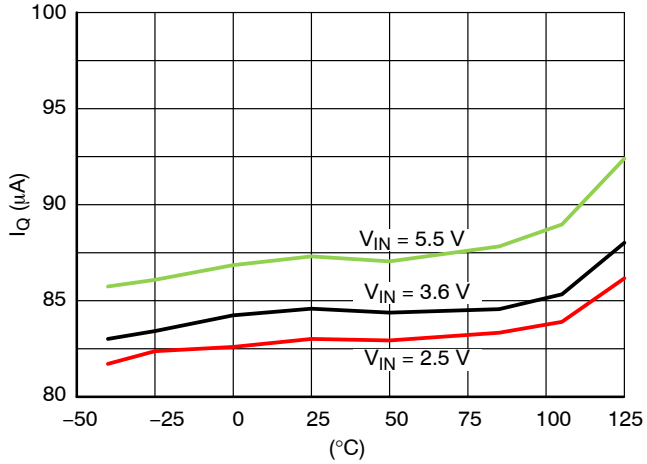


Figure 13. Quiescent Current versus Temperature, Vinx and PVIN Tied Together HWEN High, LDOs on, DCDC On, No Switching

TYPICAL OPERATING CHARACTERISTICS

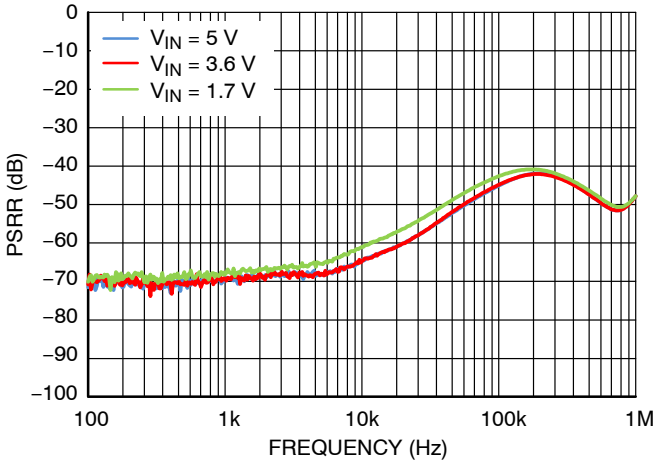


Figure 14. LDO4 PSRR

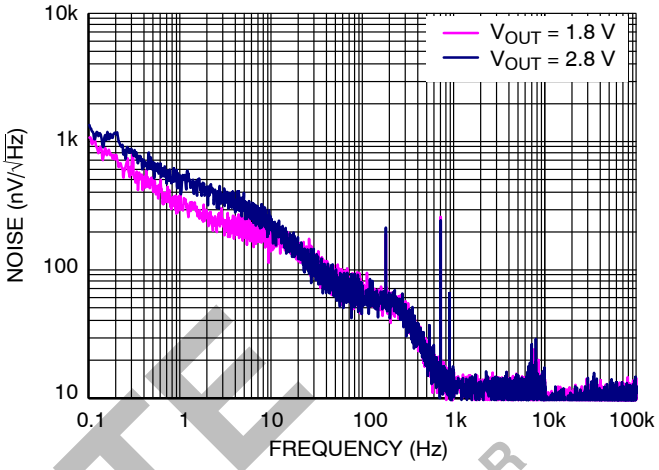


Figure 15. LDO1 Output Noise versus Frequency and Vout, Vin 3.6 V

I²C Compatible Interface

NCP6915 can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

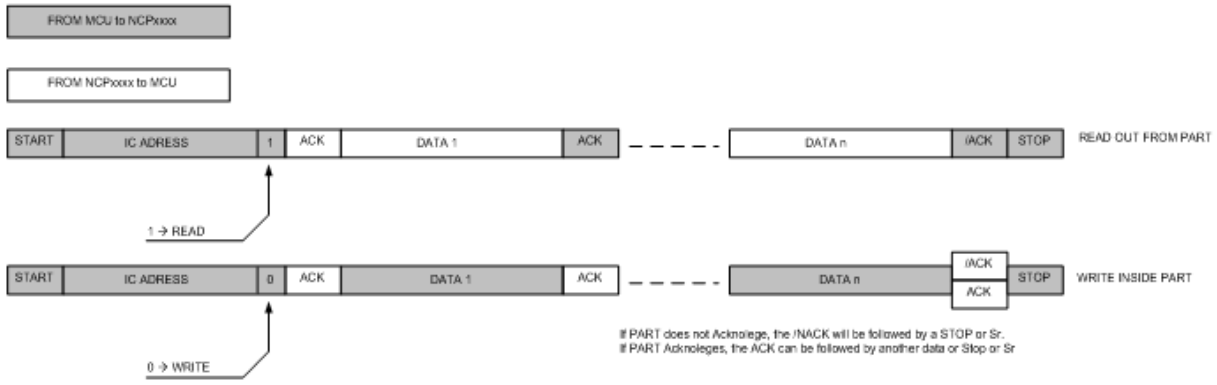


Figure 16. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1 .... The data are optional.
- In case of read operation, the NCP6915 will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

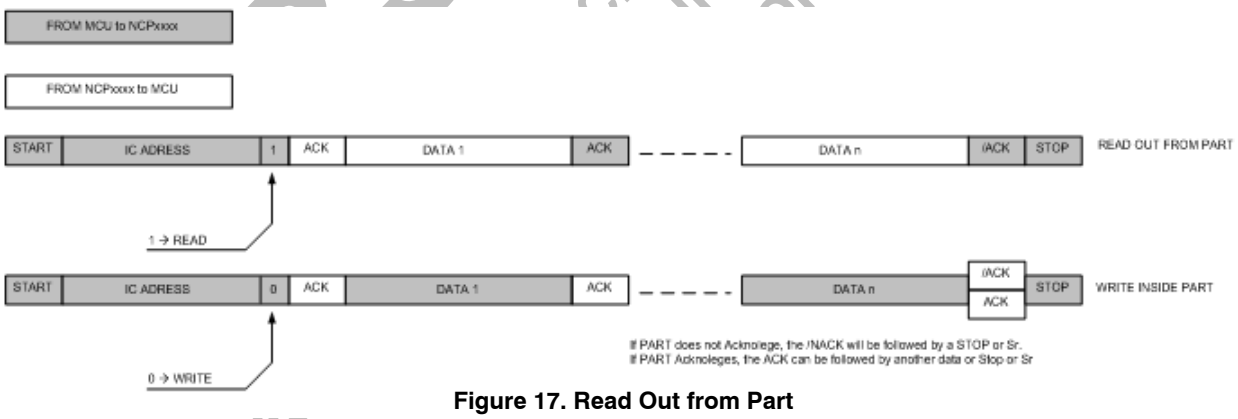


Figure 17. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

1. With Stop Then Start

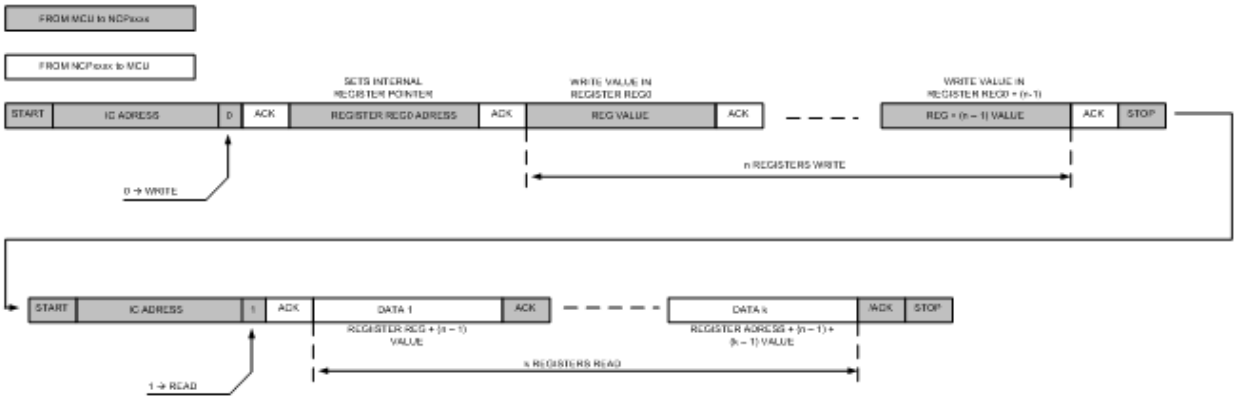


Figure 18. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg +n.

Write n Registers:

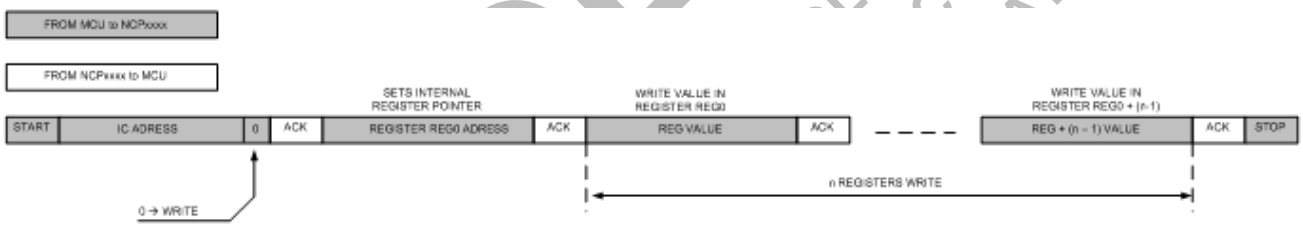


Figure 19. Write in n Registers

I²C Address

NCP6915 has fixed I²C but different I²C address (by default $10, 7 bit address, see below table A7~A1), NCP6915 supports 7−bit address only.

Table 10. NCP6915 I²C ADDRESS

Device	I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
NCP6915AFCCLT1G	ADD0 (Default)	W $20 /R $21	0	0	1	0	0	0	0	X
	ADDRESS	$10	0	0	1	0	0	0	0	–
NCP6915BFCCLT1G	ADD0 (Default)	W $30 /R $31	0	0	1	1	0	0	0	X
	ADDRESS	$18	0	0	1	1	0	0	0	–

Register Map

Following register map describes I^2C registers.

Registers can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
RWM	Read, Write and can be modified by the IC
Reserved	Address is reserved and register is not physically designed
Spare	Address is reserved and register is physically designed

Table 11. REGISTERS SUMMARY

Address	Register Name	Type	Default	Function
$00	GENERAL_SETTINGS	RW	$00	DVS control Settings
$01	LDO1_SETTINGS	RW	$39	LDO1 register settings
$02	LDO2_SETTINGS	RW	$79	LDO2 register settings
$03	LDO3_SETTINGS	RW	$8C	LDO3 register settings
$04	LDO4_SETTINGS	RW	$BE	LDO4 register settings
$05	LDO5_SETTINGS	RW	$D1	LDO5 register settings
$06	DCDC_SETTINGS1	RW	$15	DCDC register settings 1
$07	DCDC_SETTINGS2	RW	$13	DCDC register settings 2
$08	ENABLE	RW	$80	Enable and DVS register settings
$09	PULLDOWN	RW	$3F	Active discharge and rearming register
$0A	STATUS	R	$04	Status or sense register
$0B	INTERRUPT_ACK	RC	$00	Interrupt register
$0C to $FF	–	–	–	Reserved, Do not access to those registers

Details of the registers are in the following section.

Registers Description

Table 12. GENERAL_SETTINGS REGISTER

Name: GENERAL_SETTINGS				Address: $00			
Type: RW				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
spare = 0	spare = 0	spare = 0	DVS	spare = 0	spare = 0	spare = 0	spare = 0

Table 13. BIT DESCRIPTION OF GENERAL_SETTINGS REGISTER

Bit	Bit Description
DVS[0]	Ramp up time per voltage step

Table 14. LDO1_SETTINGS REGISTER

Name: LDO1_SETTINGS				Address: $01			
Type: RW				Default: $39			
D7	D6	D5	D4	D3	D2	D1	D0
LDO1_T [2:0]			LDO1_V[4:0]				

Table 15. BIT DESCRIPTION OF LDO1_SETTINGS REGISTER

Bit	Bit Description
LDO1_V[4:0]	LDO1 output voltage setting, refer to Table 16
LDO1_T[2:0]	LDO1 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO1 startup Delay time = (LDO1_T[2:0] + 1) * 128 μs Remark: it's not recommended to use same LDOx_T for two consecutives LDOs.

64 μs, 128 μs, 1 ms, 2 ms OTP options (128 μs default value)

Table 16. LDO2_SETTINGS REGISTER

Name: LDO2_SETTINGS				Address: $02			
Type: RW				Default: $79			
D7	D6	D5	D4	D3	D2	D1	D0
LDO2_T [2:0]				LDO2_V[4:0]			

Table 17. BIT DESCRIPTION OF LDO2_SETTINGS REGISTER

Bit	Bit Description
LDO2_V[4:0]	LDO2 output voltage setting, refer to Table 16
LDO2_T[2:0]	LDO2 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO2 startup Delay time = (LDO2_T[2:0] + 1) * 128 μs Remark: it's not recommended to use same LDOx_T for two consecutives LDOs.

Table 18. LDO3_SETTINGS REGISTER

Name: LDO3_SETTINGS					Address: $03		
Type: RW					Default: $8C		
D7	D6	D5	D4	D3	D2	D1	D0
LDO3_T [2:0]			LDO3_V[4:0]				

Table 19. BIT DESCRIPTION OF LDO3_SETTINGS REGISTER

Bit	Bit Description
LDO3_V[4:0]	LDO3 output voltage setting, refer to Table 16
LDO3_T[2:0]	LDO3 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO3 startup Delay time = (LDO3_T[2:0] + 1) * 128 μs Remark: it's not recommended to use same LDOx_T for two consecutives LDOs.

Table 20. LDO1_V[4:0], LDO2_V[4:0], LDO3_V[4:0] SETTING TABLE

Register	Vout (V)	Register	Vout (V)	Register	Vout (V)	Register	Vout (V)
00000	1.70	01000	1.70	10000	2.10	11000	2.75
00001	1.70	01001	1.70	10001	2.20	11001	2.80
00010	1.70	01010	1.70	10010	2.30	11010	2.85
00011	1.70	01011	1.75	10011	2.40	11011	2.90
00100	1.70	01100	1.80	10100	2.50	11100	2.95
00101	1.70	01101	1.85	10101	2.60	11101	3.00
00110	1.70	01110	1.90	10110	2.65	11110	3.10
00111	1.70	01111	2.00	10111	2.70	11111	3.30

Table 21. LDO4_SETTINGS REGISTER

Name: LDO4_SETTINGS				Address: $04			
Type: RW				Default: $BE			
D7	D6	D5	D4	D3	D2	D1	D0
LDO4_T [2:0]				LDO4_V[4:0]			

Table 22. BIT DESCRIPTION OF LDO4_SETTINGS REGISTER

Bit	Bit Description
LDO4_V[4:0]	LDO4 output voltage setting, refer to Table 21
LDO4_T[2:0]	LDO4 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO4 startup Delay time = (LDO4_T[2:0] + 1) * 128 μs Remark: it's not recommended to use same LDOx_T for two consecutives LDOs.

Table 23. LDO5_SETTINGS REGISTER

Name: LDO5_SETTINGS				Address: $05			
Type: RW				Default: $D1			
D7	D6	D5	D4	D3	D2	D1	D0
LDO5_T [2:0]				LDO5_V[4:0]			

Table 24. BIT DESCRIPTION OF LDO5_SETTINGS REGISTER

Bit	Bit Description
LDO5_V[4:0]	LDO5 output voltage setting, refer to Table 21
LDO5_T[2:0]	LDO5 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO5 startup Delay time = (LDO5_T[2:0] + 1) * 128 μs Remark: it's not recommended to use same LDOx_T for two consecutives LDOs.

Table 25. LDO4_V[4:0], LDO5_V[4:0] SETTING TABLE

Register	Vout (V)	Register	Vout (V)	Register	Vout (V)	Register	Vout (V)
00000	1.20	01000	1.35	10000	1.75	11000	2.40
00001	1.20	01001	1.40	10001	1.80	11001	2.50
00010	1.20	01010	1.45	10010	1.85	11010	2.60
00011	1.20	01011	1.50	10011	1.90	11011	2.65
00100	1.20	01100	1.55	10100	2.00	11100	2.70
00101	1.20	01101	1.60	10101	2.10	11101	2.75
00110	1.25	01110	1.65	10110	2.20	11110	2.80
00111	1.30	01111	1.70	10111	2.30	11111	2.85

Table 26. DCDC_SETTINGS1 REGISTER

Name: DCDC_SETTINGS1				Address: $06			
Type: RW				Default: $15			
D7	D6	D5	D4	D3	D2	D1	D0
DCDC_T[2:0]				DCDC_V1[4:0]			

Table 27. BIT DESCRIPTION OF DCDC_SETTINGS1 REGISTER

Bit	Bit Description
DCDC_V1[4:0]	DCDC output voltage setting 1, refer to Table 25
DCDC_T[2:0]	DCDC startup delay time setting (delay time between HWEN transitions from LOW to High and DCDC startup Delay time = (DCDC_T[2:0] + 1) * 128μs

Table 28. DCDC_SETTINGS2 REGISTER

Name: DCDC_SETTINGS2				Address: $07			
Type: RW				Default: $13			
D7	D6	D5	D4	D3	D2	D1	D0
spare = 0	spare = 0	MODEDCDC	DCDC_V2[4:0]				

Table 29. BIT DESCRIPTION OF DCDC_SETTINGS2 REGISTER

Bit	Bit Description
DCDC_V2[4:0]	DCDC output voltage setting 2, refer to Table 25
MODEDCDC	DCDC Operating Mode 0: Auto switching PFM / PWM (default) 1: Forced PWM

Table 30. DCDC_Vx[4:0] SETTING TABLE

DCDC_V1/2	Vout (V)	DCDC_V1/2	Vout (V)	DCDC_V1/2	Vout (V)	DCDC_V1/2	Vout (V)
00000	0.80 V	01000	1.15 V	10000	1.55 V	11000	1.95 V
00001	0.80 V	01001 (V1)*	1.20 V	10001	1.60 V	11001	2.00 V
00010	0.85 V	01010	1.25 V	10010	1.65 V	11010	2.05 V
00011	0.90 V	01011	1.30 V	10011	1.70 V	11011	2.10 V
00100	0.95 V	01100	1.35 V	10100	1.75 V	11100	2.15 V
00101	1.00 V	01101	1.40 V	10101	1.80 V	11101	2.20 V
00110	1.05 V	01110	1.45 V	10110	1.85 V	11110	2.25 V
00111 (V2)	1.10 V	01111	1.50 V	10111	1.90 V	11111	2.30 V

*Default value: V1

Table 31. ENABLE REGISTER

Name: ENABLE				Address: $08			
Type: RW				Default: $80			
D7	D6	D5	D4	D3	D2	D1	D0
DCDC_V2/V1	spare = 0	DCDC_ EN	LDO5_ EN	LDO4_ EN	LDO3_ EN	LDO2_ EN	LDO1_ EN

Table 32. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
DCDC_V2/V1	DCDC output voltage setting 0: DCDC converter output voltage is set to DCDC_V2 1: DCDC converter output voltage is set to DCDC_V1
DCDC_ EN	DCDC Enabling 0: Disabled 1: Enabled

Table 32. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
LDO5_ EN	LDO5 Enabling 0: Disabled 1: Enabled
LDO4_ EN	LDO4 Enabling 0: Disabled 1: Enabled
LDO3_ EN	LDO3 Enabling 0: Disabled 1: Enabled
LDO2_ EN	LDO2 Enabling 0: Disabled 1: Enabled
LDO1_ EN	LDO1 Enabling 0: Disabled 1: Enabled

Table 33. PULLDOWN REGISTER

Name: PULLDOWN				**Address: $09**			
Type: RW				**Default: $3F**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
REARM_ TSD[7]	REARM_ TSD[6]	DCDC_ PULLDOWN	LDO5_ PULLDOWN	LDO4_ PULLDOWN	LDO3_ PULLDOWN	LDO2_ PULLDOWN	LDO1_ PULLDOWN

Table 34. BIT DESCRIPTION OF PULLDOWN REGISTER

Bit	Bit Description
REARM_ TSD[7:6]	Device Rearming after Thermal Shut Down 11: N/A 10: No re−arming after TSD 01: Re-arming active after TSD with no reset of I^2C registers: new power-up sequence is initiated with I^2C registers values. 00: Re-arming active after TSD with reset of I^2C registers: new power-up sequence is initiated with default I^2C registers values (default).
DCDC_ PULLDOWN	DCDC active output discharge 0: Disabled 1: Enabled
LDO5_ PULLDOWN	LDO5 active output discharge 0: Disabled 1: Enabled
LDO4_ PULLDOWN	LDO4 active output discharge 0: Disabled 1: Enabled
LDO3_ PULLDOWN	LDO3 active output discharge 0: Disabled 1: Enabled
LDO2_ PULLDOWN	LDO2 active output discharge 0: Disabled 1: Enabled
LDO1_ PULLDOWN	LDO1 active output discharge 0: Disabled 1: Enabled

Table 35. STATUS REGISTER

Name: STATUS				Address: $0A			
Type: R				Default: $04			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare = 0	spare = 0	spare = 0	spare = 0	SEN_UVLO	SEN_/PUS	SEN_TSD	SEN_WNRG

Table 36. BIT DESCRIPTION OF STATUS REGISTER

Bit	Bit Description
SEN_UVLO	UVLO sense 0: Input voltage is higher than (UVLO + hyst) threshold. 1: Input voltage is lower than (UVLO) threshold.
SEN_PUS	Power up sequence 0: Power up sequence on going 1: Power up sequence finished or HWEN is low
SEN_TSD	Thermal Shut Down sense 0: IC temperature is below TSD threshold 1: IC temperature is over TSD threshold
SEN_WNRG	Thermal warning sense 0: IC temperature is below Thermal Warning threshold 1: IC temperature is over Thermal Warning threshold

Table 37. INTERRUPT_ACK REGISTER

Name: INTERRUPT_ACK				Address: $0B			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare = 0	spare = 0	spare = 0	spare = 0	ACK_UVLO	ACK_PUS	ACK_TSD	ACK_WNRG

Table 38. BIT DESCRIPTION OF INTERRUPT_ACK REGISTER

Bit	Bit Description
ACK_UVLO	UVLO sense acknowledge 0: Cleared 1: SEN_UVLO Dual edge triggered interrupt
ACK_PUS	Power up sequence sense acknowledge 0: Cleared 1: SEN_PUS Rising edge triggered interrupt
ACK_TSD	Thermal Shut Down sense acknowledge 0: Cleared 1: SEN_TSD Dual edge triggered interrupt
ACK_WNRG	Thermal warning sense acknowledge 0: Cleared 1: SEN_WNRG Dual edge triggered interrupt

NOTE: SEN_PUS rising edge appears (16) x 128μs (default) after HWEN rising edge.

DEMOBOARD INFORMATIONS

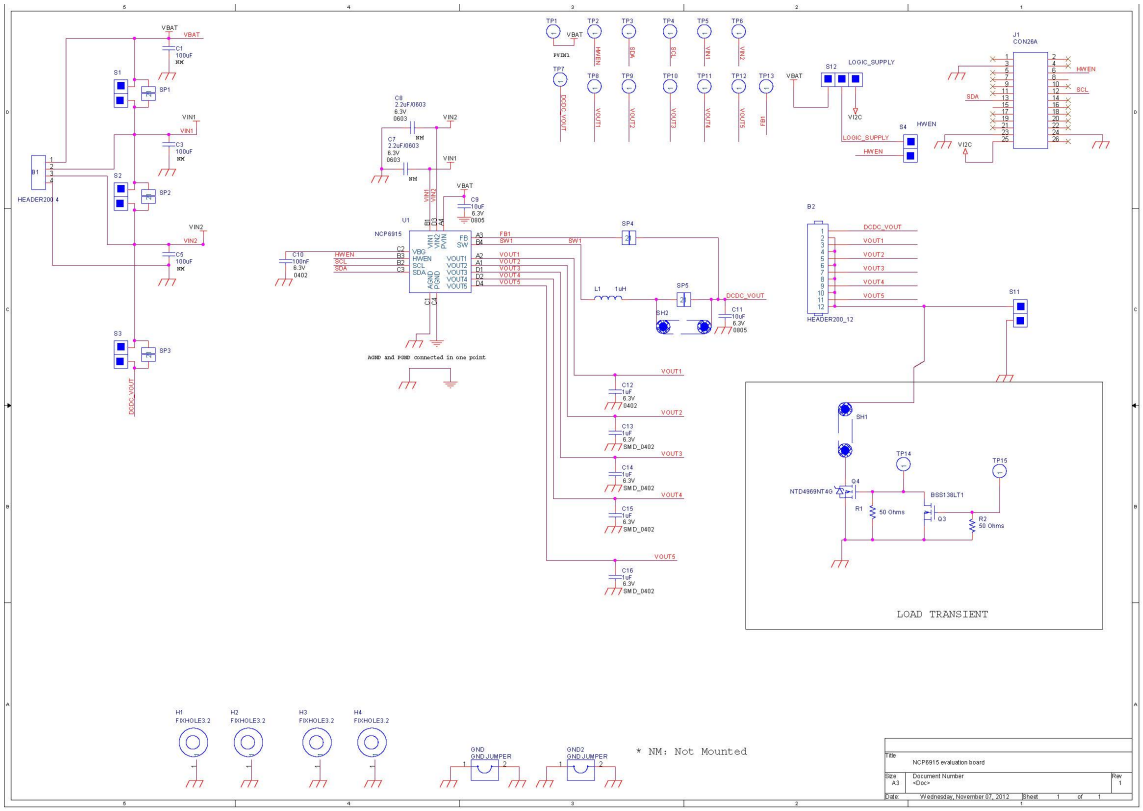


Figure 20. Demoboard Schematic

COMPONENTS SELECTION

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{L_PP} of approximately 20% to 50% of the maximum output current I_{OUT_MAX} for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 39 shows recommended.

Table 39. INDUCTOR SELECTION

Supplier	Part	Value	Size	DC Rated Current	DCR Max at 25°C
TOKO	DFE201610R−H−1R0N	1 μH	2.0 × 1.6 mm	2.2 A	48 mΩ
TOKO	MDT2012−CLR1R0AM	1 μH	2.0 × 1.2 mm	2.15 A	80 mΩ
Murata	LQM21PN1R0NGR	1 μH	2.0 × 1.2 mm	1.3 A	66 mΩ
Murata	LQM2MPN1R0NG0	1 μH	2.0 × 1.6 mm	1.4 A	85 mΩ
Cyntec	PIFE2016T−1R0	1 μH	2.0 × 1.6 mm	2 A	80 mΩ

Table 40. BOARD COMPONENTS DESCRIPTION

Quantity	Reference Schem	Part Description	Part Number	Manufacturer
1	B1	HEADER200 4	SL 5.08/4/90B	Weidmuller
1	B2	HEADER200_12	2.54 mm, 77313−101−06LF	FC
3	C1,C3,C5	100 μF	GRM31CR60J107ME39#	Murata
2	C7,C8	2.2 μF	GRM188R60J225KE19#	Murata
2	C9,C11	10 μF	GRM188R60J106ME47#	Murata
1	C10	100 nF	GRM033C801J104KE84B	Murata
5	C12,C13,C14,C15,C16	1 μF	GRM155R70J105KA12#	Murata
2	GND2,GND	GND JUMPER	D3082F05	Harvin
1	J1	CON26A	N2526−5002RB	3M
1	L1	1 μH	DFE201610R−H−1R0N	Toko
1	Q3	Nmos	BSS138LT1	ON Semiconductor
1	Q4	Nmos	NTD4969NT4G	ON Semiconductor
2	R1,R2	50 Ω	FC0603E50R0BTBST1	Vishay
4	S1,S2,S3,S11	STRAP 2pins	77311−401−36LF	FCI
1	TP2	HWEN	77311−401−36LF	FCI
1	S12	LOGIC_SUPPLY	77311−401−36LF	FCI
1	TP1	VBAT	77311−401−36LF	FCI
1	TP3	SDA	77311−401−36LF	FCI
1	TP4	SCL	77311−401−36LF	FCI
1	TP5	VIN1	77311−401−36LF	FCI
1	TP6	VIN2	77311−401−36LF	FCI
1	TP7	DCDC_VOUT	77311−401−36LF	FCI
1	TP8	VOUT1	77311−401−36LF	FCI
1	TP9	VOUT2	77311−401−36LF	FCI
1	TP10	VOUT3	77311−401−36LF	FCI
1	TP11	VOUT4	77311−401−36LF	FCI
1	TP12	VOUT5	77311−401−36LF	FCI
1	TP13	FB1	77311−401−36LF	FCI
1	TP14	SMB4	77311−401−36LF	FCI
1	TP15	SMB3	77311−401−36LF	FCI
1	U1	PMIC	NCP6915	ON Semiconductor

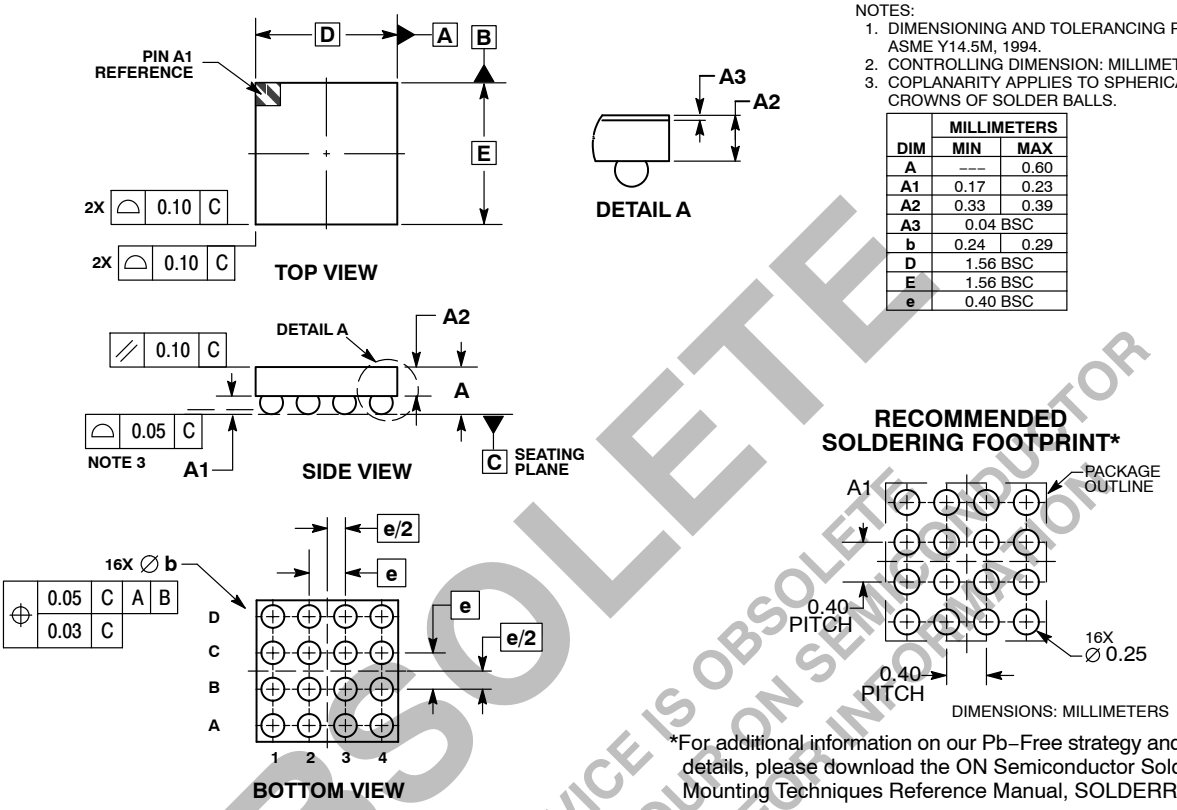
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP6915AFCCLT1G	6915A	WLCSP 1.56x1.56 mm (Pb−Free)	3000 / Tape & Reel
NCP6915BFCCLT1G (In Development)	6915B	WLCSP 1.56x1.56 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WLCSP16, 1.56x1.56
CASE 567GF
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.33	0.39
A3	0.04 BSC	
b	0.24	0.29
D	1.56 BSC	
E	1.56 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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