Technical Guide 2021

CeraLink Capacitors

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CeraLink Capacitors

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GENERAL REMARK

This document is a guideline for engineers working with CeraLink®. CeraLink is a PLZT (lead lanthanum zirconium titanate) based ceramic capacitor with anti-ferroelectric behavior, which is optimized for high frequency & high temperature power electronic applications. We exemplify this using figures and values of CeraLink LP 500 V series (P/N B58031I/U5105M 62) unless otherwise mentioned. Electrical characterization values for this type are:

$V_{pk, max}$	V_R	V_{op}	$C_{nom, typ}$	$C_{eff, typ}$	C_0
650 V	500 V	400 V	1 µF	0.6 µF	0.35 µF ±20%

Table 1: Technical parameter for CeraLink LP 500 V

The main features of CeraLink are:

- Increasing capacitance with DC bias between 0 V and V_{op} and best in class capacitance density at operating point (V_{op} & T_{op})
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- No limitation of dV/dt, i.e. suitable for fast switching, respectively, high switching frequencies (e.g. SiC or GaN applications)
- Good thermal self-regulating properties
- Qualification based on AEC-Q200
- RoHS compatible

CeraLink is not recommended for operation under constant polarity change (AC voltage) - please see chapter >Polarization< for details.

CAPACITANCE

CeraLink features a non-linear capacitance behavior, i.e. the capacitance strongly depends on external parameters such as the applied DC bias voltage or the temperature. It is important to note that CeraLink is designed to have its capacitance maximum under operating conditions, where we distinguish two scenarios:

1. DC-Link operation, i.e. operation under a DC bias (constant operating voltage) and with a superimposed ripple amplitude. As explained in the following, for this scenario it depends on the amplitude of the superimposed ripple voltage, whether the effective capacitance C_{eff} or the nominal capacitance C_{nom} should be considered.*
2. Snubbering / Filtering, i.e. operation to filter out voltage spikes. These voltage spikes can be superimposed on a specific DC bias voltage, e.g. the characteristic voltage spikes that are superimposed on the operating voltage during fast semiconductor switching as shown in Figure 1.
   Or the voltage spikes are induced by fast current switching of an inductive load, e.g. when disconnecting an electric motor or pump from the battery supply in a protection circuit. In this case, the voltage may start from 0 V to some peak voltage.
   In all these scenarios, the applied current is limited only indirectly by the maximally rated device temperature of 150 °C, where we note that operation above rated temperature is possible in principle but not recommended since it will affect lifetime of the capacitor significantly. Furthermore, the induced voltage spikes must not exceed the maximally allowed peak voltage $V_{pk,\,max}$ for a given CeraLink type, i.e. short voltage pulses ranging from 0 V to $V_{pk,\,max}$ are tolerable and there is no limit on dV/dt, respectively, dV/dt is limited by the intrinsic ESR of the capacitor.
   Usually in all these scenarios, the nominal capacitance C_{nom} can be considered. This is also commonly referred to as the large signal capacity. Details about the definition and how to measure the large signal capacitance are explained in section >Measurement of Cnom (nominal capacitance)<.

* We note that the full nominal capacitance C_{nom} can be achieved only if the voltage seen by the CeraLink capacitor spans a sufficiently large range in the hysteresis loop as explained in section >Measurement of Cnom (nominal capacitance)<. This is typically fulfilled in a snubber application, whereas for DC Link applications a capacitance in a range between C_{eff} and C_{nom} can be obtained realistically. The exact value depends on the superimposed ripple amplitude. Further details will be provided in section >Capacitance Calculation<.

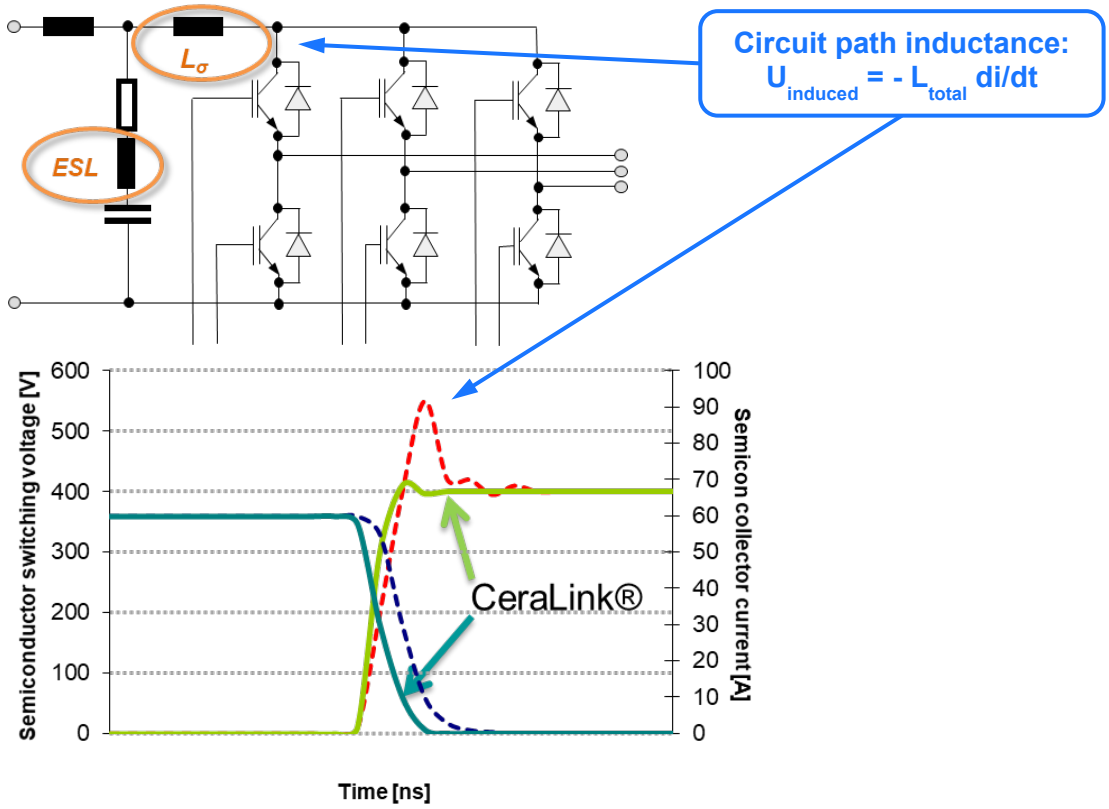


Figure 1: Semiconductor overshoot principle. The larger the overall inductance, the larger are the induced voltage spikes during switching. Thanks to the high temperature rating of 150 °C, CeraLink capacitors can be mounted close to the semiconductors and therefore minimizing the overall conductance loop.

Note that the specific operating voltage V_{op} for all CeraLink types is usually 100 V below the rated voltage V_R, i.e. in case of the LP 500 V, the operating voltage is 400 V. This is also the regime in which the component provides the maximal capacitance.

Due to this intrinsic non-linearity, there are usually three different capacitance values stated in the CeraLink data sheets: the initial capacitance C_0, the effective capacitance C_{eff}, and the nominal capacitance C_{nom}, where the latter value defines the rated capacitance of a CeraLink capacitor:

Initial capacitance C_0: measured at 0 V_{DC}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature

This means no DC bias and just a small AC voltage is applied (this measurement corresponds to a usual incoming inspection test with LCR-meter)

Effective capacitance C_{eff}: measured at operating voltage V_{op}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature

Same as the C_0 measurement but with a DC bias (constant operating voltage), which is in this case operating voltage V_{op}. This measurement corresponds to the usual operation under DC link voltage with a small superimposed ripple amplitude. Throughout, this will be also denoted as the small signal capacitance.

Nominal capacitance C_{nom}: measured at operating voltage V_{op}, quasistatic, room temperature

The nominal capacitance value is derived from the maximum of the mean hysteresis through the common definition C = dQ/dV. Throughout, this will be also denoted as the large signal capacitance. The measurement is explained in the chapter >Measurement of C_{nom} (nominal capacitance)<.

These definitions, together with the corresponding voltage scenarios are schematically depicted in Figure 2.

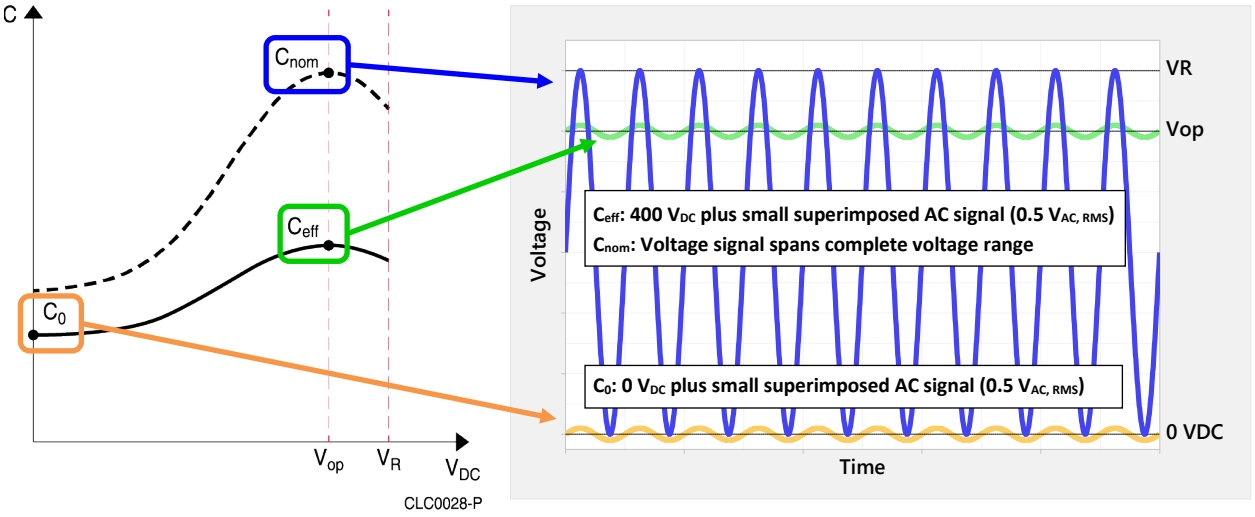


Figure 2: (left) Schematic representation of capacitance versus DC bias for small signal (solid line) and large signal (dashed line) and definition of the capacitance values C_0, C_{eff} and C_{nom}. Note that the maxima of C_{eff} and C_{nom} not necessarily overlap resp., can be slightly shifted around V_{op}. (right) Schematic representation of corresponding voltage levels. The definition of small and large signal depends on the applied voltage signal. Here, for small superimposed ripple amplitudes (small signal), the effective capacitance C_{eff} should be considered, where in the limit of very large voltage amplitudes (large signal), the nominal capacitance C_{nom} can be considered.

MEASUREMENT OF C_0 (INITIAL CAPACITANCE) AND C_{EFF} (EFFECTIVE CAPACITANCE)

The initial capacitance C_0 of CeraLink is defined using the following conditions: only a negligible external field is applied. That means that C_0 is measured at zero DC bias voltage and with a small sinusoidal AC field of 0.5 $V_{AC,\,RMS}$ at 1 kHz oscillator frequency at room temperature (small signal).

On the other hand, the effective capacitance C_{eff} is defined under the same conditions, but with a DC bias. This means that C_{eff} is measured at operating voltage V_{op} with a small sinusoidal external field of 0.5 $V_{AC,\,RMS}$ @ 1 kHz oscillator frequency at room temperature (small signal).

MEASUREMENT OF C_{NOM} (NOMINAL CAPACITANCE)

The base is a quasi-static unipolar polarization measurement, where the electrical charge on the capacitor is monitored versus the voltage. The capacitance is then obtained from the derivative C = dQ/dV.

The term “quasi-static” means that the voltage level is increased slowly enough such that the charging current is not exceeding the maximum current limit of the measurement device. Since this depends on the used measurement equipment, it can vary. Here a dV/dt value of 100 to 500 V/s is a reasonable choice and will not influence the result, as long as the current can be handled by the equipment.

For the measurement, the voltage is ramped up / down according to:

$$V(t) = k \cdot t$$

The triangular function should be chosen such that k = 100 … 500 and the maximally applied voltage is slightly below or equal to $V_{pk,max}$ for a given CeraLink type as defined in the data sheet.

The described measurement procedure and the polarization curve Q(V) is shown in the following diagrams:

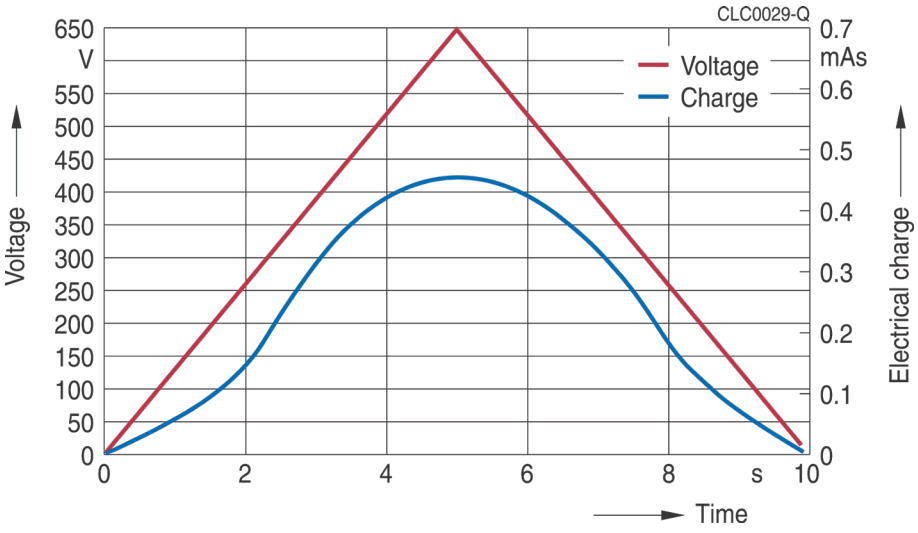


Figure 3: Electrical charge and voltage versus measurement time.

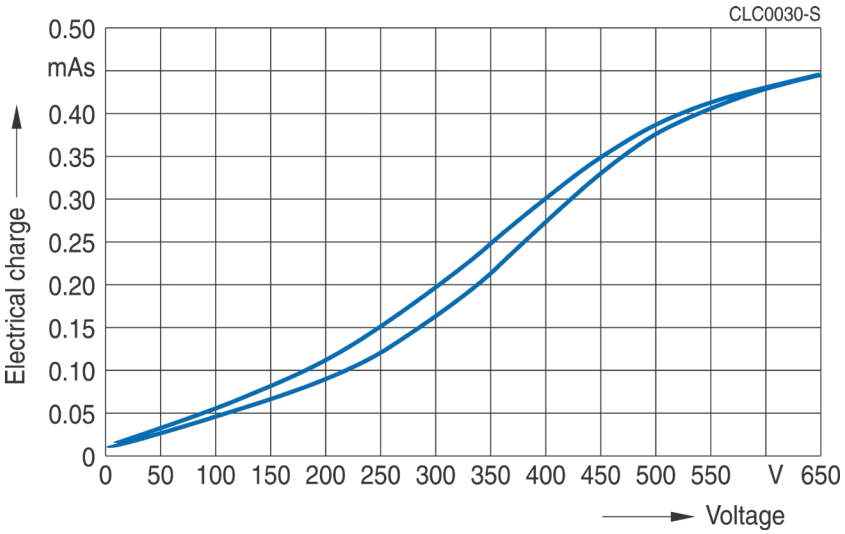


Figure 4: Electrical charge versus voltage. Note that the electrical charge will be different for different CeraLink types (in this case it is for a CeraLink LP 500 V capacitor).

The differential capacitance is defined via the derivative of the electrical charge with respect to the voltage, i.e.

$$C(V) = \frac{dQ}{dV}$$

Applying the derivative to the polarization curve shown above results in the following diagram:

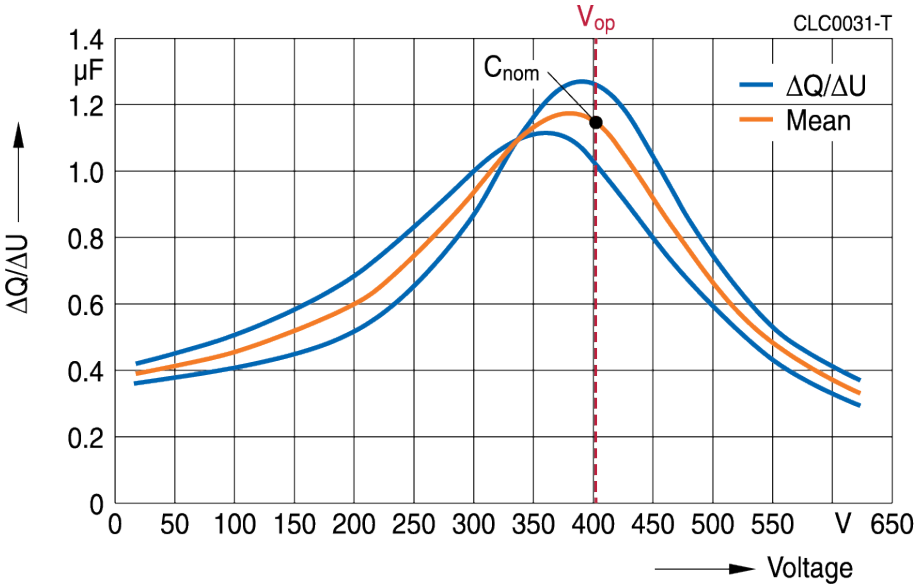
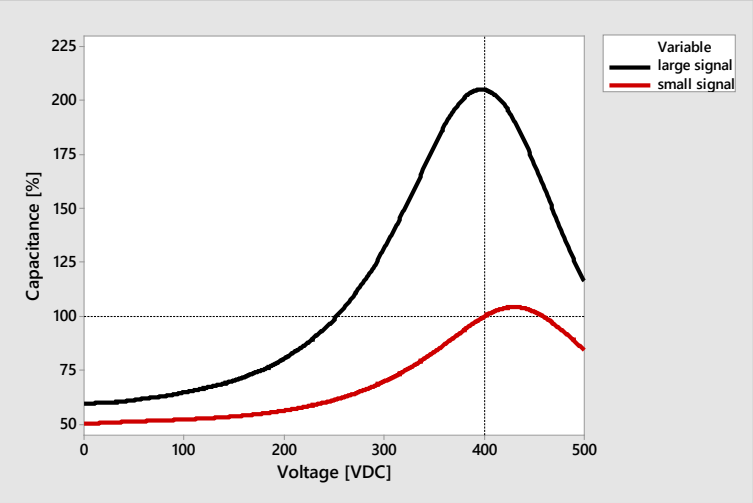


Figure 5: Derivative of hysteresis shown in Figure 4. C_{nom} corresponds to the value of the mean curve at V_{op}.

In a final step, the average between the two blue dashed envelope curves is taken. Here, the value of the curve at operating voltage V_{op} corresponds to the nominal capacitance C_{nom} as defined in the data sheet. This value corresponds roughly to the maximum of the curve, or, phrased differently, the capacitance maximum of a CeraLink is centered around its respective operating voltage V_{op}.

In Figure 6, the difference between the small signal capacitance and the large signal capacitance at room temperature for a CeraLink is shown.



The 100% value corresponds to $C_{eff, typ}$ as defined in the data sheet (see Table 1 in this document for an example).

Small signal capacitance (red curve). The effective capacitance C_{eff} corresponds to the value at V_{op} = 400 V_{DC}.

Large signal capacitance (black curve). The nominal capacitance C_{nom} corresponds to the value at V_{op} = 400 V_{DC}.

Figure 6: Capacitance measurement at large and small signal for CeraLink LP 500 V. Note that the exact location of the capacitance maxima also depends on the device temperature as discussed in the next section.

TEMPERATURE DEPENDENCE OF CAPACITANCE

Capacitance of CeraLink depends on voltage (DC bias), superimposed ripple amplitude, frequency and ambient temperature applied. Whereas the dependence on frequency is usually small (see section >Frequency Dependence of Capacitance<), the dependence on temperature is sizeable as shown in the following figures and should be considered in application.

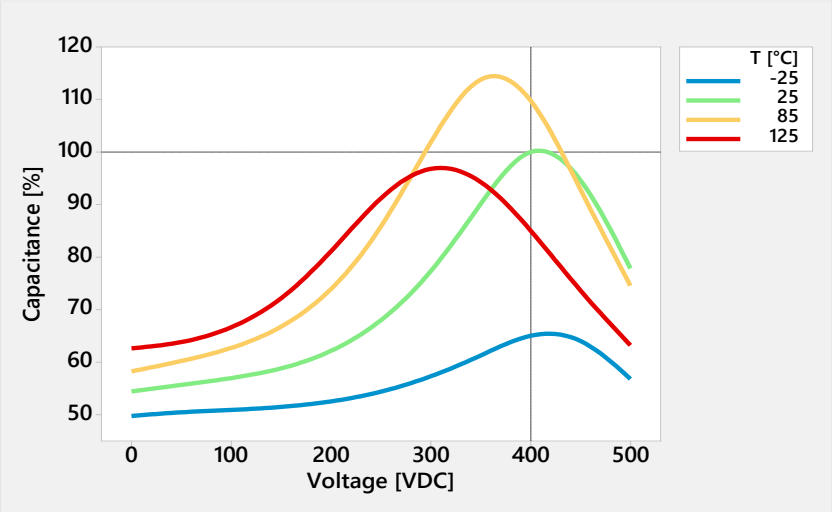


Figure 7: Voltage dependence of capacitance for different temperatures. *

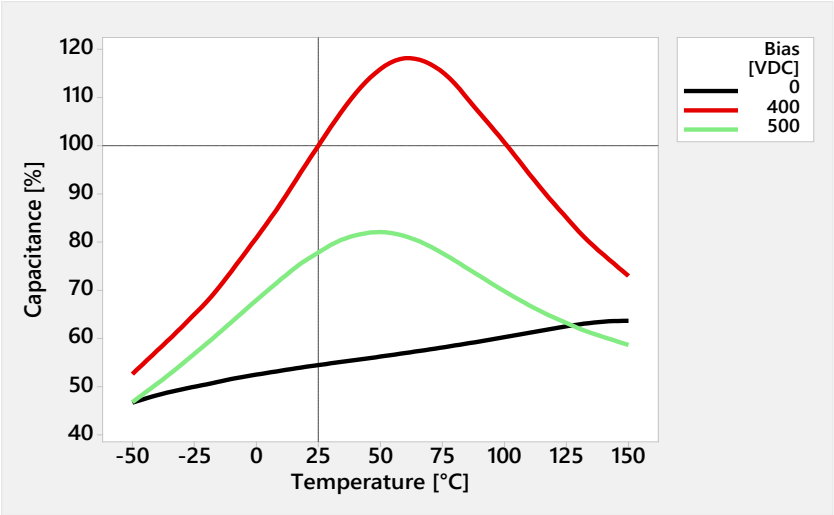


Figure 8: Temperature dependence of capacitance for different DC bias voltages. *

* The 100% value corresponds to $C_{eff, typ}$ as defined in the data sheet (see Table 1 in this document for an example).

At operating voltage, the maximum in capacitance is reached at around 60 °C, so the optimal temperature for CeraLink is in the range of +50 to +90 °C at V_{op}. It is important to note that for lower temperatures, especially below 25 °C, the device will potentially heat up more quickly as compared to other ceramic capacitors (e.g. C0G or X7R) in order to reach an optimal working point. This “feel-good” temperature can be significantly higher than the ambient temperature and is caused by the increased ESR at low temperatures as shown in Figure 10. Due to low losses at high temperature, CeraLink can carry more current under high temperature conditions.

On the other hand, for higher temperatures, the capacitance drops, which provides excellent thermal self-regulating properties since in operation, the hottest capacitor will draw less current and vice versa, i.e. hotspots can be avoided and the risk of a thermal runaway can be minimized.

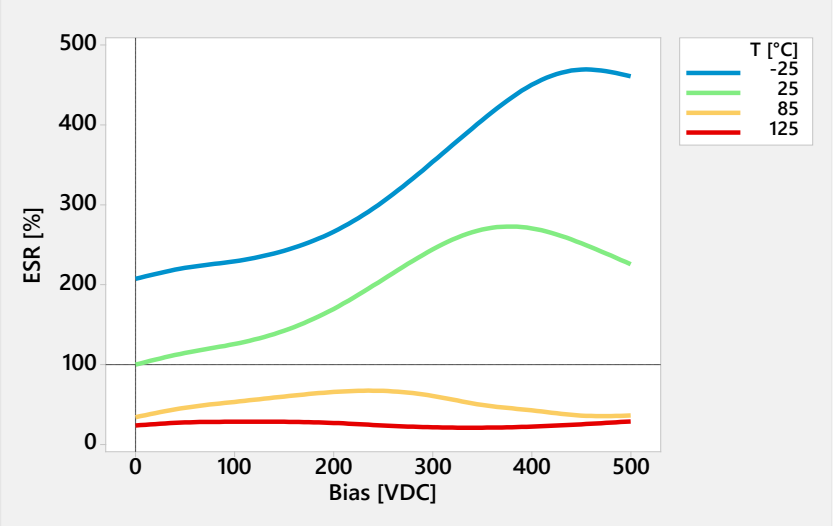


Figure 9: DC bias dependence of ESR for different temperatures. *

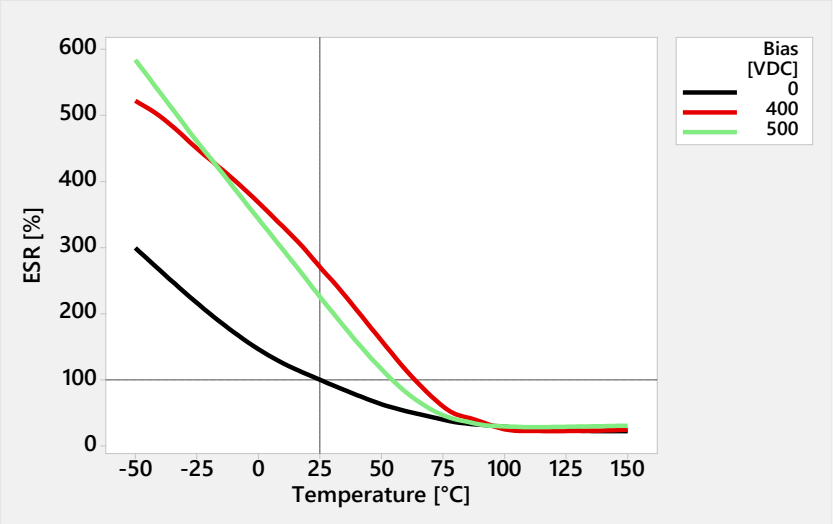
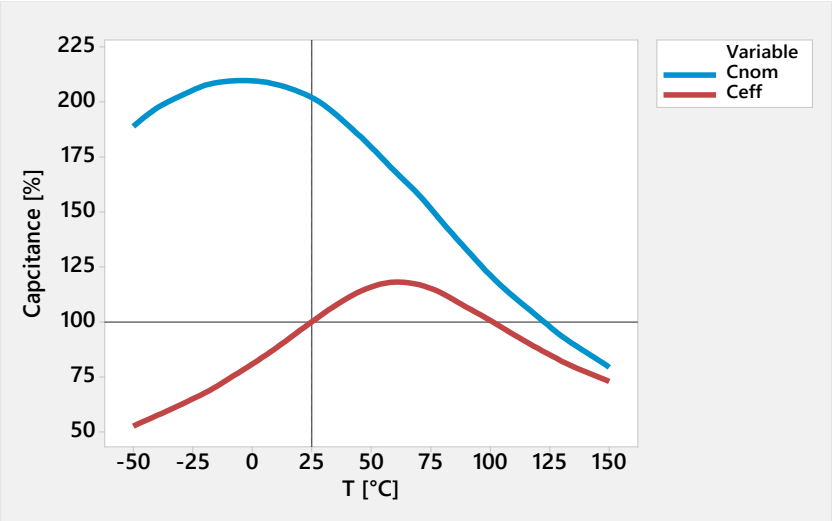


Figure 10: Temperature dependence of ESR for different DC bias voltages. *

* The 100% value corresponds to the typical ESR value as defined in the data sheet (i.e. typical ESR @ 0 V_{DC}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature)

In Figure 11, the temperature dependence of the effective capacitance C_{eff} and the nominal capacitance C_{nom} is shown. As detailed previously, C_{eff} and C_{nom} corresponds to the small signal capacitance (small AC ripple) and the large signal capacitance (voltage signal spans full voltage range), evaluated at V_{op} which in this case is 400 V_{DC}. Note that C_{nom} does not show the significant temperature drop in the low temperature regime as compared to C_{eff}. Above 70 °C operating temperature, dependence of the effective capacitance on AC ripple decreases and the two capacitances convergence.



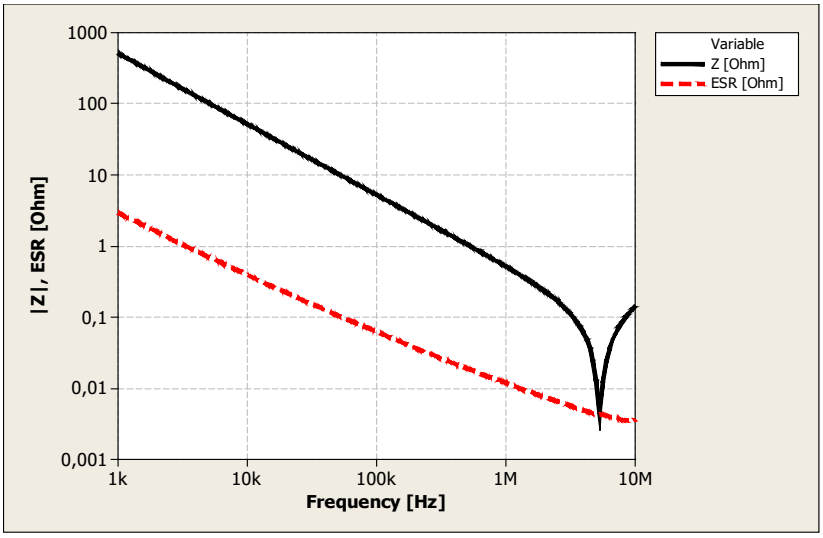
The 100% value corresponds to $C_{eff,typ}$ as defined in the data sheet (see Table 1 in this document for an example).

Figure 11: Typical nominal capacitance C_{nom} versus typical effective capacitance C_{eff} for different temperatures for a LP 500 V.

Furthermore, it is important to note that CeraLink is designed in particular for high switching frequencies, where at lower frequencies (below 10 kHz) ESR and impedance will be significantly higher as shown in Figure 12.

Optimal values are obtained in the range of 100 kHz to MHz at room temperature. However, as shown in Figure 10, the effective ESR for a realistic application temperature of 75 °C and higher, will be orders of magnitude lower.

As mentioned before, there is basically no limitation of dV/dt, i.e. the limit is imposed by the intrinsic ESR of the capacitor. Same is true for short peak current pulses which are in principle limited only by two factors, *1)* the overall induced voltage on the capacitor must stay below $V_{pk,max}$ and *2)* the induced device temperature stays within the rated limit.



$V = 0\ V_{DC} + 0.5\ V_{AC,\ RMS}$

$T_{device} = 25\ °C$

Equivalent circuit:

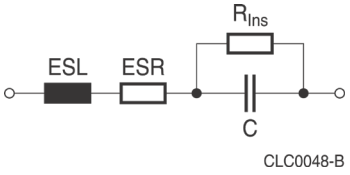


Figure 12: Impedance curve of CeraLink LP 500 V

FREQUENCY DEPENDENCE OF CAPACITANCE

The frequency dependence of the small signal capacitance (C_0) is shown in Figure 13. Up to the resonance frequency at around 5 MHz, the capacitance is relatively constant. Typical deviations of max. -3% in the frequency range 1 kHz to 1 MHz can be expected.

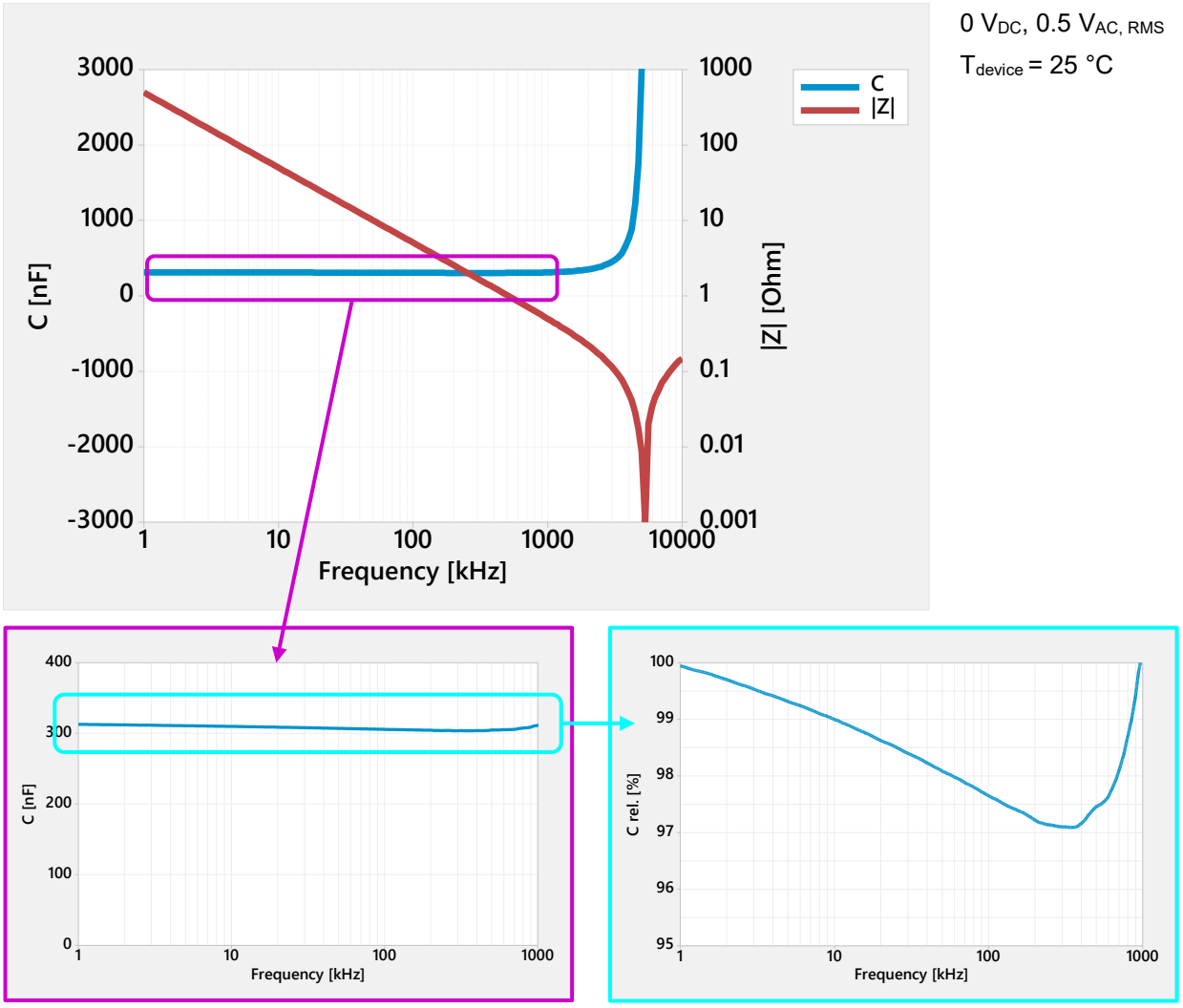


Figure 13: Frequency dependence of small signal capacitance C_0 of CeraLink LP 500 V.

CAPACITANCE CALCULATION

In the following example we consider a CeraLink LP 500 V which has a typical effective capacitance $C_{eff,\ typ}$ = 600 nF. The application conditions are:
$V_{DC\ bias}$ = 350 V, f_{ripple} = 50 kHz, T_{device} = 115 °C. Note that it is not relevant whether the device temperature is caused by the self-heating or by ambient temperature, i.e. it could be T_{amb} = 80 °C and ΔT = 35 °C, resulting in T_{device} = 115 °C. Furthermore, we consider the three scenarios with

1) a small superimposed ripple voltage (0.5 $V_{AC,\ RMS}$) – see green curve below

2), an intermediate superimposed ripple voltage (20 $V_{AC,\ RMS}$) – see red curve below

3), a large signal (voltage signal covers full voltage range) – see blue curve below

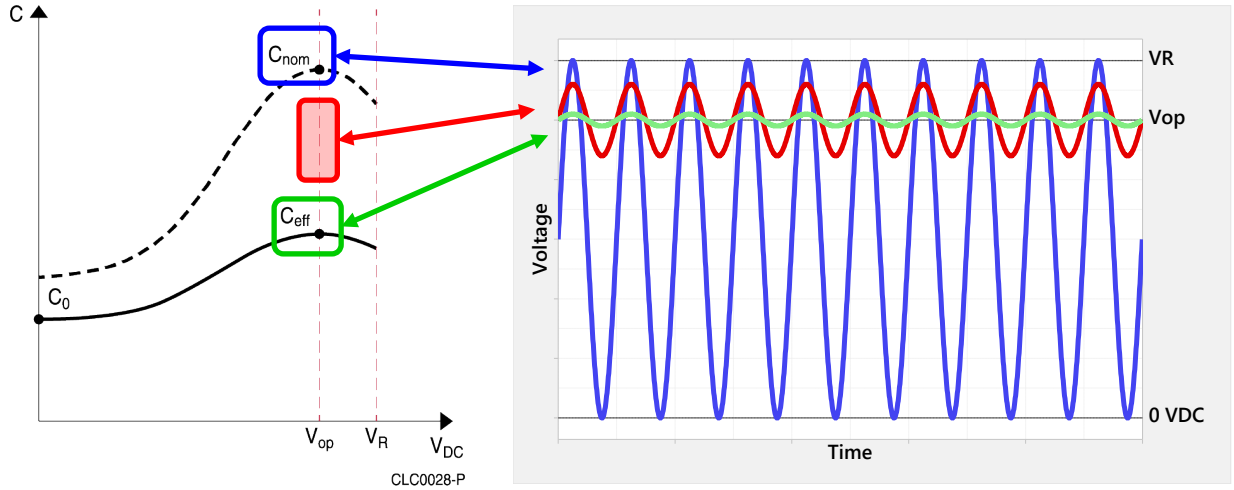


Figure 14: Small signal scenario (green), intermediate signal scenario (red) and large signal scenario (blue) for our calculation example.

From the capacitance graphs in the CeraLink LP 500 V data sheet (see also Figure 15), the effective capacitance at a DC bias of 350 V_{DC} and 25 °C is roughly 90%, i.e. 10% lower than at 400 V_{DC} (see green curve). However, from the capacitance increase due to temperature, we obtain 114% for the 85 °C case (orange curve) and 95% for 125°C case (red curve). By linear interpolation between these two values, we obtain for the 115 °C case roughly 109%, i.e. an increase of about +9% as compared to the C_{eff} value of 600 nF.

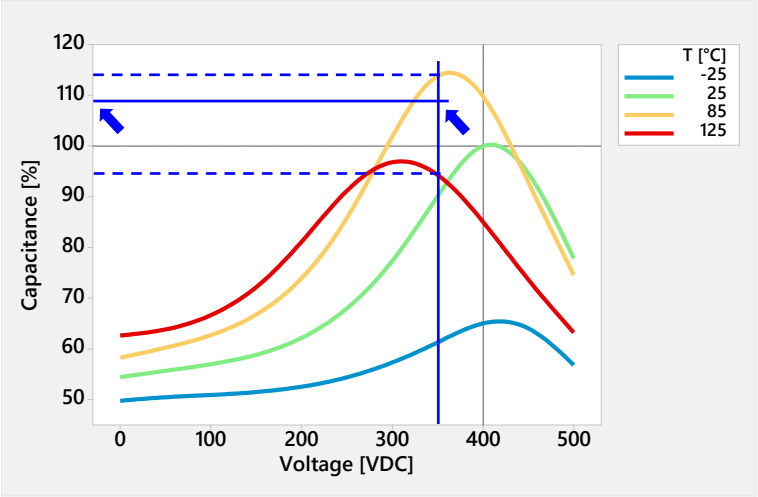


Figure 15: Capacitance values for these operating conditions.

As shown in Figure 13, the frequency dependence of the capacitance in this frequency region is approximately -2%. In total, the capacitance will change by about +7%. Therefore, the capacitance for the small signal scenario *1)*, for these operating conditions is about 640 nF. On the other hand, the capacitance for the intermediate signal scenario *2)*, for these application conditions will be around 700 nF, i.e. approximately 10% higher, whereas for scenario *3)* we would have roughly 750 nF, i.e. 17% higher as shown in Figure 16.

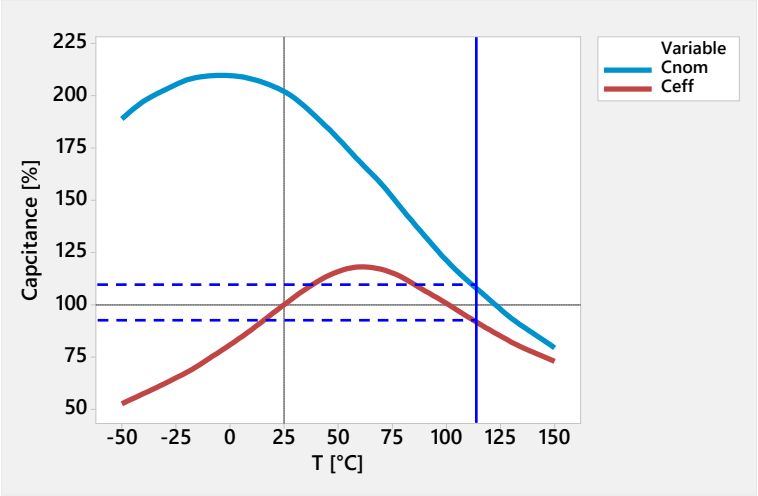
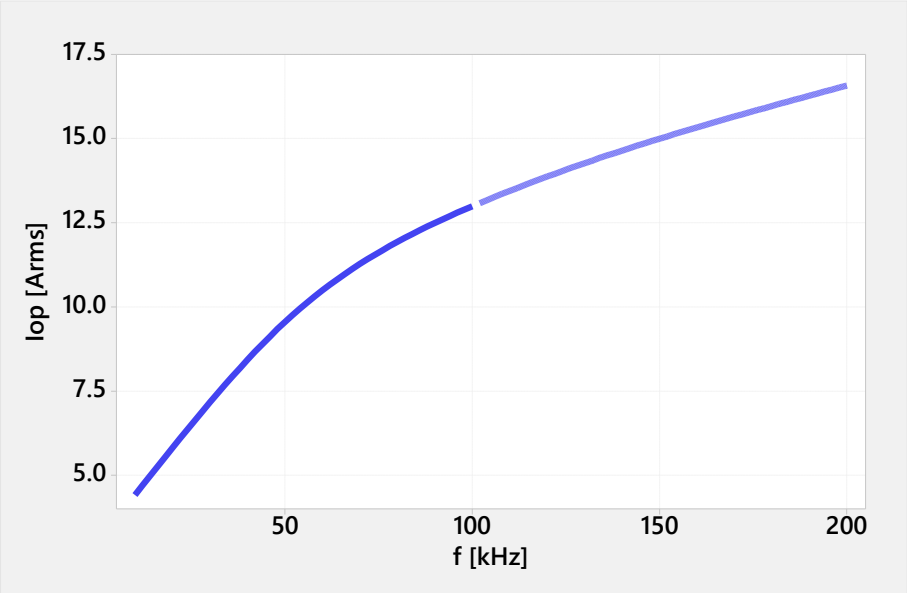


Figure 16: Difference between C_{eff} and C_{nom} for these operating conditions.

We note that this calculated example should provide only an idea about the non-linear aspects of CeraLink capacitors. For a more detailed analysis of certain application conditions, we refer to our simulation tools on our website: www.tdk-electronics.tdk.com

CURRENT CAPABILITY

CeraLink is optimized for operation at high frequency and temperature. The ESR, shown in Figure 10, decreases significantly for higher frequencies or at high temperatures. Therefore, the efficiency and thus the current capability of the device gets better when operated in this regime. This is also obvious from Figure 17 that shows the current capability of a CeraLink LP 500 V for different frequencies. Note that from 100 kHz to 200 kHz, the current capability can be increased by almost 30%.



$T_{ambient}$ = 105 °C

T_{device} = 150 °C

Capacitor is mounted on an aluminum heatsink with forced airflow. Experimental setup is detailed in footnote on the following page

Figure 17: Current capability of a CeraLink LP 500 V for different frequencies.

The current capability is measured using the setup shown in Figure 18.

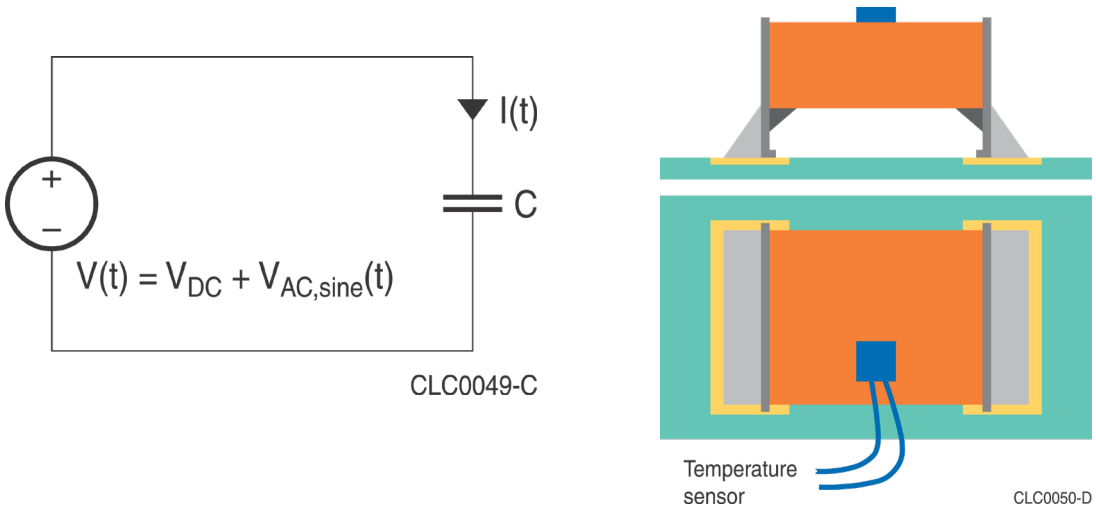


Figure 18: Schematic circuit for the current capability measurements. The device temperature is measured using a standard PT100 probe that is glued directly on the ceramics (note that for our SP types the probe is mounted on the housing)

Using a fixed DC bias voltage of V_{op}, the superimposed sinusoidal ripple voltage amplitude $V_{AC,\ sine}(t)$ is adjusted iteratively such that the current reaches the predefined fixed value, i.e. I_{RMS} is fixed. The temperature of the device is measured using a temperature sensor, which is attached to the top side of the ceramics.
In order to evaluate the current which leads to a device temperature of exactly 150 °C, three I_{RMS} values are chosen which lead to three different device temperatures (e.g. 134 °C, 148 °C and 161 °C). From these three current and temperature pairs, the exact current for T_{device} = 150 °C can be extracted via linear interpolation.

We note, that the main heat transfer of CeraLink happens through thermal conduction through the copper inner electrodes and the termination (lead frames) to the PCB. Only a fraction of the heat is dissipated through convection to the air. Therefore, a good cooling concept, i.e. the efficient mounting to a heatsink, is of paramount importance in order to maximize the current capability of the device.

Figure 19 shows this concept schematically. In the first scenario, the device is only mounted on a PCB without any further cooling (no heatsink and no forced airflow). This is the usual setting for our data sheet measurements, since it represents the worst-case condition. In the second scenario, the device is mounted on the same PCB, however, this time with an additional aluminum heatsink and forced airflow*. It can be seen that with cooling the current capability increases significantly, where the improvement at 10 kHz and 100 kHz is about 54% and 33%, respectively.

* Throughout this experiment, a standard 40 mm x 75 mm x 100 mm aluminum heatsink was used which offers a thermal resistance of roughly 1.2-1.4 K/W, where for safety reasons the heatsink was isolated from the PCB by a layer of Kapton® foil. The forced airflow is provided by the oven fan. It is important to note, that this example should provide only an idea about the importance of a proper cooling concept, where the current capability in real application might be different since it depends on various factors such as thermal conductivity through PCB, electrical/thermal isolation, heatsink, housing etc.

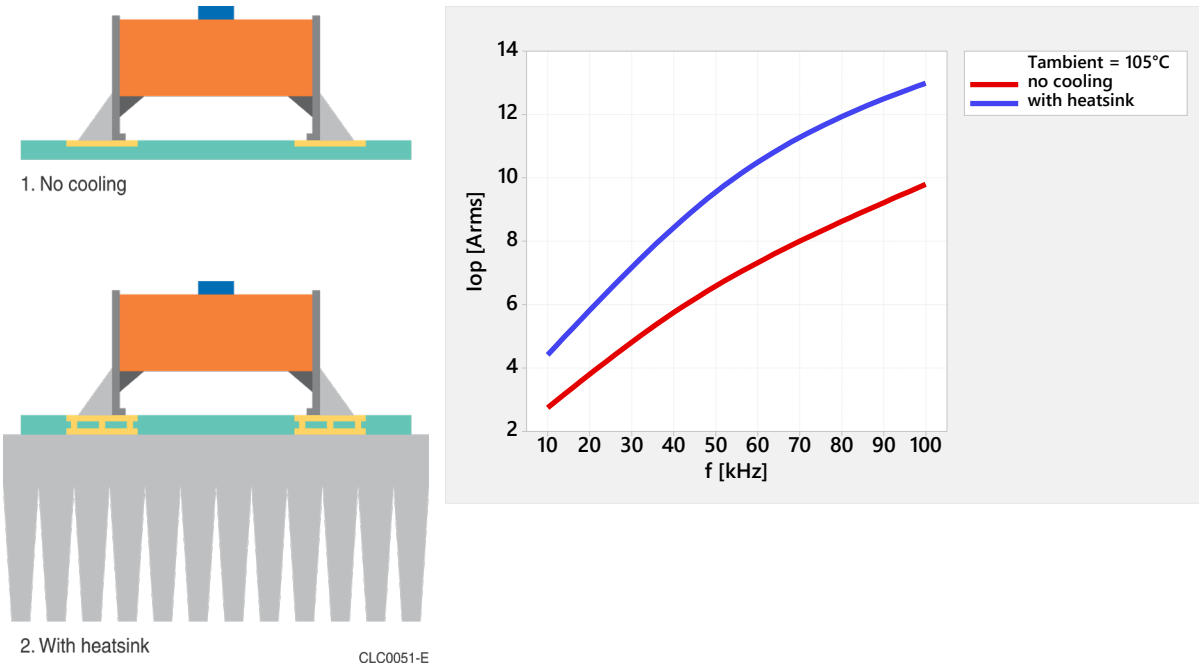


Figure 19: Current capability of CeraLink LP 500 V using two different cooling setups.

POLARIZATION

In contrast to other ceramic capacitors, most CeraLink capacitors (except CeraLink 2220 SMD components) are shipped with a defined polarity as marked on the case (see specification in data sheet). This chapter shall describe the reasons, why a polarity is defined and the proper usage for giving the user a feeling about what has to be considered in application. Furthermore, we emphasize again, that an operation under constant polarity change (AC) is not recommended due to significantly higher losses.

Note that the polarity marking is mainly for incoming inspection purposes since the components are usually unpoled anyway after reflow soldering due to temperature effects. If operated at normal DC-Link conditions, i.e. at voltage levels $\geq V_{op}$, the poling happens automatically during the first seconds after switching on the DC-Link voltage. However, if the components are operated below the specified operational voltage V_{op}, a first time poling is required to establish the full capacitance. The corresponding procedure and further background information shall be detailed in the following.

Because of its specific material features, CeraLink can be in poled, unpoled or reversely poled state or have a status somewhere in between. The polarity of CeraLink can be removed or changed in the opposite direction by application of voltage and/or temperature over time. So basically there are three methods to change or remove polarity of CeraLink:

VOLTAGE

Applying voltage causes poling of CeraLink in the applied voltage direction. If enough voltage is applied, the polarization state is fully developed. Note that an unpoled CeraLink has only around 60% of its initial capacitance. As shown in Figure 20, the required voltage V to fully pole CeraLink is in the range of 90% to 95% of the rated voltage V_R. Note that with operating voltage V_{op} the full polarity is usually not established (since $V_{op} < V_R$). This is particularly true for the 500 V types for which V_{op} is 400 V, i.e. only 80 % of the rated voltage, where for the 700 V and 900 V types the ratio is 86% and 89% respectively.

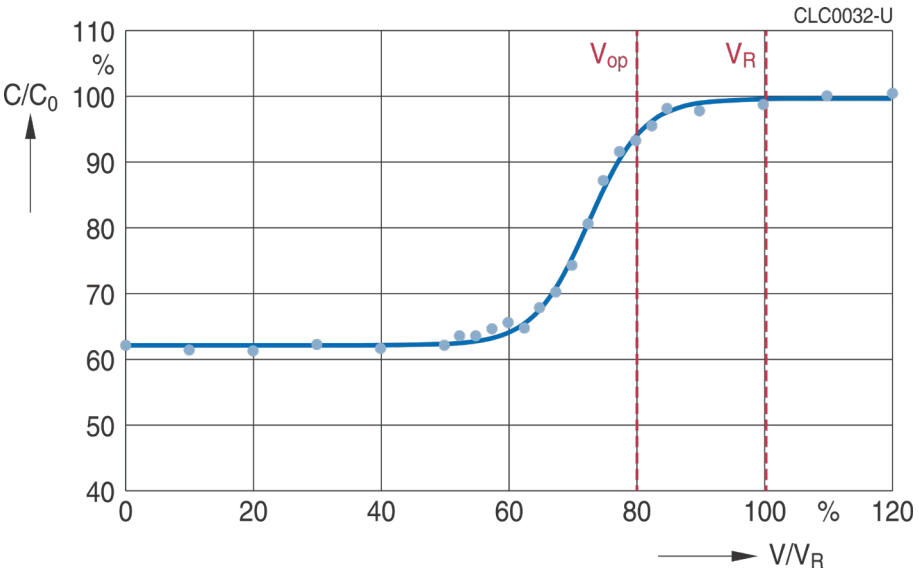


Figure 20: Required voltage to re-pole a CeraLink capacitor.

It is important to note, that the polarity can be fully reversed in the opposite direction, when sufficient negative bias is applied. In this case, the poling state changes independent of time, it only has to be ensured that the full negative voltage drop occurs at the capacitor. The measured capacitance in poling and in reverse poling direction is shown in Figure 21. Note that the difference in capacitance will be only visible at around operating voltage. For small electrical fields, there is no difference in capacitance, whereas at voltage levels close to rated voltage, the device gets basically poled during the measurement and the two curves have roughly the same endpoint.

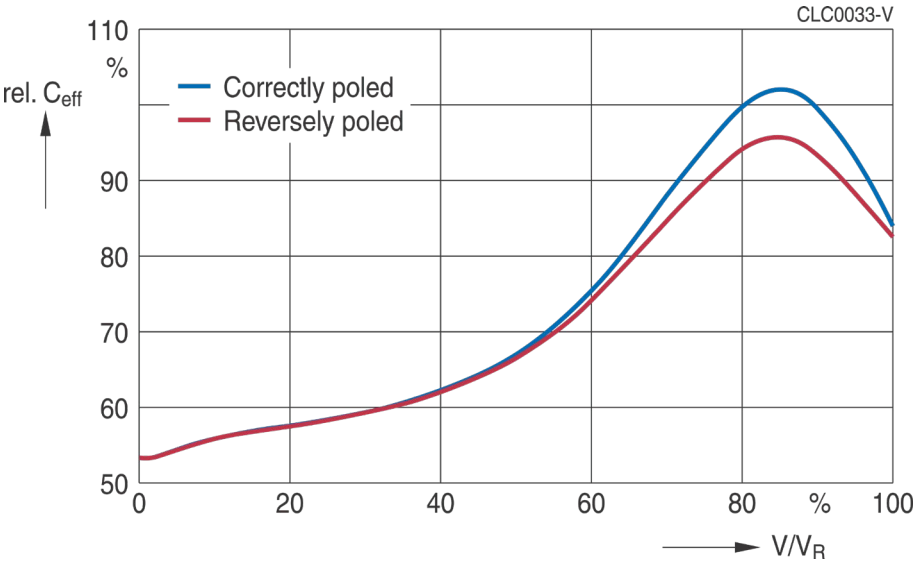


Figure 21: Measured capacitance in poling and in reverse poling direction.

DE-POLARIZATION OVER TIME

CeraLink partly loses polarity over time if no voltage is applied. Typical decay rates at room temperature are approximately 2.5% per decade. That means when capacitance is measured for example one hour after poling, the capacitance after 10 hours will be 97.5% of the initial value, after 100 hours it will be 95%.

DE-POLARIZATION OVER TEMPERATURE

The unpoling effect mentioned above can be accelerated if the device is exposed to temperature. In practical terms, this happens during reflow soldering. Application of typical reflow solder profiles with peak temperatures of approximately 240-260 °C and an overall duration in the range of several minutes will lead to partial unpoling of the CeraLink capacitor. Both effects (loosing polarity by time and/or temperature) can be totally recovered by applying rated voltage V_R (see section Voltage).

OVERVIEW

Measuring the small signal capacitance C_0 only allows one to determine the difference between the poled and unpoled states. Since there is no given direction in the measurement, the direction of polarity cannot be determined. By applying rated voltage, the part under test poles itself automatically to the given direction.

In Figure 22, the previously mentioned properties are highlighted schematically:

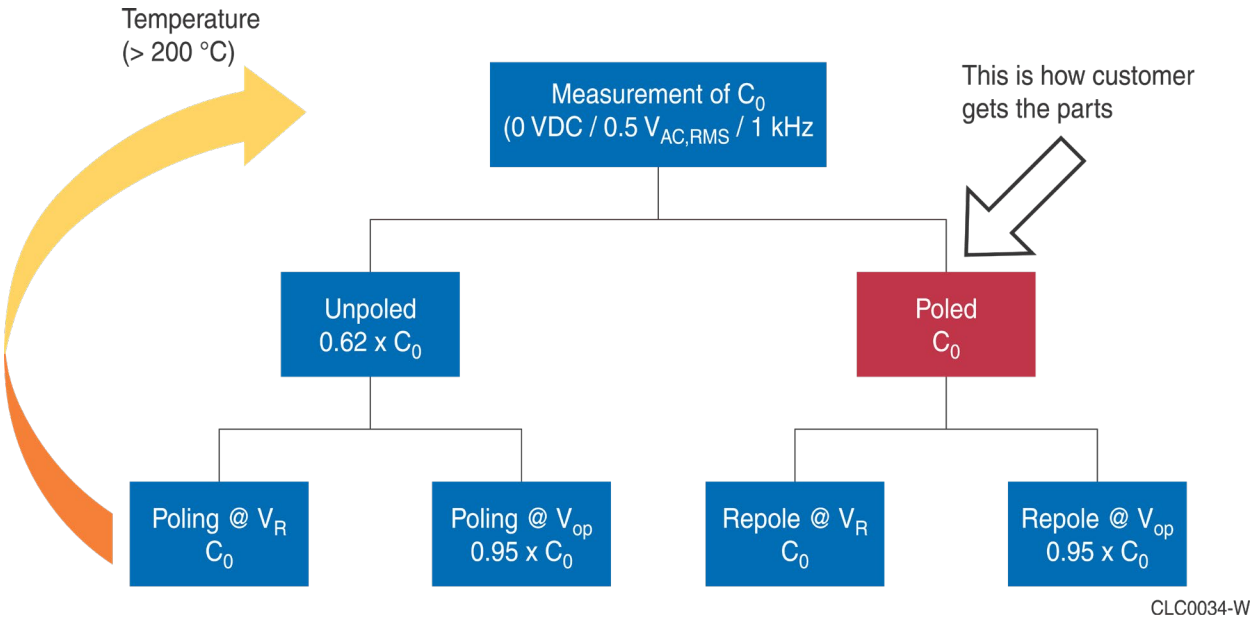


Figure 22: Schematic description of the relation between poling state and capacitance value for CeraLink

LIFETIME ESTIMATION

The lifetime of CeraLink mainly depends on the voltage level and the device temperature in the application. The lifetime acceleration parameters are determined by a Highly Accelerated Life Test (HALT). From a comparison of the Weibull-distributed end-of-life measurements at different voltage levels and temperatures, the lifetime at specific operating conditions can be assessed from an Arrhenius law of the following form:

$$t_{char,\ app} = \left(\frac{\alpha_{\text{voltage}}}{U_{app}}\right)^{3.4} \times \exp\left(\frac{9280}{T_{app}} - 19.6\right)$$

$t_{char,\ app}$ … characteristic lifetime in application (in hours)
$\alpha_{voltage}$ … pre-factor depending on the voltage class of the CeraLink
U_{app} … voltage level in application
T_{app} … temperature in application (in Kelvin)

The pre-factors $\alpha_{voltage}$ for the different voltage classes are given by *):

$$\alpha_{\text{voltage}} = \begin{cases} 4000\ for\ voltage\ class\ 500V\ (rated\ voltage) \\ 5600\ for\ voltage\ class\ 700V\ (rated\ voltage) \\ 7200\ for\ voltage\ class\ 900V\ (rated\ voltage) \end{cases}$$

*) the pre-factors and activation energies are based on experimental data and might be updated periodically

Furthermore, from the characteristic lifetime, the lifetime for a given failure rate $\tau(p)$ can be determined by using the steepness of the Weibull distribution obtained from the HALT measurements. It can be calculated from the following expression:

$$\tau(p) = t_{char,app} \times ln\left(\frac{1}{1-p}\right)^{0.435}$$

Where p is the user-defined cumulative failure amount (e.g. 0.1% or 100 ppm).

TDK notes that the experimental test boundary condition for no failure is the High Temperature Operational Life test (MIL-STD-202, method 108) at rated voltage and 150 °C for 1000 hours. Nevertheless, due to statistical nature of the failure mechanism, a zero failure rate within this time cannot be guaranteed.

CALCULATION EXAMPLE - CERALINK LP 500V 1µF

For the lifetime calculation, the operating temperature and voltage, experienced by the chip is important. Note that for the operating temperature it is irrelevant whether the chip is heated up due to electrical current flow or through the ambient temperature.

Throughout, three different operating temperatures and two different voltage levels are considered. In the following table, we give the characteristic lifetime in hours as well as the lifetime for 1% and 10 ppm failure rate. Note that after the characteristic lifetime, due to the assumed Weibull–type distribution, 63.2 % of the samples will statistically fail.

It is important to note that this example calculation provides only a rough assessment. For a more detailed estimation of the lifetime, a dedicated mission profile is required.

U_{op} \ T_{op}	100 °C	125 °C	150 °C
400 V	T_{char} = 440000 h $T_{1\%}$ = 60000 h T_{10ppm} = 2950 h	T_{char} = 93000 h $T_{1\%}$ = 12500 h T_{10ppm} = 620 h	T_{char} = 23400 h $T_{1\%}$ = 3160 h T_{10ppm} = 156 h
500 V	T_{char} = 207000 h $T_{1\%}$ = 28000 h T_{10ppm} = 1380 h	T_{char} = 43400 h $T_{1\%}$ = 5900 h T_{10ppm} = 290 h	T_{char} = 11000 h $T_{1\%}$ = 1500 h T_{10ppm} = 73 h

Table 2: Lifetime calculation CeraLink LP 500 V

FREQUENTLY ASKED QUESTIONS

HOW DO I DETECT IF CERALINK IS POLED OR UNPOLED?

Measure the small signal capacitance C_0 as described in the data sheet (usually done at 0 V_{DC}, 0.5 $V_{AC, RMS}$, 1 kHz). If C_0 is only 60% of the data sheet value, CeraLink is unpoled (note that this is the usual case after reflow soldering).

CERALINK SEEMS TO BE PARTLY POLED/UNPOLED (E.G. AFTER REFLOW SOLDERING). HOW SHALL I PROCEED?

During operation, i.e. when DC bias voltage ≥ V_{op} is applied, CeraLink gets poled. If you want to make sure to have a fully poled component before operation, apply rated voltage V_R to the component. This is of particular importance in cases when the capacitor is not operated constantly, e.g. in protection circuits. In this case, the application of a voltage pulse after reflow is highly recommended in order to ensure a fully poled device in case of failure.

IF CERALINK IS POLED, HOW DO I DETECT THE POLING DIRECTION?

The only possible way to detect the direction of polarity of a CeraLink is by measuring the effective capacitance C_{eff}, i.e. performing the C_0 measurement with DC bias (note that C_{eff} is defined as C_0 at operating voltage V_{op}). In this case, a slightly smaller capacitance value would be measured on a reversely poled CeraLink, see Figure 20. This effect is most prominent for the 500 V type and less distinctive for the higher voltage classes (see previous statement). In general, the easier solution is to reset the polarity by applying rated voltage V_R.

WHAT HAPPENS IF A CERALINK CAPACITOR IS MOUNTED IN THE WRONG POLARITY DIRECTION?

a) If **V_R** is applied, the capacitor is re-poled during first switching on and no further action is needed.
b) If **V_{op}** is applied in application, two scenarios have to be considered:
    a. **V_{op} with a small superimposed** ripple voltage (small signal): the capacitor will be poled to a level of ≥ 95%, i.e. there will be a capacitance loss of ≤ 5%.
    b. **V_{op} with a large superimposed** ripple voltage (large signal): the additional ripple amplitude is usually enough to fully pole CeraLink.
c) If **<V_{op}** is applied in application, mounting CeraLink capacitor in pre-defined polarity is recommended. Note that after reflow soldering and/or time exposure, CeraLink is partly unpoled (see chapter >Polarization<).

WHERE CAN I SEE POLARITY MARKING?

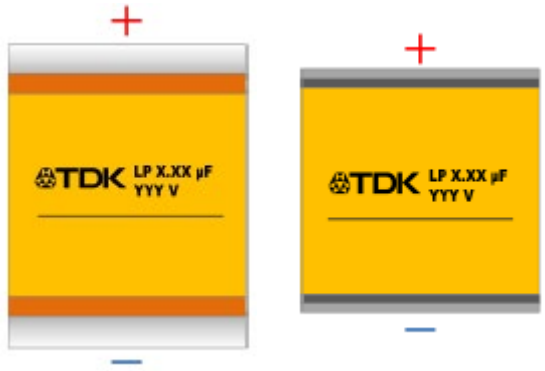


Figure 23: Polarity marking of CeraLink LP

Description on polarity marking is mentioned in the respective data sheet after dimensional drawing and solder pad recommendation. As an example, Figure 23 shows polarity marking of CeraLink LP version.

Note that polarity is only for incoming inspection purposes and it does not affect operation. If put under reverse rated voltage V_R, CeraLink is repoled and works identically. Note furthermore, that CeraLink 2220 components do not have polarity marking at all (due to the aforementioned reasons).

YOU MENTION THERE IS NO LIMITATION ON DV/DT. HOW IS THIS TO BE UNDERSTOOD IN REGARDS TO VOLTAGE OR CURRENT PEAKS IN THE MILLISECONDS RANGE?

The dV/dt ratio is limited only by the intrinsic ESR of the capacitor, where the time constant is given by $\tau = ESR \cdot C$. It is difficult to give a general value for τ since the ESR of CeraLink is a non-linear quantity and depends on frequency and temperature. However, for typical application conditions, the time constant will be in the nanoseconds range, i.e. well below the microseconds range.

Furthermore, we note that there is no limit on di/dt in principle, i.e. short peak current pulses are basically limited only by two factors *1)* the overall induced voltage (e.g. from stray inductance or large inductive loads) on the capacitor must stay below $V_{pk,\,max}$ and *2)* the induced device temperature stays within the rated limits.

WHAT DO I HAVE TO CONSIDER IN REGARDS TO CREEPAGE AND CLEARANCE DISTANCE?

CeraLink ceramic features a CTI ≥ 600, and therefore fulfills the requirements on creepage and clearance distance according to DIN EN 60664-1 for degree of contamination 1 or 2 for all voltage types:

	Degree of Contamination		
CeraLink V classes	**1**	**2**	**3**
500 V	Yes	Yes	No
700 V	Yes	Yes	No
900 V	Yes	Yes	No

Table 3: Creepage distance requirements for contamination class 1 & 2 are fulfilled for all voltage types.

WHICH SOLDERING PROCESSES ARE APPLICABLE FOR CERALINK?

CeraLink Series	Reflow soldering*	Wave soldering	Vapor phase soldering
LP, FA	Recommended	Not recommended	Please consult TDK
SP	Recommended	Recommended	Please consult TDK
2220	Recommended	Not recommended	Please consult TDK

Table 4: Soldering processes

* Reflow soldering profiles according to IEC 60068-2-58 recommendations. For details, please check the respective product data sheet. The usage of lead-free solder types is recommended.

IS CERALINK USING THE CLASSICAL MLCC DESIGN?

The CeraLink ceramic chip (LP, FA & SP) features a multilayer serial connection (MLSC) design, i.e. a series connection of two MLCC geometries in one component as shown in Figure 24. This design offers additional safety properties as compared to standard MLCC and can reduce the risk of short circuits caused by cracks (e.g. from mechanical overstress). A drawback of this design is the decreased capacitance density as compared to MLCC. Note that CeraLink 2220 components feature the classical MLCC design. In this case, short circuit / crack prevention is realized via soft termination.

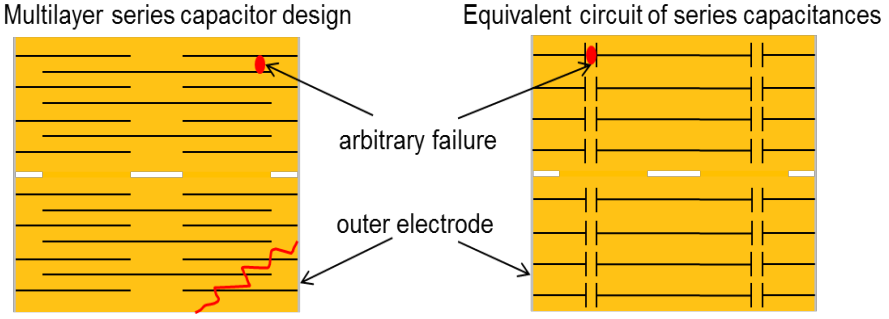


Figure 24: MLSC design of CeraLink standard chip (LP, FA & SP)

WHY CAN CERALINK HANDLE SO MUCH CURRENT?

CeraLink chips feature copper inner electrodes, which provide not only excellent electrical conductance and low losses but also outstanding thermal properties, i.e. the heat produced inside the chip is transported to the outer contacts (leadframes) and subsequently to the PCB very efficiently. The connection between CeraLink ceramic body and outer contacts is a sintered layer of silver, where the outer contacts are made of CIC (copper-invar-copper), which combines highest electrical and thermal conductivity with low coefficient of thermal expansion (CTE). Furthermore, the CTE is matched to the ceramic such that thermo-mechanical stress of the whole system is minimized.

In conclusion, all employed materials provide excellent thermal and electrical conductivity (lowest thermal and electrical resistance) allowing to transfer the component heat efficiently through the lead frames to the PCB. This is especially the case for CeraLink LP and FA series. However, it is important to have a good cooling concept for the current handling as shown in chapter >Current Capability<. Note that all data sheet values are based upon worst-case scenarios (mounting on standard FR4, no heatsink, no active airflow).

HOW MUCH LEAD (PB) CONTAINS CERALINK?

CeraLink ceramic chip contains roughly 60 wt% of lead in a covalent / ionic bond.
Further details on the material composition are available in the material data sheet on our website: www.tdk-electronics.tdk.com

GLOSSARY

SYMBOLS	TERMS
AC	Alternating current
C_0	Initial capacitance @ 0 V_{DC}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature
C_{eff} ($C_{eff, typ}$)	Typical effective capacitance @ V_{op}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature
C_{nom} ($C_{nom, typ}$)	Typical nominal capacitance @ V_{op}, quasistatic, room temperature
CTE	Coefficient of thermal expansion
CTI	Comparative tracking index
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
FA	Flex assembly
f_{ripple}	Frequency of the operation ripple current
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
LP	Low profile
MLCC	Multilayer ceramic capacitor
MLSC	Multilayer serial capacitor
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
ppm	Parts per million
R_{ins}	Insulation resistance @ V_{pk}, measurement time t = 7 s, room temperature
SP	Solder pin
T_{amb}	Ambient temperature
tan δ	Dissipation factor @ 0 V_{DC}, 0.5 $V_{AC, RMS}$, 1 kHz, room temperature
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current)
V_{op}	Operating voltage
V_R	Rated voltage
$V_{AC, RMS}$	Root mean square value of sinusoidal AC voltage
$V_{pk, max}$	Maximum peak operating voltage
ΔT	Increase of temperature during operation

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