

# EVAL-1ED32xxMC12H user guide

## Single channel, isolated, two-level, slew-rate control gate driver IC (2L-SRC)

1ED3241MC12H, 1ED3251MC12H

### About this document

#### Scope and purpose

The gate driver evaluation boards EVAL-1ED3241MC12H and EVAL-1ED3251MC12H feature the two-level, slew-rate control (2L-SRC) gate driver ICs 1ED3241MC12H and 1ED3251MC12H. This user guide demonstrates the functionality and key features of the Infineon EiceDRIVER™ 2L-SRC gate driver ICs.

The gate driver ICs are certified according to UL 1577 and VDE 0884-11.

The design of the evaluation board EVAL-1ED32x1MC12H was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full range of ambient operating conditions. The boards provided by Infineon are not subject to full production tests.

Evaluation boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD). Evaluation boards are intended to be used under laboratory conditions and by trained specialists only.

#### Intended audience

- Engineers who want to learn how to use the Infineon EiceDRIVER™ 1ED3241MC12H and 1ED3251MC12H
- Experienced design engineers who design circuits with Infineon EiceDRIVER™, IGBT and CoolSiC™ MOSFET
- Design engineers who develop power electronic devices, such as inverters

#### Evaluation Board

This board will be used during design in, for evaluation and measurement of characteristics, and proof of data sheet specifications.

*Note: PCB and auxiliary circuits are NOT optimized for final customer design.*

### Important notice

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### Safety precautions

### Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

**Table 1** Safety precautions

|   |  |
|---|--|
|    | <p><b>Warning:</b> The DC link potential of this board is up to 600 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.</p>   |
|    | <p><b>Warning:</b> The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.</p>                                |
|    | <p><b>Caution:</b> The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.</p>   |
|   | <p><b>Caution:</b> Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.</p>   |
|  | <p><b>Caution:</b> The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.</p> |
|  | <p><b>Caution:</b> The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.</p>   |

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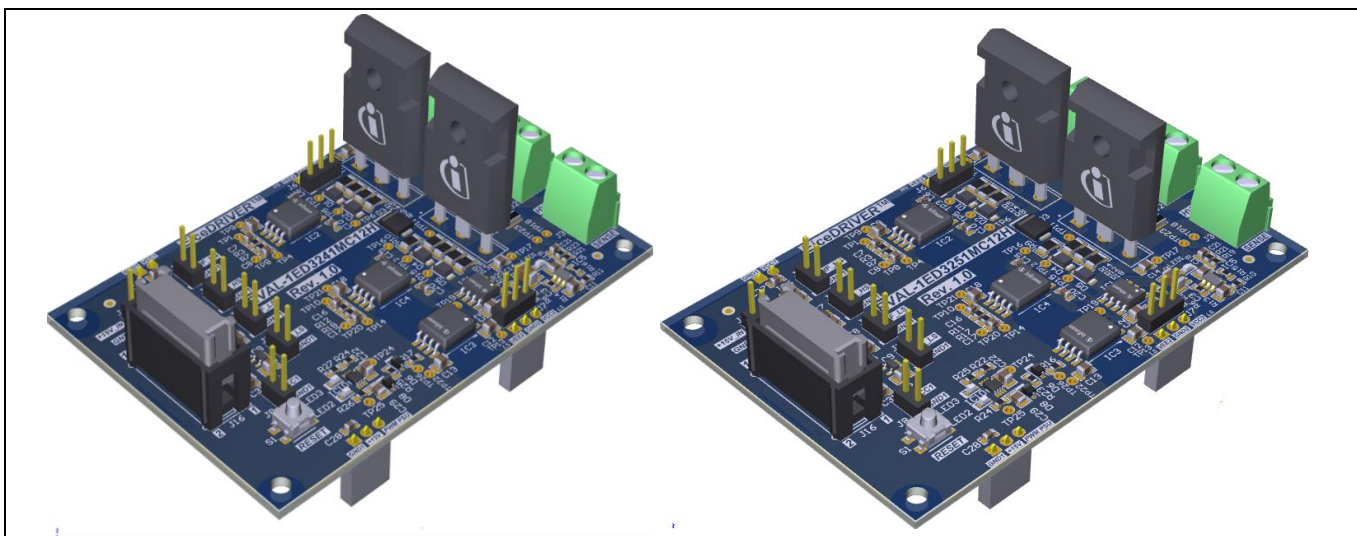
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### The board at a glance

## 1 The board at a glance

This user guide (UG-2021-25) describes the evaluation board EVAL-1ED32x1MC12H that is intended for the product feature evaluation of the Infineon EiceDRIVER Compact 1ED32x1MC12H in an application circuit. The key elements of the board and the product are listed here.

- Evaluation board in half-bridge configuration with two gate driver ICs to drive power switches such as IGBTs, silicon MOSFETs and silicon-carbide (SiC) MOSFETs
- Additional driver IC for ultra-fast, isolated, overcurrent feedback signaling from the high-voltage domain to the logic control domain
- Fast operational amplifier and comparator for ultra-fast overcurrent detection



**Figure 1** Evalboard EVAL-1ED3241MC12H (left) and EVAL-1ED3251MC12H (right)

This board is best suited for double-pulse testing. An additional high-voltage DC blocking capacitor at the high-voltage supply is mandatory. The capacitor has to be placed as close as possible to the high-voltage supply connectors. It requires additional considerations on thermal and power balance for continuous operation.

The control interface can be connected to a pulse generator, a microcontroller or other digital circuits.

For safe operation, a fast overcurrent detection and protection circuit is implemented with a galvanically isolated feedback path to the low-voltage input-side. The input-side flip-flop latches the overcurrent event information. This circuit will report the fault and turn off both gate driver ICs. The S1 button, also labeled with RESET, clears the flip-flop to enable the gate driver ICs again.

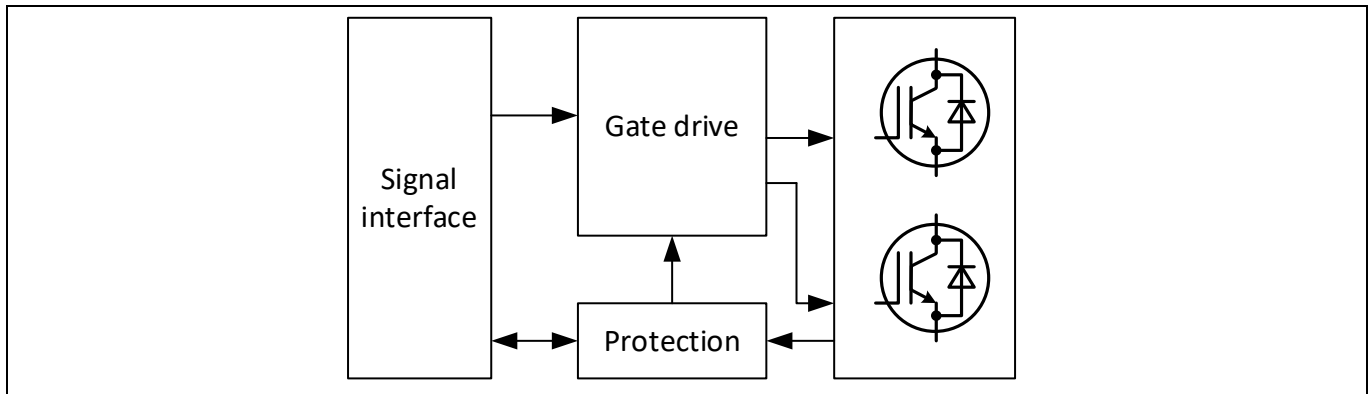
### 1.1 Delivery content

The evaluation board EVAL-1ED3241MC12H contains the printed circuit board. This board is designed to feature the 2L-SRC function for turn-on and turn-off. The assembled gate resistors are selected for use with IKQ75N120CT2 and with gate supply of 0 - +15 V. However, the power transistors are not assembled.

The evaluation board EVAL-1ED3251MC12H contains the printed circuit board. This board is designed to feature the 2L-SRC function for turn-on only. The assembled gate resistors are selected for use with IKQ75N120CT2 and with gate supply of 0 - +15 V. However, the power transistors are not assembled.

### The board at a glance

## 1.2 Block diagram



**Figure 2** Block diagram of EVAL-1ED32xxMC12H

## 1.3 Board parameters and technical data

The selected components on the evaluation boards, as well as the gate driver ICs, have maximum ratings and operating conditions to avoid damaging the individual parts and the evaluation board overall.

**Table 2** Absolute maximum ratings

| Pin/parameter name | Connector                | Min  | Max        | Unit    | Note  |
|--------------------|--------------------------|------|------------|---------|---|
| +15V_IN            | J15.2                    | -0.2 | 20<br>100  | V<br>mA | Input, if J16.10 is not connected; support supply voltage   |
| +15V               | J16.10                   | -0.2 | 20<br>100  | V<br>mA | Support supply voltage; input, if J15 is not connected; otherwise can be output                                   |
| INF_HS1, INF_LS1   | J16.1, J16.2             | -0.2 | VCC1 + 0.2 | V       | Input, digital signal   |
| VCC1               | J16.3                    | -0.2 | 5.3        | V       | Input, gate driver IC supply voltage  |
| RST                | J16.5                    | -0.2 | VCC1 + 0.2 | V       | Input, digital signal   |
| FAULT              | J16.6                    | -0.2 | VCC1 + 0.2 | V       | Open drain output, digital signal   |
| IN_HS1, IN_LS1     | J16.7, J16.8             | -0.2 | VCC1 + 0.2 | V       | Input, digital signal   |
| VCC2_HS, VCC2_LS   | J6.3, J7.3, J11.3, J12.3 | -0.2 | 35         | V       | Overall isolated secondary supply with reference to VEE2_HS/VEE2_LS   |
| VCC2_HS, VCC2_LS   | J6.3, J7.3, J11.3, J12.3 | -0.2 | 20         | V       | Positive secondary supply voltage with reference to GND2_HS/GND2_LS   |
| VEE2_HS, VEE2_LS   | J6.2, J7.2, J11.2, J12.3 | -15  | 0.2        | V       | Gate reference supply pin with reference to GND2_HS/GND2_LS   |
| V-HV               | J1                       | -0.2 | 800        | V       | Input, high-voltage supply, for voltages above 42 V, special high-voltage lab environment is strongly recommended |

### The board at a glance

| Pin/parameter name | Connector | Min | Max | Unit          | Note  |
|--------------------|-----------|-----|-----|---------------|---|
| Phase peak current | J2        | 150 | 150 | A             | Phase peak current for double-pulse tests   |
| $t_{\text{pulse}}$ |           | -   | 100 | $\mu\text{s}$ | Maximum ON pulse length for double-pulse tests  |
| $f_{\text{sw}}$    |           | -   | 100 | kHz           | Maximum switching frequency for continuous operation, careful consideration of power dissipation required for power transistor and EiceDRIVER™ IC |

The PCB assembly is optimized for a VCC1 supply voltage of 3.3 V. Higher supply voltages may require adjustments to the current limiting resistors of the status LEDs.

**Table 3 Operating conditions and supply voltages**

| Pin name         | Min. | Typ. | Max.     | Unit | Note  |
|------------------|------|------|----------|------|---|
| +15V_IN          | 15.5 | 16   | 16.5     | V    | Input, if J16.10 is not connected; support supply voltage   |
| +15V             | 15.5 | 16   | 16.5     | V    | Support supply voltage; input, if J15 is not connected; otherwise can be output   |
| VCC1             | 3.2  | 3.3  | 3.4      | V    | Input, gate driver IC supply voltage  |
| FAULT            | -0.1 | 3.3  | VCC1+0.1 | V    | Output, digital signal  |
| RST              | -0.1 | 3.3  | VCC1+0.1 | V    | Input, digital signal   |
| IN_HS            | -0.1 | 3.3  | VCC1+0.1 | V    | Input, digital signal   |
| IN_LS            | -0.1 | 3.3  | VCC1+0.1 | V    | Input, digital signal   |
| VCC2_HS,VCC2_LS  | 12   | 15   | 20       | V    | Overall isolated secondary supply with reference to GND2_HS/GND2_LS   |
| VEE2_HS, VEE2_LS | 0    | -    | -15      | V    | Gate reference supply pin with reference to GND2_HS/GND2_LS   |
| V-HV             | 25   | 600  | 800      | V    | Input, high-voltage supply, referenced to HV_GND; for voltages above 42 V, special high-voltage lab environment is strongly recommended |

Please note that the current into the supply terminals depends strongly on the operating conditions, such as the switching frequency or the selected power transistor.



## 2 System and functional description

### 2.1 Commissioning

Follow the steps below to set up and power up the board, and to perform first evaluations.

#### Prerequisites

- Assemble fitting power switches at the location Q1 and Q2, e.g. IKQ75N120CT2 IGBTs
- Assemble an external high-voltage DC capacitor (>330  $\mu$ F) between *J1-1/2 (V-HV)* and *J3-2 (HV\_GND)*, ensuring low stray inductance
- Have low-voltage power supplies ready for input support and logic supply (+15V\_IN, VCC1) with a current capability of at least 100 mA for +15V\_IN and 20 mA for VCC1
- Have isolated low-voltage power sources ready for the gate drivers' output supply (VCC2\_HS - GND2\_HS, GND2\_HS - VEE2\_HS, VCC2\_LS - GND2\_LS, and GND2\_LS - VEE2\_LS). Each supply requires a current capability of 100 mA.
- Have a high-voltage power supply ready for HV-DC between *J1-1/2 (V-HV)* and *J3-2 (HV\_GND)*
- Have an inductive load ready for double-pulse tests, e.g. 600  $\mu$ H
- Have a dual channel PWM generator ready for half bridge PWM input

To adapt the circuit to application requirements, resistor or capacitor values can be changed to optimize the performance.

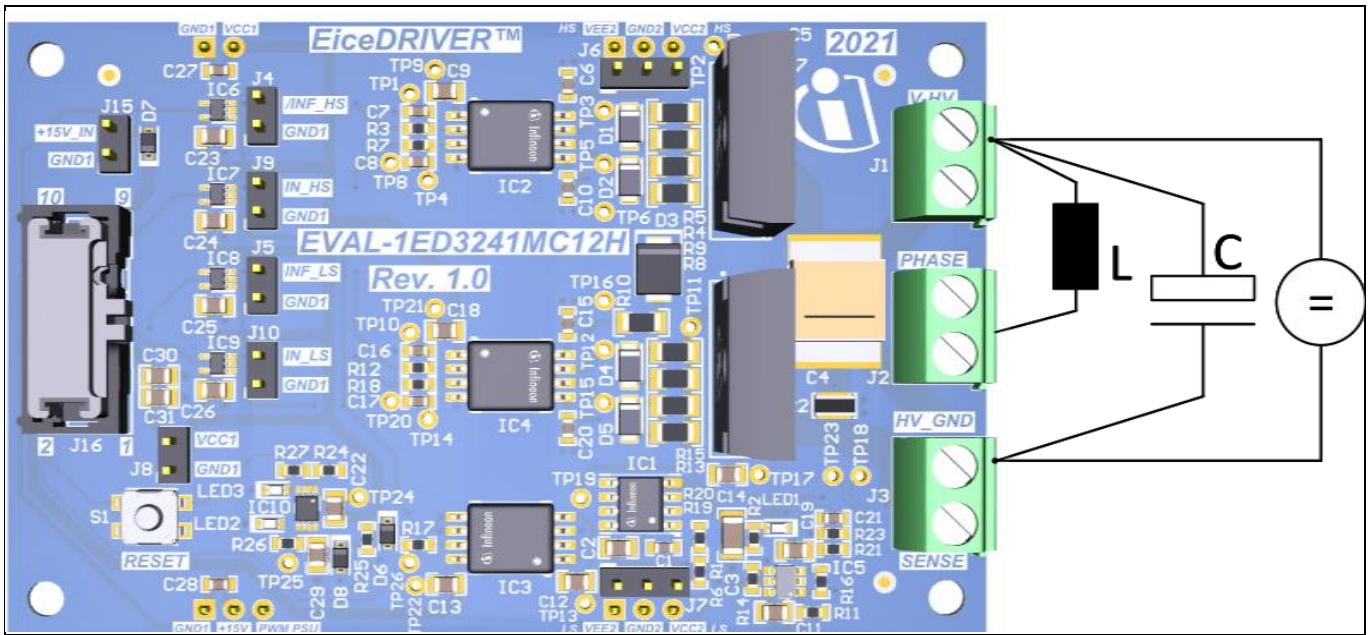
#### Power-up sequence

1. Connect supply GND to connector *J15.1* and supply +15V\_IN to connector *J15.2* with +16 V.
2. Connect supply GND to connector *J8.1* and supply VCC1 to connector *J8.2* with +3.3 V.
3. The red LED3 will turn on.
4. Supply both secondary gate driver supplies with individual power sources at VCC2\_HS - GND2\_HS, and GND2\_HS - VEE2\_HS at connector *J6*, and VCC2\_LS - GND2\_LS and GND2\_LS - VEE2\_LS at connector *J7* according to the assembled power switch needs.
5. The green LED1 will turn on.
6. Connect the digital PWM generator to the digital interface connectors *J16.7* and *J16.8* labeled with IN\_HS1 and GND as well as IN\_LS1 and GND. Make sure that the outputs of the PWM generator are disabled, or the signals are on low.
7. Connect the high-voltage supply to connector *J1.1* or *J1.2* and HV\_GND to *J3.2*.
8. Connect one end of the inductive load to *J2.1* and the other end according to the double-pulse requirements to either *J1.1* or *J3.1* (low-side or high-side testing).
9. Push S1 to reset the error flip-flop.
10. The red LED3 will turn off and green LED2 will turn on.
11. The board is now ready for double-pulse evaluation.

#### Safe power-down sequence

1. Turn-off the DC-link voltage source and discharge the DC-link capacitor.
2. Check the DC-link voltage with e.g. a digital multimeter or an oscilloscope.
3. Turn-off the other supply voltages (VCC2, VEE2, +15\_IN, VCC1).





**Figure 3 Connection of load for double-pulse tests**

## 2.2 Overcurrent protection

The detection circuit measures the voltage across shunt resistor R22. This signal passes a RC filter R21 and C19 and comparator U5 compares it to a reference voltage. The reference voltage is defined by the voltage divider R14 and R23. The trip value is at approximately 96 A, and can be adapted to application requirements by changing the shunt resistor R22 and/or adapting the reference voltage divider R14 and R23.

The output signal is transferred with coupler U3 to the low-voltage domain to trigger the flip-flop and store the overcurrent event. Once the flip-flop is triggered, the input signals of the logic AND gates U6 - U9 are low. This turns off both IGBTs via the *OUT* terminal of the ICs U2 and U4. Thus the IGBTs are turned off in the slow mode in case of EVAL-1ED3241MC12H. This can be compared to the soft turn-off function of gate drivers, which contain an integrated short-circuit detection. In addition, it reports the overcurrent event to the digital interface connector as a *FAULT* signal and turns the LED7 on.

EVAL-1ED3251MC12H does not contain the slow turn-off feature.

To return to normal operation, S1 needs to be pushed to reset the flip-flop. As feedback, LED7 turns off and LED6 turns back on again.

## 2.3 Preparation for positive gate supply (0 – +15 V)

The board can be operated with output supply voltage of 0 - +15 V, too. Please apply a jumper on pins J6.1 and J6.2. Furthermore, a jumper has to be applied on pins J7.1 and J7.2. Then, the output-side supply voltage can be connected to pins J6.2, J6.3 and to pins J7.2 and J7.3, respectively.

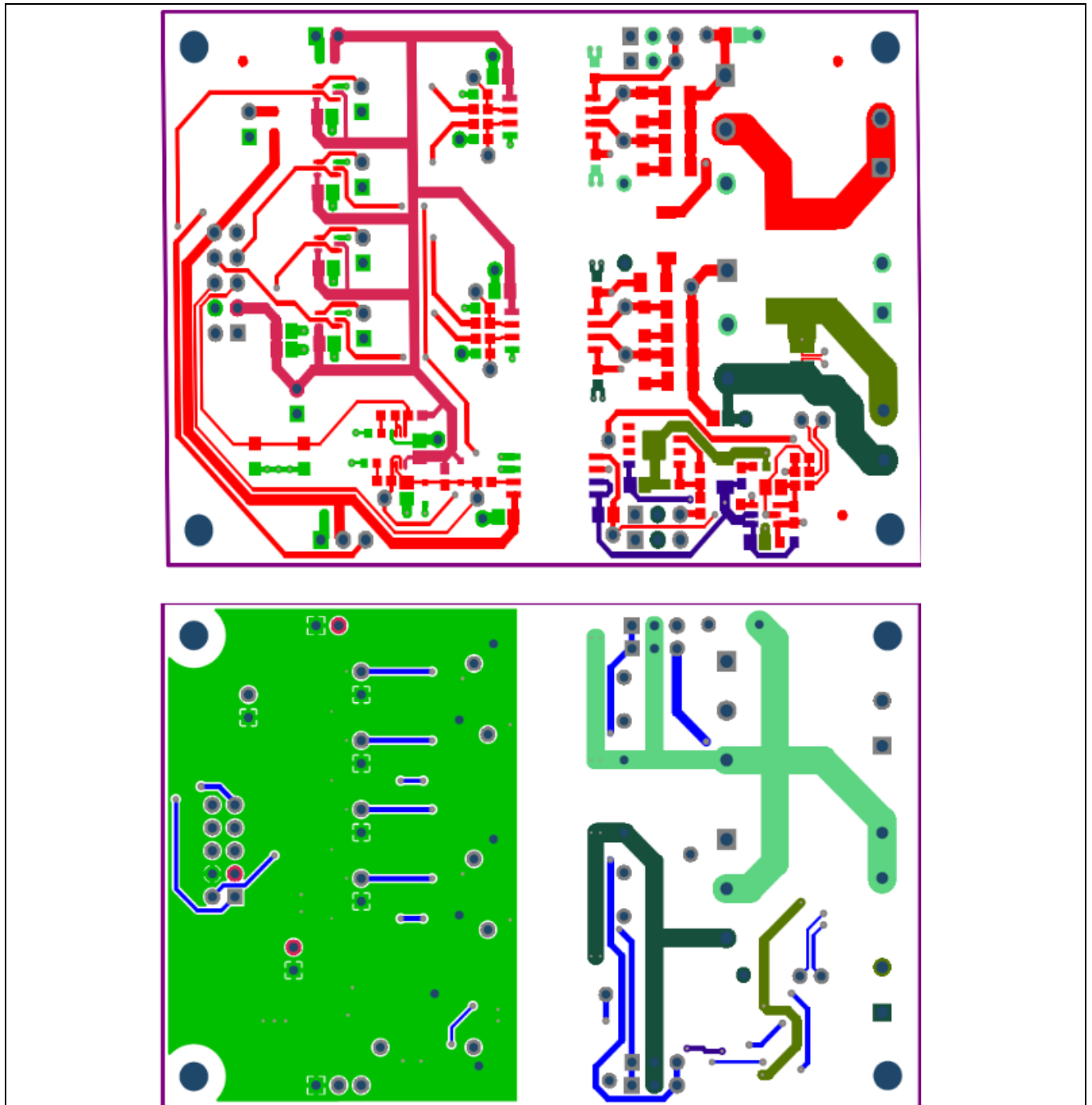
**System design**

**3 System design**

**3.1 Schematics**

The complete schematics are available on the download section of the Infineon homepage. A log-in is required to download this material.

**3.2 Layout**



**Figure 4 Top and bottom layer of Eval-1ED3241MC12H**

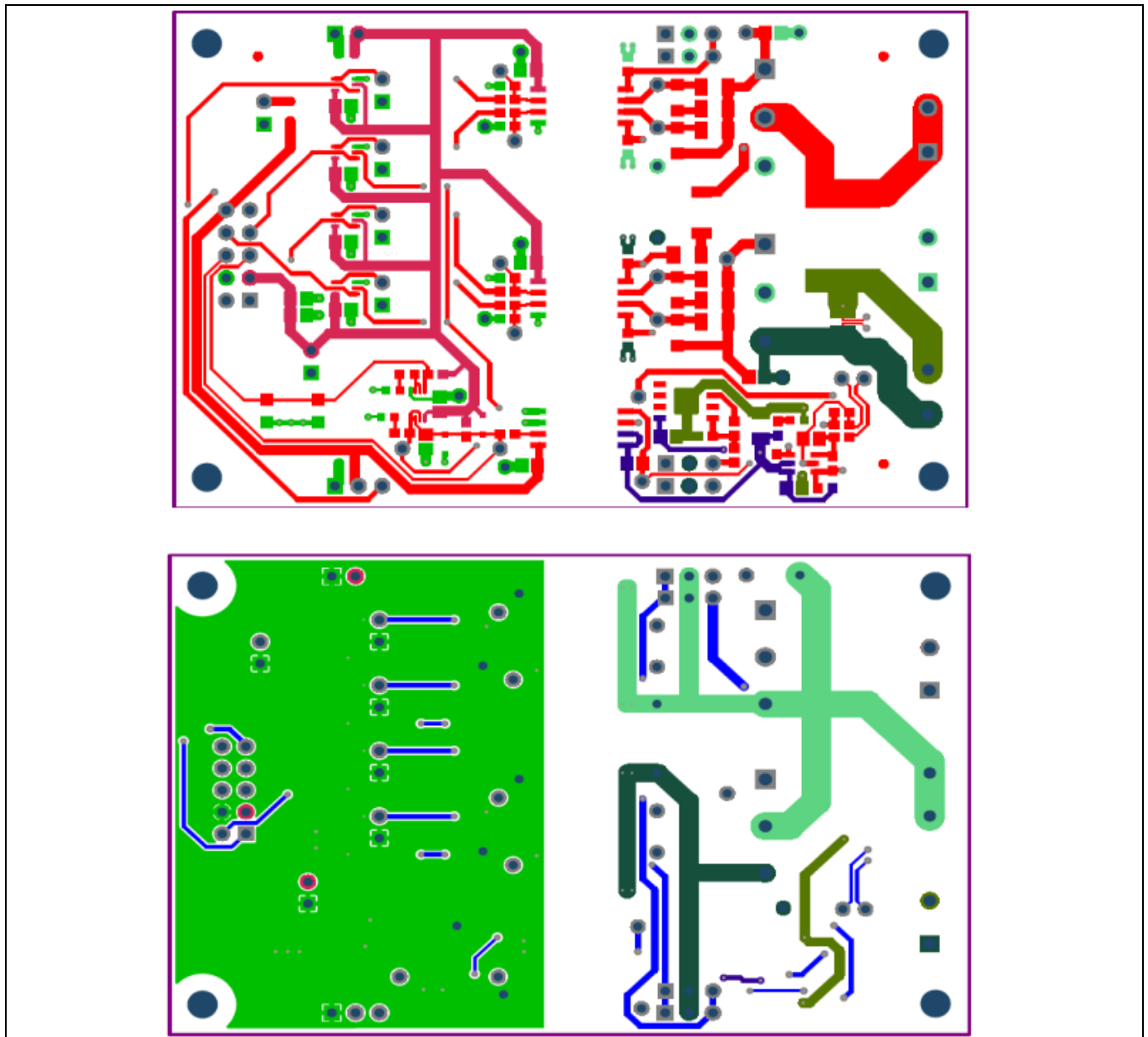


Figure 5 Top and bottom layout of Eval-1ED3251MC12H

### 3.3 Bill of material

The complete bill of material is available on the download section of the Infineon homepage. A log-in is required to download this material.

Table 4 BOM of the most important/critical parts of the evaluation or reference board

| S. No. | Ref Designator | Description                                  | Manufacturer   | Manufacturer P/N |
|--------|----------------|--|----------------|------------------|
| 1      | C4             | CAP, CERM,<br>0.25uF, 900V, 20%,<br>CeraLink | TDK            | B58031I9254M062  |
| 1      | R20            | RES, 0R001, 5%,<br>1W, 0612                  | Isabellenhütte | VLK-R001-5.0     |

### 3.4 Connector details

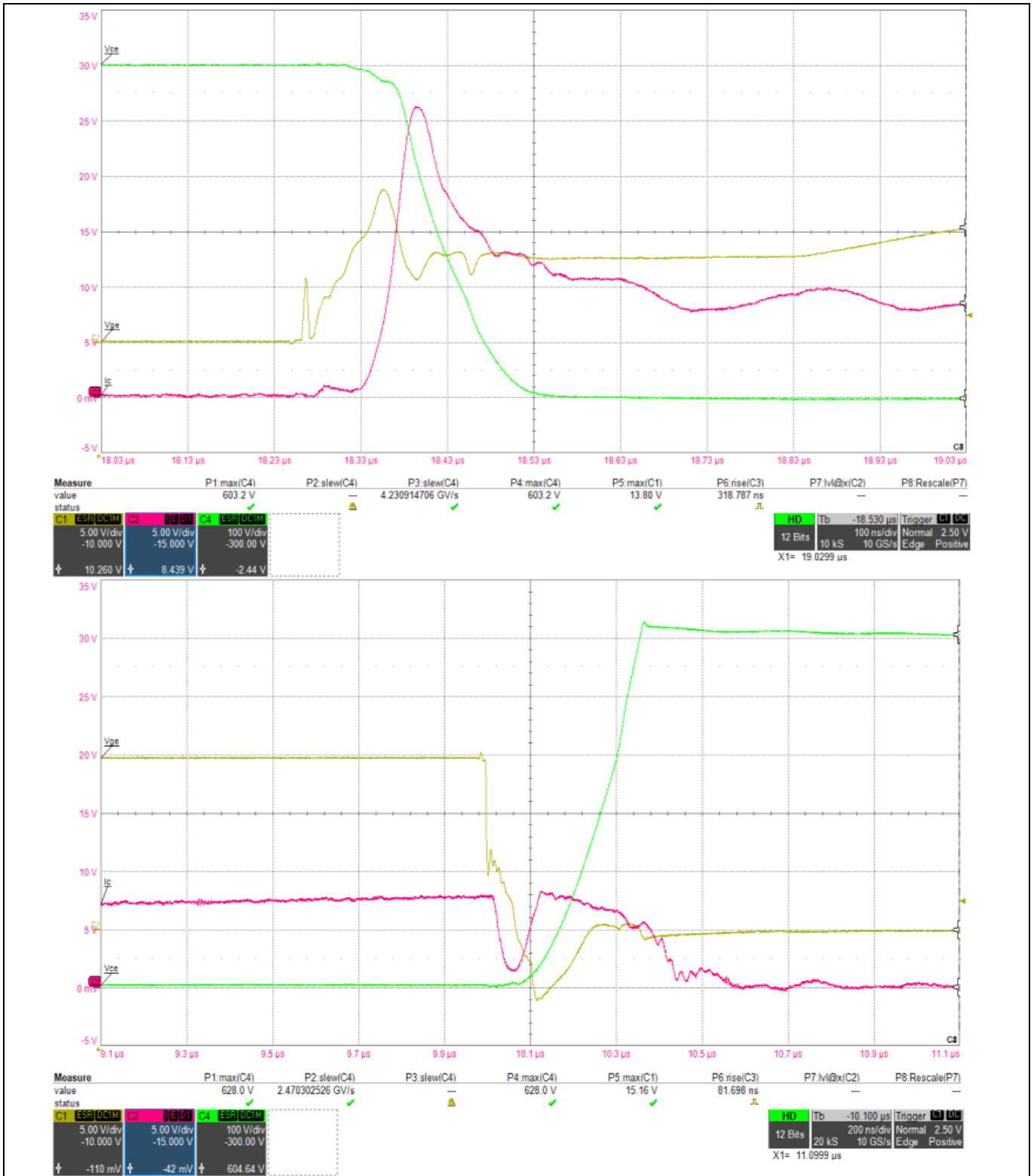
**Table 5 Connectors and pin assignment**

| Connector   | Pin   | Marking/<br>function   | Note   |
|---|---|--|--|
| J1  | 1,2   | <i>V-HV</i>  | High-voltage power supply  |
| J2  | 1,2   | <i>PHASE</i>   |  |
| J3  | 1<br>2  | <i>SENSE</i><br><i>HV_GND</i>  | Shunt resistor sense signal<br>High-voltage reference signal   |
| J4  | 1<br>2  | <i>GND</i><br><i>INF_HS</i>  | High-side negative gate driver reference<br>High-side gate driver input signal /INF  |
| J5  | 1<br>2  | <i>GND</i><br><i>INF_HS</i>  | High-side gate driver input signal IN<br>High -side gate driver supply reference   |
| J6, J7 (for direct supply only)<br>J11, J12 (for use with power supply unit only) | 1<br>2<br>3                                     | <i>VEE2_HS</i><br><i>GND2_HS</i><br><i>VCC2_HS</i>   | High-side negative gate driver supply<br>High-side gate driver supply reference<br>High-side positive gate driver supply   |
| J8  | 1<br>2  | <i>GND</i><br><i>VCC1</i>  | Input-side gate driver supply reference<br>Input-side gate driver supply   |
| J9  | 1<br>2  | <i>GND</i><br><i>IN_HS</i>   | Input-side gate driver supply reference<br>High-side gate driver input signal IN   |
| J10   | 1<br>2  | <i>GND</i><br><i>IN_HS</i>   | Low-side positive gate driver supply<br>Low-side gate driver input signal IN   |
| J13 (for use with power supply unit only)   | 1<br>2<br>3                                     | <i>GND</i><br><i>+15V</i><br><i>PWM_PSU</i>  | Input-side ground reference<br>External +15 V supply for power supply unit<br>PWM signal for power supply unit   |
| J14 (for use with power supply unit only)   | 1<br>2  | <i>GND</i><br><i>VCC1</i>  | Input-side ground reference<br>Input-side supply voltage, 3.3 V or 5 V   |
| J15   | 1<br>2  | <i>GND</i><br><i>+15V_IN</i>   | Input-side ground reference<br>Input-side supply voltage +1 5 V  |
| J16   | 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10 | <i>INF_HS1</i><br><i>INF_LS1</i><br><i>VCC1</i><br><i>GND</i><br><i>RST</i><br><i>FAULT</i><br><i>IN_HS1</i><br><i>IN_LS1</i><br><i>PWM_PSU</i><br><i>+15V</i> | Input control signal high-side for slew-rate-control<br>Input control signal low-side for slew-rate-control<br>Input-side supply voltage<br>Input-side ground reference<br>Reset input signal<br>Fault (overcurrent) indication signal<br>Input control signal high-side for PWM<br>Input control signal low-side for PWM<br>Input PWM signal for power supply unit<br>External +15 V supply for power supply unit (if not supplied through J15.2) |

System performance

### 4 System performance

This section shows examples of switching waveforms using EVAL-1ED3241MC12H. The waveforms represent turn-on and turn-off at a collector current of 7.5 A and a turn-off triggered by the overcurrent protection.



**Figure 6** Turn-on (top) and turn-off (bottom) of IKQ75N120CT2 as low-side switch ( $V_{DC} = 600\text{ V}$ ,  $I_C = 7.5\text{ A}$ ,  $/INF = 1$ ; yellow:  $V_{GE} 5\text{ V/div}$ , red:  $I_C 5\text{ A/div}$ , green:  $V_{CE,LS} 100\text{ V/div}$ )

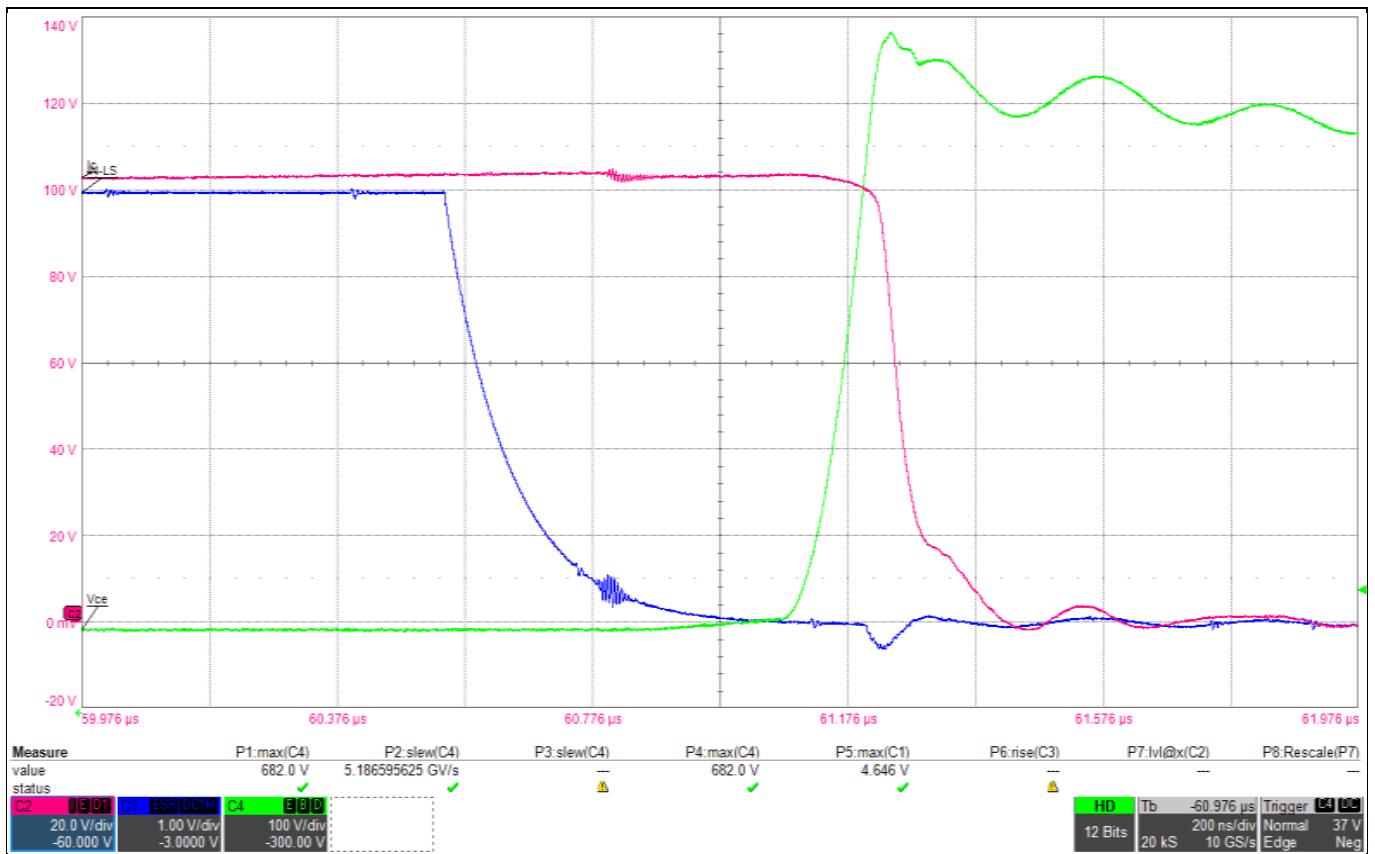


Figure 7 Protection turn-off of IKQ75N120CT2 as low-side switch ( $V_{dc} = 600\text{ V}$ ,  $I_c = 100\text{ A}$ ,  $/INF = 1$ ; red:  $I_c$  20 A/div, blue:  $V_{IN}$  1 V/div, green:  $V_{CE,LS}$  100 V/div )

## **5 Appendices**

### **5.1 Abbreviations and definitions**

**Table 6 Abbreviations**

| <b>Abbreviation</b> | <b>Meaning</b>               |
|---------------------|------------------------------|
| CE                  | Conformité Européenne        |
| EMI                 | Electromagnetic interference |
| UL                  | Underwriters Laboratories    |
|                     |                              |





**Revision history**

| <b>Document version</b> | <b>Date of release</b> | <b>Description of changes</b> |
|-------------------------|------------------------|-------------------------------|
| Revision 1.0            | 2021-05-28             | Initial version               |
|                         |                        |                               |
|                         |                        |                               |

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