CUSTOMER ADVISORY
ADV2012

Intel® Stratix® 10 Device Datasheet Update

Description:

Intel® is notifying customers of an important documentation update for Intel Stratix® 10 devices.

Following are the most recent changes listed in the document revision history of the Intel Stratix 10 device datasheet-

- Mentioned that the specifications for 1SG040HF35 and 1SX040HF35 devices are still preliminary in the Datasheet Status for Intel Stratix 10 Devices table.
- Updated the Absolute Maximum Ratings for Intel Stratix 10 Devices table.
  - Added VCCIO3C and VCCIO3D specifications.
  - Updated the description for VCCIO.
  - Added VI specifications for 3.3 V I/O.
- Added a new table: Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for 3.3 V I/O).
- Updated the Recommended Operating Conditions for Intel Stratix 10 Devices table.
  - Added VCCIO3C, VCCIO3D, and VI (for 3.3 V I/O) specifications.
  - Updated the description for VCCIO.
  - Updated note to TJ specification for Industrial.
- Added II_3.3VIO specifications in the I/O Pin Leakage Current for Intel Stratix 10 Devices table.
- Added CIO_3.3VIO specifications in the Pin Capacitance for Intel Stratix 10 Devices table.
- Added RPU specifications for 3.3 V I/O in the Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices table.
- Added 3.3 V LVTTL, 3.3 V LVCMOS, 3.0 V LVTTL, and 3.0 V LVCMOS specifications for 1SG040F35 or 1SX040F35 devices I/O bank 3C only in the

Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices table.
- Updated the description in the DPA Lock Time Specifications for Intel Stratix 10 Devices table.
- Added a note to VICM (AC coupled) in the E-Tile Receiver Specifications table.
- Added specifications for Intel Stratix 10 TX 400 devices and updated specifications for Intel Stratix 10 GX 400, SX 400, GX 1650, GX 2100, SX 1650, and SX 2100 devices in the following tables:
  - Configuration Bit Stream Sizes for Intel Stratix 10 Devices **(No changes to the Intel Quartus® Prime software. Bitstream size generated by the Intel Quartus® Prime software is correct.)**
  - Maximum Configuration Time Estimation for Intel Stratix 10 Devices (Avalon-ST)
  - Maximum Configuration Time Estimation for Intel Stratix 10 Devices (AS and SD/MMC)

The Intel Stratix 10 device datasheet can be found here:

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_datasheet.pdf

Recommended Actions:

Customers are requested to take note of the changes and determine the impact on their designs.

For questions or support, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

All Intel Stratix 10 devices

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2012-opn-list.xlsx

Reason for Change:

Addition and clarification of certain device specifications based on latest available data and characterization. There is no change to the Intel Stratix 10 device silicon and materials.

Change Implementation:

Table 1

Milestone	Availability
Availability of Intel Stratix 10 device datasheet update	Now

Contact:

For more information, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via: https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Customer Notifications Subscription:

Customers that subscribe to the Intel FPGA customer notification mailing list will receive the notifications automatically via email.

If you would like to receive Intel FPGA customer notifications by email, you can register to the Intel FPGA program and set up your subscription at: https://www.intel.com/content/www/us/en/programmable/my-intel/malemailsub/technical-updates.html

Revision History

Date	Rev	Description
03/20/2020	1.0.0	Initial Release