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NTE74HC273
Integrated Circuit
TTL – High Speed CMOS,
Octal Transparent D–Type Latch with 3–State Output

Description:

The NTE74HC273 is an octal transparent d–type latch in a 20–Lead DIP type package. When the latch–enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs..

A buffered output–enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high–impedance state. In the high–impedance state, the outputs neither load nor drive the bus lines significantly. The high–impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high–impedance state.

To ensure the high–impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current–sinking capability of the driver.

Features:

- Wide Power Supply Range: 2V to 6V
- Balanced Propagation Delay and Transition Times
- Standard Output Drives up to 15 LS–TTL Loads
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} ..... −0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} ..... ±20mA
DC Drain Current (Per Output), I_{OUT} ..... ±35mA
DC Output Source or Sink Current (Per Output), I_{OUT} ..... ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} ..... ±50mA
Storage Temperature Range, T_{stg} ..... −65°C to +150°C
Typical Thermal Resistance, Junction−to−Ambient, R_{thJA} ..... 69°C/W
Lead Temperature (During Soldering, 10sec), T_L ..... +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions: (Note 3)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
High−Level Input Voltage V_{CC} = 2.0V	V_{IH}	1.5	–	–	V
V_{CC} = 4.5V		3.15	–	–	V
V_{CC} = 6.0V		4.2	–	–	V
Low−Level Input Voltage V_{CC} = 2.0V	V_{IL}	–	–	0.5	V
V_{CC} = 4.5V		–	–	1.35	V
V_{CC} = 6.0V		–	–	1.8	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	−40	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

Note 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics:

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = −20μA	–	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V
			I_{OUT} = −6mA	4.5	–	3.98	3.84	V
			I_{OUT} = −7.8mA	6.0	–	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = 20μA	–	–	0.1	0.1	V
			I_{OUT} = 6mA	4.5	0.2	0.26	0.33	V
			I_{OUT} = 7.8mA	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Three−State Leakage Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}		6.0	–	±0.5	±5.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	8.0	80	μA
Maximum Input Capacitance	C_{IN}			–	–	10	10	pF
Maximum 3−State Output Capacitance	C_{OUT}			–	–	20	20	pF
Power Dissipation Capacitance	C_{PD}			5	51	–	–	pF

Timing Requirements:

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Minimum Pulse Duration, LE High	t_w		2.0	–	80	100	ns
			4.5	–	16	20	ns
			6.0	–	14	17	ns
Minimum Setup Time, Data Before LE↓	t_{su}		2.0	–	50	65	ns
			4.5	–	10	13	ns
			6.0	–	9	11	ns
Minimum Hold Time, Data After LE↓	t_h		2.0	–	5	5	ns
			4.5	–	5	5	ns
			6.0	–	5	5	ns

Switching Characteristics: (C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Propagation Delay Time (From Input D to Output Q)	t_{pd}		2.0	–	150	190	ns
			4.5	–	30	38	ns
			6.0	–	26	33	ns
Propagation Delay Time (From Input LE to Output Q)	t_{pd}		2.0	–	175	220	ns
			4.5	–	35	44	ns
			6.0	–	30	37	ns
Output Enable and Disable Time (From Input $\overline{OE}$ to Output Q)	t_{en}, t_{dis}		2.0	–	150	190	ns
			4.5	–	30	38	ns
			6.0	–	26	33	ns
Output Transition Time (To Output Q)	t_t		2.0	–	60	75	ns
			4.5	–	12	15	ns
			6.0	–	10	13	ns

Function Table (Each Latch:

Inputs			Output
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = Input Voltage HIGH Level
L = Input Voltage LOW Level
X = Don't Care
Z = Output in high impedance state

Pin Connection Diagram