MCU-SMHMI-HDUG

Smart HMI Hardware Development User Guide

Rev. 1 — 17 April 2023 User guide

Document Information

Information	Content
Keywords	MCU-SMHMI-HDUG, i.MX RT117H, EdgeReady, Smart HMI
Abstract	The Smart HMI solution is designed to provide a complete hardware and software reference for applications that require secured face recognition and local voice control, for example, coffee machine applications and elevator applications

1 Overview

NXP EdgeReady MCU-SMHMI solution is a Smart human machine interface (HMI) hardware and software solution for HMI projects. This solution is implemented using an NXP platform (SLN-TLHMI-IOT), which is based on NXP i.MX RT117H MCU. This solution is fully supported by NXP.

This document explains the overall design and usage of the SLN-TLHMI-IOT board from a hardware system perspective as well as provides recommended optimization for specific customer products. It also provides advanced system setup and hardware debugging instructions.

The MCU-SMHMI solution is designed to provide a complete hardware and software reference for applications that require secured face recognition and local voice control, for example, coffee machine applications and elevator applications. The main board and the external modules were carefully selected to achieve optimum performance, low-power capabilities, and competitive production cost. The board kit includes a “Kit Content” document, which lists all the accessories that come with the kit.

1.1 Acronyms

The table below lists the acronyms used in this document.

Table 1. Acronyms

Acronym	Meaning
ADC	Analog-to-digital converter
CAN	Controller area network
CSI	Camera serial interface
DAC	Digital-to-analog converter
DRAM	Dynamic random-access memory
eMMC	Embedded multimedia card
ESD	Electrostatic discharge
FPC	Flexible printed circuit
GPIO	General-purpose input/output
IR	Infrared
ISP	In-system programming
JTAG	Joint Test Access Group (IEEE standard 1149.1)
LAN	Local area network
LCD	Liquid crystal display
LDO	Low-dropout regulator
LED	Light-emitting diode
MEMS	Micro-electromechanical systems
MIPI	Mobile industry processor interface
MMC	Multimedia card
MSD	Mass storage device
PDM	Pulse-density modulation
PIR	Passive infrared

Table 1. Acronyms...*continued*

Acronym	Meaning
PLL	Phase-locked loop
PWM	Pulse width modulation
QSPI	Quad serial peripheral interface
ROM	Read-only memory
RTC	Real-time clock
SD	Secure digital
SDHC	Secure digital high capacity
SDIO	Secure digital input/output
SDRAM	Synchronous dynamic random-access memory
SNR	Signal-to-noise ratio
SoC	System-on-chip
SRAM	Static random-access memory
SWD	Serial wire debug
SWO	Serial wire debug trace output
TCM	Tightly coupled memory
TFT	Thin film transistor
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
WLAN	Wireless LAN

1.2 Related documentation

The table below lists the additional documents and resources that you can refer to for more information on the SLN-TLHMI-IOT board and MCU-SMHMI solution. Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to such documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document/resource	Link
MCU-SMHMI solution home page	http://www.nxp.com/mcu-smhmi
Smart HMI Getting Started Guide	MCU-SMHMI-GSG.pdf
Smart HMI User Guide	MCU-SMHMI-UG.pdf
Smart HMI Software Development User Guide	MCU-SMHMI-SDUG.pdf

1.3 Kit contents

The SLN-TLHMI-IOT board kit contains the following items:

- Fully assembled SLN-TLHMI-IOT board
- USB Type-C cable

1.4 Block diagram

The figure below shows the block diagram of the SLN-TLHMI-IOT board.

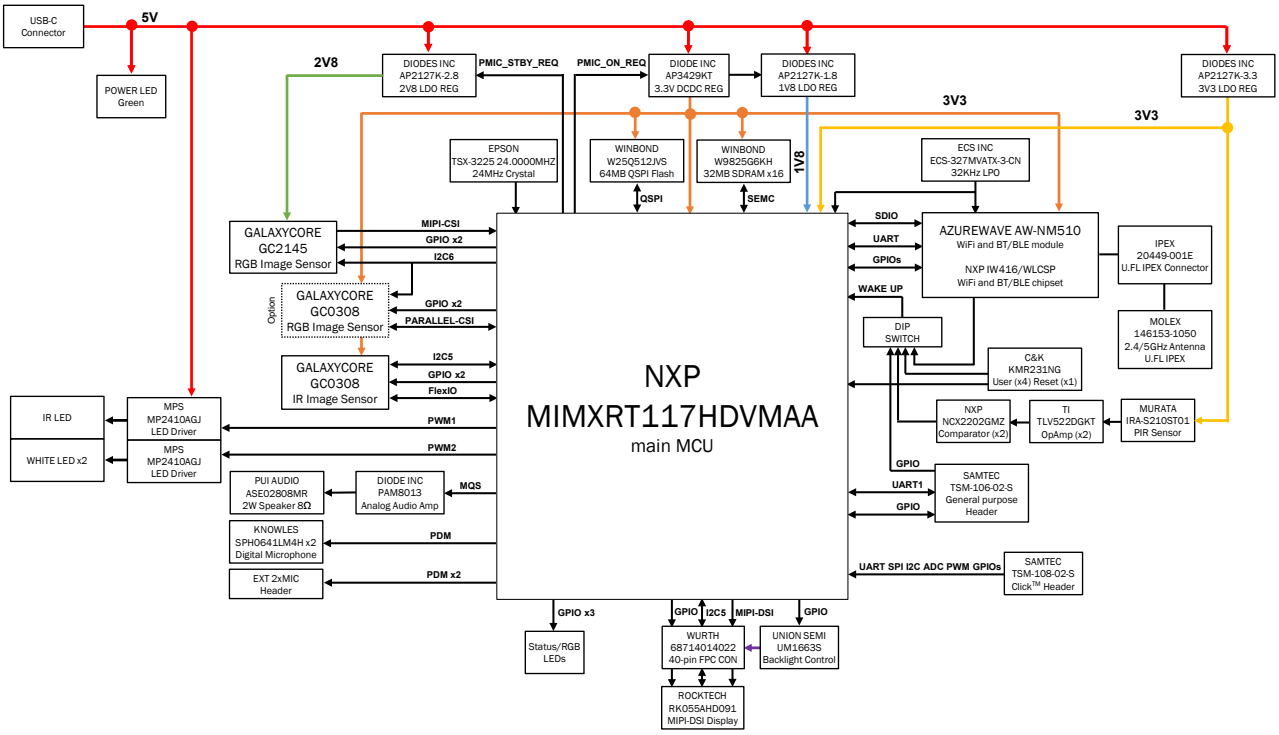

Figure 1. SLN-TLHMI-IOT block diagram

1.5 Board features

The table below lists the features of the SLN-TLHMI-IOT board.

Table 3. Board features

Board feature	Description	Manufacturer and/or part number
Processor	Application controller	NXP MIMXRT117HDVMAA
DRAM memory	32 MB, x16, 200 MHz data rate	Winbond W9825G6KH-5
Flash memory	64 MB, x4, 133 MHz frequency	Winbond W25Q512JVEIQ
RGB camera	Module with a GalaxyCore GC2145 UXGA CMOS image sensor	JSX-Vision GC20-0SLN-F0
	30-pin FPC connector	OK-16M030-04
	LED driver	MPS MP2410AGJ
	Two white LEDs	Lumileds L1T2-5770000000000
IR camera	Module with a GalaxyCore GC0308 VGA sensor	JSX-Vision GC03-0SLN-F0
	24-pin FPC connector	Molex 505110-2491
	LED driver	MPS MP2410AGJ
	IR LED	ORIENT-CHIP OCIR35-80I852-P0

Table 3. Board features*...continued*

Board feature	Description	Manufacturer and/or part number
Display	5.5 inch MIPI TFT LCD display at 720x1280 resolution	Rocktech RK055AHD091
	40-pin FPC MIPI display connector	Wurth 68714014022
Wireless connectivity	Wi-Fi/Bluetooth module with IW416 chipset	Azurewave AW-AM510
	u.FL MFH4 antenna connector	IPEX 20449-001E
	u.FL MFH4 antenna	Molex 146153-1050
Audio	3 W mono class-D audio amplifier	Diodes Incorporated PAM8013
	3 W enclosed speaker	PUI ASE02808MR-LW150-R
Sensor	PIR motion sensor	Murata IRA-S210ST01
	Two digital microphones	Knowles SPH0641LM4H-1
USB	USB Type-C connector	Molex 2012670005
Power supply	5 V DC through USB Type-C connector	
Power ICs	Main 3V3 DC-DC for Active mode	Diodes Incorporated AP3429KT
	2V8 LDO for Active mode	Diodes Incorporated AP2127K-1.2
	1V2 LDO for Active mode (not populated)	Diodes Incorporated AP2127K-2.8
	1V8 LDO for Active mode	Diodes Incorporated AP2127K-1.8
	3V3 LDO for SNVS/LP mode	Diodes Incorporated AP2127K-3.3
Buttons	Four user switches are connected to i.MX RT117H	E-Switch TL3301PF160QG
	One reset switch is connected to i.MX RT117H	C&K KMR231NG
User LED	RGB LED	Kingbright APTF1616LSEKJ3ZG
Debug	10-pin JTAG connector to connect an external debugger for debugging i.MX RT117H in SWD mode	Samtec FTSH-105-01-F-DV-K
Expansion	Two 8-position receptacles for connecting a Mikroelektronika Click board	Samtec SSM-108-F-SV
	3-pin header for connecting external microphones	Samtec TSM-103-01-G-SV-TR
	General-purpose header	Samtec SSM-106-F-SV
PCB	Six-layer PCB	

1.6 Board pictures

The figure below shows the top and bottom side views of the SLN-TLHMI-IOT board.

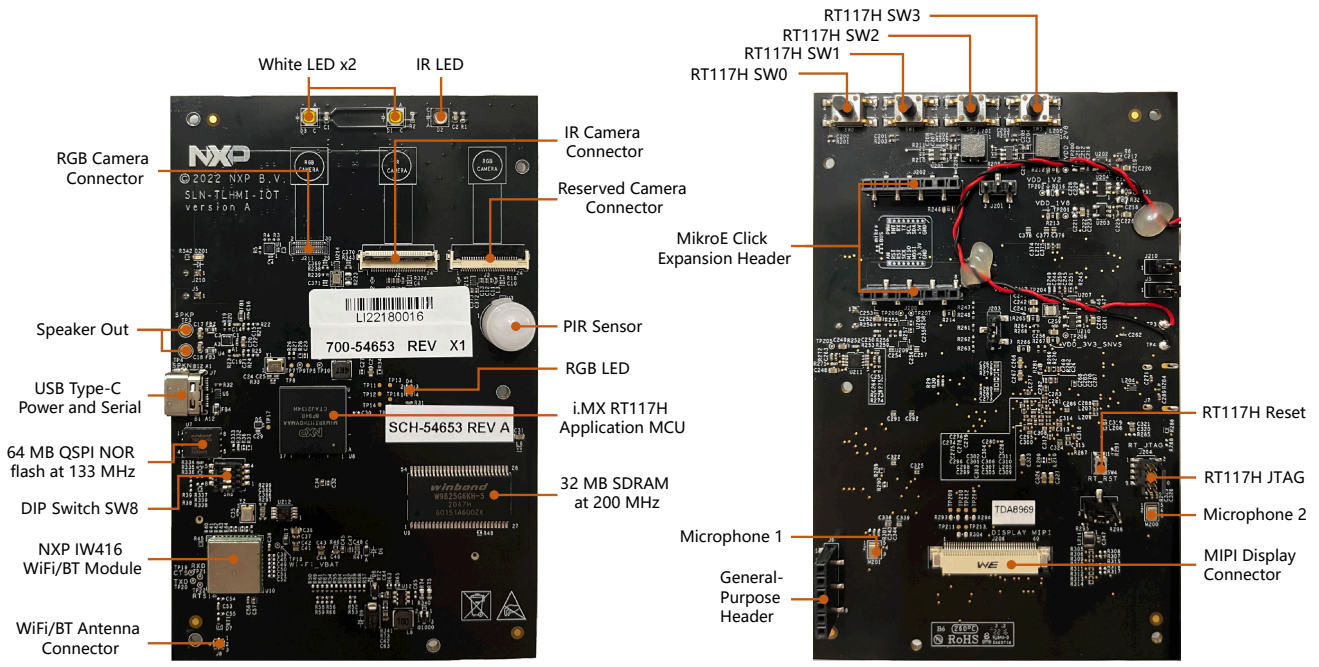

Figure 2. SLN-TLHMI-IOT board top and bottom views

The figure below shows the top and bottom side views of fully assembled SLN-TLHMI-IOT board.

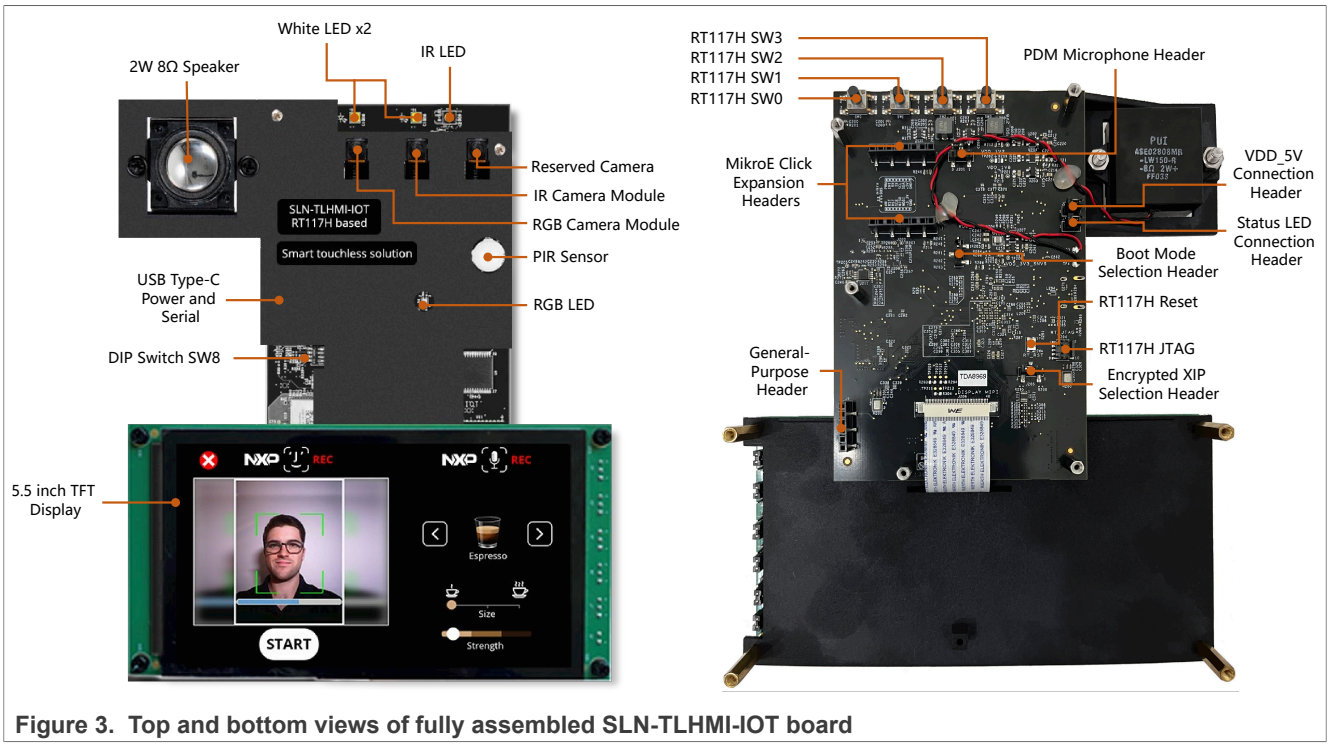

Figure 3. Top and bottom views of fully assembled SLN-TLHMI-IOT board

1.7 Board design files

The schematics, layout files, and gerber files (including silkscreen) can be downloaded from MCU-SMHMI solution home page.

1.8 PCB information

The SLN-TLHMI-IOT board uses standard six-layer technology. The material used is FR4. The table below describes the PCB stack-up information.

Table 4. PCB stack-up information

Layer	Description	Copper (Oz)	Dielectric thickness (mil)
1	Signal	1/2	Not applicable
	Dielectric	Not applicable	3.5
2	GND	1	Not applicable
	Dielectric	Not applicable	5
3	Signal	1	Not applicable
	Dielectric	Not applicable	37
4	Power	1	Not applicable
	Dielectric	Not applicable	5
5	GND	1	Not applicable
	Dielectric	Not applicable	3.5
6	Signal	1/2	Not applicable

2 Functional description

This section provides detailed information about the electrical design and practical considerations about the SLN-TLHMI-IOT board.

2.1 i.MX RT117H microcontroller

The i.MX RT117x crossover MCUs are part of the NXP EdgeVerse edge computing platform, having core frequency up to 1 GHz. This ground-breaking family combines superior computing power and multiple media capabilities with ease-of-use and real-time functionality. The dual-core i.MX RT117H MCU runs on the Arm Cortex-M7 core at 1 GHz and Arm Cortex-M4 core at 400 MHz, while providing advanced security.

2.1.1 Characteristics

The following are some major characteristics of the i.MX RT117H MCU:

- The i.MX RT117H MCU embeds 2 MB on-chip RAM in total, including 512 KB RAM, which can be flexibly configured as TCM or general-purpose on-chip RAM
- The i.MX RT117H MCU integrates an advanced power management module with DC-DC and LDO that reduces the complexity of external power supply and simplifies power sequencing
- Its memory controller supports a wide variety of external modules, including SDRAM (up to x32), single/dual/quad/octal SPI NOR flash (up to two), HyperRAM/Flash, and SD cards
- Its interfaces connect peripherals, such as camera sensors, displays, and WLAN or Bluetooth radio
- Similar to the i.MX processors, the i.MX RT117H MCU embeds rich audio and video features, including parallel CSI/DSI and MIPI CSI/DSI, graphics accelerator, microphone PDM input or MQS, and I2S audio interfaces

2.1.2 Boot mode configuration

The i.MX RT117H MCU has four boot modes, with one reserved for NXP use. The boot mode is selected based on the values stored in bits 1:0 of the BOOT_MODE register of the MCU, as described in the table below.

Table 5. Boot mode selection

BOOT_MODE[1]	BOOT_MODE[0]	Selected boot mode
0	0	Boot from Fuses
0	1	Serial Downloader
1	0	Internal Boot
1	1	Reserved

The table below explains how BOOT_MODE register bits 1:0 are mapped to MCU pins / board signals on the SLN-TLHMI-IOT board.

Table 6. BOOT_MODE register bit - MCU pin mapping

BOOT_MODE register bit	MCU pin name (number)	Boot mode function	Board signal
BOOT_MODE[0]	GPIO_LPSR_02 (P6)	BOOT_MODE0	SRC_BOOT_MODE00
BOOT_MODE[1]	GPIO_LPSR_03 (T7)	BOOT_MODE1	SRC_BOOT_MODE01

On the SLN-TLHMI-IOT board, MCU boot mode can be controlled using jumper J203, as shown in the table below.

Table 7. MCU boot mode control on SLN-TLHMI-IOT board

Jumper J203 setting	MCU boot mode
1-2 shorted (default setting)	Internal Boot
2-3 shorted	Serial Downloader

The figure below shows the circuit diagram of jumper J203.

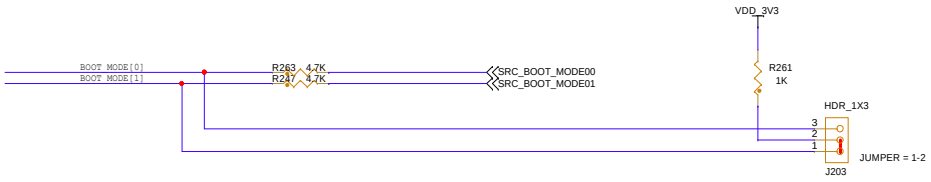

Figure 4. Boot mode selection jumper

2.2 Memories

2.2.1 QSPI NOR flash

One 512 Mbit (64 MB) serial quad SPI NOR flash memory Winbond W25Q512JVEIQ is connected to the i.MX RT117H MCU through its FlexSPI1_A interface in Quad SPI mode. This external memory stores the i.MX RT117H applications, which boot after reset, power-cycle, or wake-up.

The figure below shows the circuit diagram of the QSPI NOR flash memory.

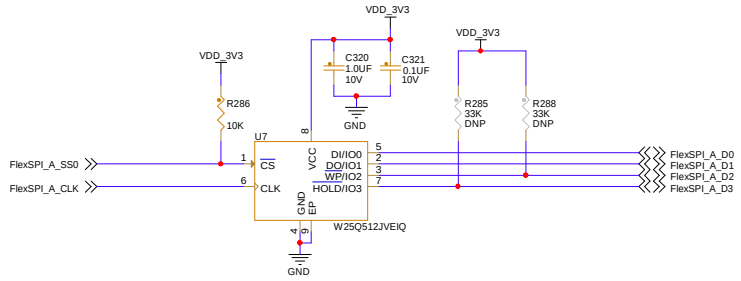

Figure 5. QSPI NOR flash memory

The table below shows signal mapping between the QSPI NOR flash memory W25Q512JVEIQ and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 8. W25Q512JVEIQ – i.MX RT117H signal mapping

W25Q512JVEIQ pin name	Board signal	i.MX RT117H pin name (number)
CLK	FlexSPI_A_CLK	GPIO_SD_B2_07 (G14)
CS	FlexSPI_A_SS0	GPIO_SD_B2_06 (F17)
DI/IO0	FlexSPI_A_D0	GPIO_SD_B2_08 (F15)
DO/IO1	FlexSPI_A_D1	GPIO_SD_B2_09 (H15)
WP/IO2	FlexSPI_A_D2	GPIO_SD_B2_10 (H14)
HOLD/IO3	FlexSPI_A_D3	GPIO_SD_B2_11 (F16)

2.2.2 SDRAM

One 256 Mbit (4194304 words x 4 banks x 16 bits), 200 MHz high-speed synchronous dynamic random access memory (SDRAM) module (Winbond W9825G6KH-5I) is used on the SLN-TLHMI-IOT board. The SDRAM is connected to the i.MX RT117H MCU through its SEMC interface.

The figure below shows the circuit diagram of the SDRAM.

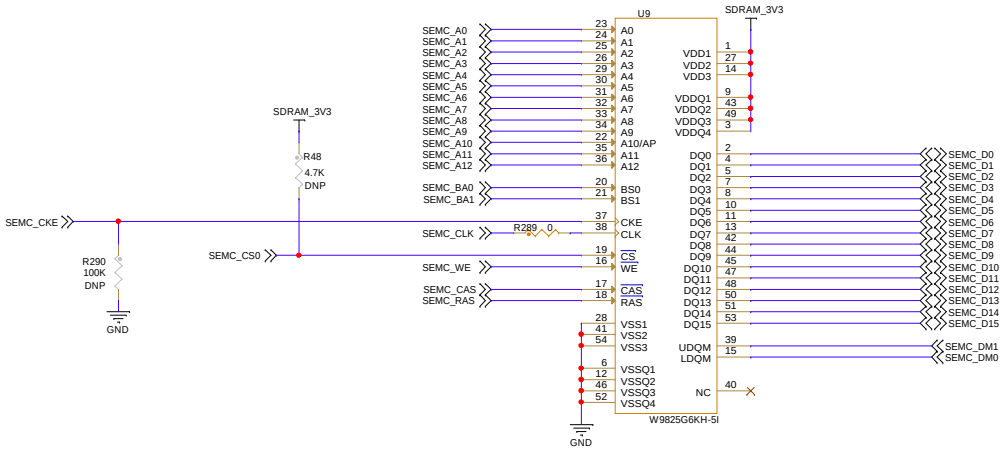

Figure 6. SDRAM

The table below shows signal mapping between the SDRAM W9825G6KH-5I and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 9. W9825G6KH-5I – i.MX RT117H signal mapping

W25Q512JVEIQ pin name	Board signal	i.MX RT117H pin name (number)
A[0:12]	SEMC_A[0:12]	GPIO_EMC_B1_10 — GPIO_EMC_B1_20 (A2, C2, C5, D5, B1, C1, D3, B3, B4, C4, C3)
DQ[0:15]	SEMC_D[0:15]	GPIO_EMC_B1_00 — GPIO_EMC_B1_07 and GPIO_EMC_B1_30 — GPIO_EMC_B1_37 (F3, F2, G4, E4, H5, F4, H4, H3, E3, D2, D1, E2, E1, F1, G1, H1)
BS0	SEMC_BA0	GPIO_EMC_B1_21 (G2)
BS1	SEMC_BA1	GPIO_EMC_B1_22 (H2)
CKE	SEMC_CKE	GPIO_EMC_B1_27 (G5)
CLK	SEMC_CLK	GPIO_EMC_B1_26 (J3)
CS	SEMC_CS0	GPIO_EMC_B1_29 (E6)
WE	SEMC_WE	GPIO_EMC_B1_28 (E5)
CAS	SEMC_CAS	GPIO_EMC_B1_24 (J5)
RAS	SEMC_RAS	GPIO_EMC_B1_25 (J4)
UDQM	SEMC_DM1	GPIO_EMC_B1_38 (J1)
LDQM	SEMC_DM0	GPIO_EMC_B1_08 (F5)

2.3 Camera modules

The SLN-TLHMI-IOT board supports the following types of cameras:

- RGB camera for displaying user feedback (MIPI-CSI2)
- IR camera for face recognition (FlexIO)
- Option for alternative RGB/IR camera (parallel CSI)

2.3.1 RGB camera (MIPI-CSI2)

The SLN-TLHMI-IOT board supports an RGB camera module for supplying RGB image required for display. The camera module has a high-quality, 2 megapixel GalaxyCore GC2145 UXGA CMOS image sensor.

Data is pushed through a 2-lane MIPI-CSI2 interface. The i.MX RT117H MCU configures and controls the GC2145 camera via its I2C6 interface, along with two GPIOs that are used for power-down and reset.

The GC2145 RGB camera is installed on the board through a 30-pin FPC connector (OK-16M030-04). The figure below shows the circuit diagram of the RGB camera connector.

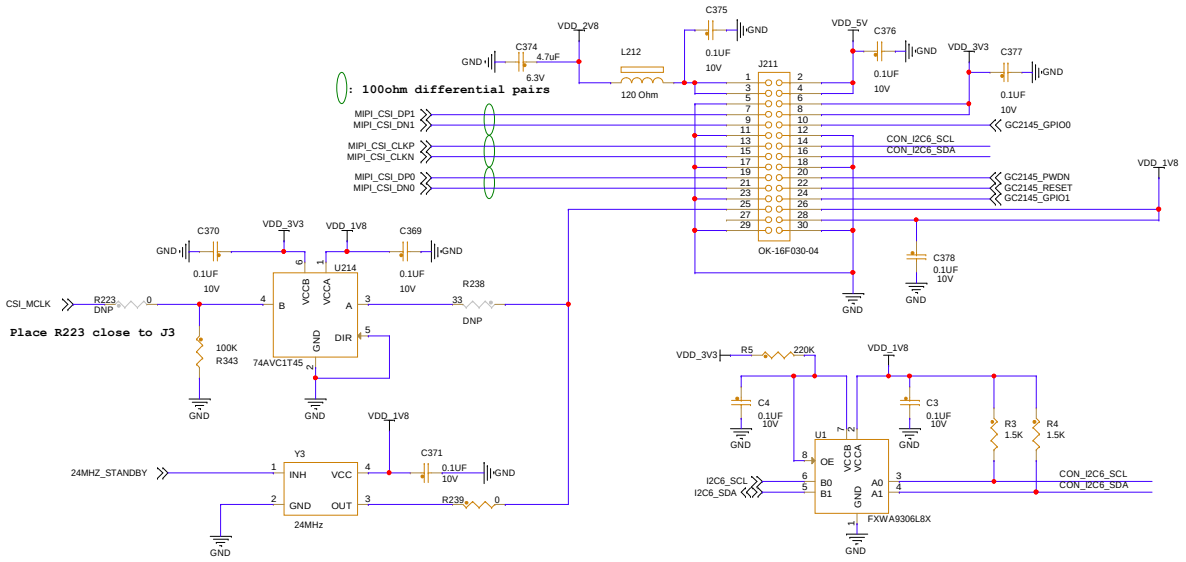

Figure 7. GC2145 RGB camera connector

The voltage level of the I2C6 interface and one GPIO from the i.MX RT117H MCU is 3.3 V. To match the GC2145 camera specification, a dual bidirectional voltage-level translator ON Semiconductor FXWA9306L8X (U1) and a single-bit bidirectional voltage-level translator Nexperia 74AVC1T45 (U214) are used to translate the voltage level down to 1.8 V.

Two clock options are available for GC2145 camera: one from CSI_MCLK of i.MX RT117H, and the other from a 24 MHz low-power crystal oscillator (Y3). The default option is the 24 MHz oscillator. Switching to CSI_MCLK of i.MX RT117H requires populating R223 and R238 resistors and removing R239 resistor.

The table below shows signal mapping between the RGB camera sensor GC2145 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 10. GC2145 – i.MX RT117H signal mapping

GC2145 pin name	Board signal	i.MX RT117H pin name (number)
RESETB	GC2145_RESET	GPIO_SNVS_02 (L9)
PWDN	GC2145_PWDN	GPIO_SNVS_06 (M9)
MCP	MIPI_CSI_CLKP	MIPI_CSI_CLKP (B12)
MCN	MIPI_CSI_CLKN	MIPI_CSI_CLKN (A12)
MDP0	MIPI_CSI_DP0	MIPI_CSI_DP0 (B11)
MDN0	MIPI_CSI_DN0	MIPI_CSI_DN0 (A11)
MDP1	MIPI_CSI_DP1	MIPI_CSI_DP1 (B13)
MDN1	MIPI_CSI_DN1	MIPI_CSI_DN1 (A13)
SBCL	CON_I2C6_SCL	GPIO_LPSR_07 (R8)
SBDA	CON_I2C6_SDA	GPIO_LPSR_06 (P8)
MCLK	CSI_MCLK	GPIO_AD_13 (L12) (for clock from CSI_MCLK)
	24MHZ_STANDBY	GPIO_SNVS_07 (R9) (for clock from crystal)

2.3.2 IR camera (FlexIO)

The SLN-TLHMI-IOT board supports an IR camera module for supplying IR images for 2D face recognition. The camera module has a GalaxyCore GC0308 VGA sensor, which provides a full-scale integration of high performance and low power with 640V x 480H resolution, 1/6.5-inch optical format, and on-chip ISP features.

Data is transmitted from the parallel CSI interface to the FlexIO interface of the i.MX RT117H MCU. The FlexIO interface emulates the running timing of the parallel CSI interface to receive IR images. The i.MX RT117H MCU configures and controls the GC0308 IR camera via its I2C5 interface, along with two GPIOs that are used for power-down and reset.

The GC0308 IR camera is installed on the board through a 24-pin FPC connector (Molex 505110-2491). The figure below shows the circuit diagram of the IR camera connector.

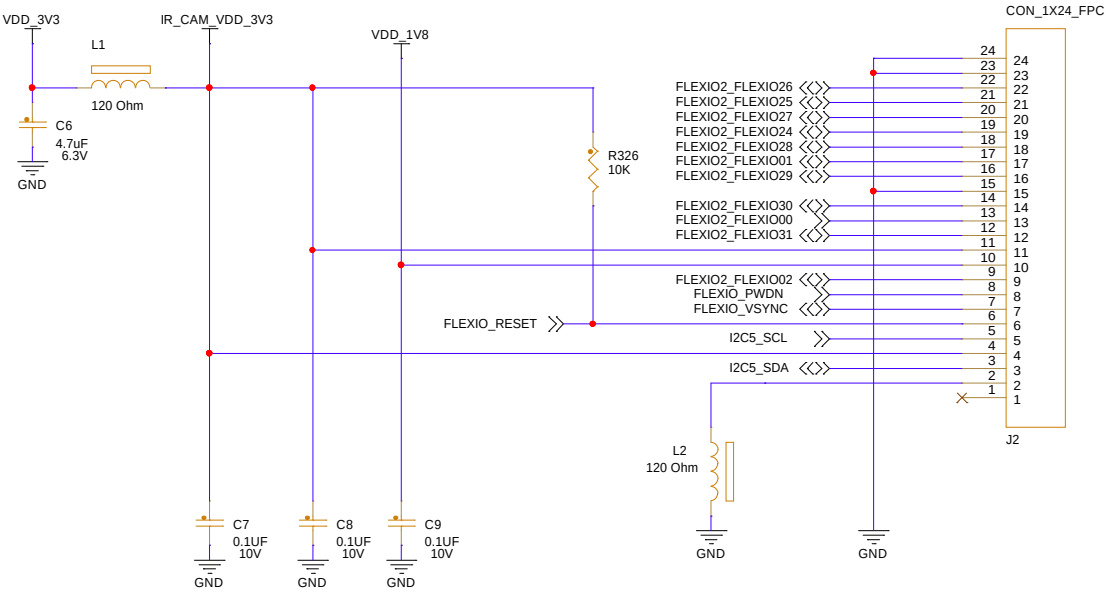

Figure 8. GC0308 IR camera connector

The table below shows signal mapping between the IR camera sensor GC0308 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 11. GC0308 – i.MX RT117H signal mapping

GC0308 pin names	Board signals	i.MX RT117H pin names (numbers)
RESETB	FLEXIO_RESET	GPIO_EMC_B2_15 (L2)
PWDN	FLEXIO_PWDN	GPIO_SD_B2_04 (F14)
HSYNC	FLEXIO2_FLEXIO02	GPIO_AD_02 (R13)
VSYNC	FLEXIO_VSYNC	GPIO_AD_32 (K16)
INCLK	FLEXIO2_FLEXIO00	GPIO_AD_00 (N12)
PCLK	FLEXIO2_FLEXIO01	GPIO_AD_01 (R14)
SBCL	I2C5_SCL	GPIO_LPSR_05 (N8)
SBDA	I2C5_SDA	GPIO_LPSR_04 (N7)
D[0:7]	FLEXIO2_FLEXIO[24:31]	GPIO_AD_[24:31] (L13, M15, L14, N16, L17, M17, K17, J17)

2.3.3 Reserved camera connector (parallel CSI)

The SLN-TLHMI-IOT board has a reserved parallel CSI interface to add an alternative RGB/IR camera. This camera can be configured and controlled via the I2C6 interface of the i.MX RT117H MCU, along with two GPIOs for power-down and reset. Data is transmitted via a parallel CSI interface to i.MX RT117H.

Note: *The RGB camera on MIPI-CSI2 and the alternative parallel camera cannot be used together.*

The figure below shows the circuit diagram of the reserved camera connector.

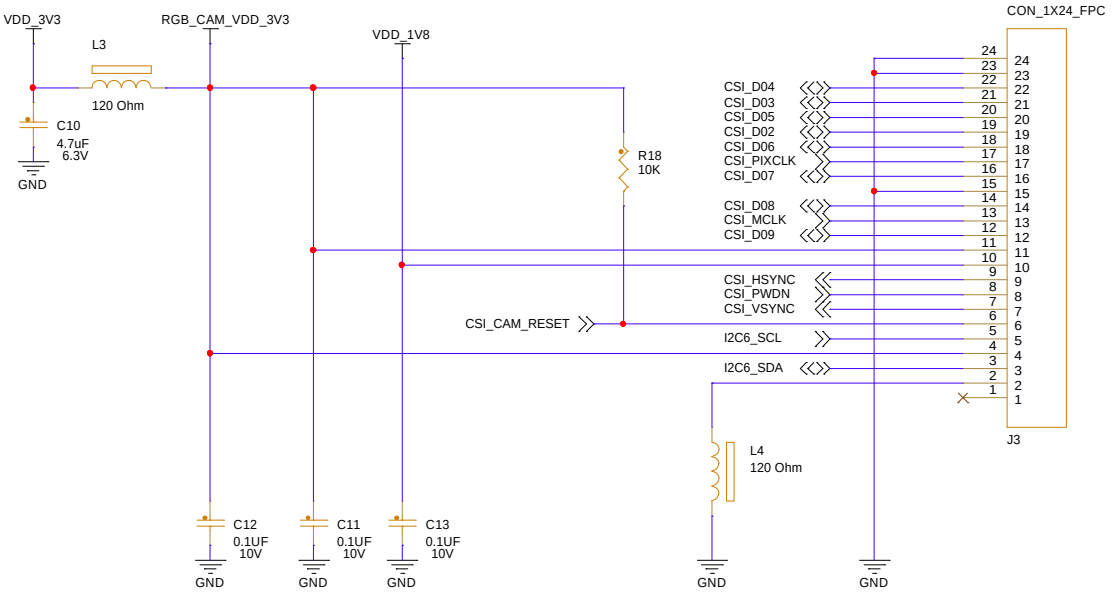

Figure 9. Reserved RGB/IR camera connector

The table below shows signal mapping between the reserved IR camera sensor GC0308 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 12. GC0308 – i.MX RT117H signal mapping (for reserved camera)

GC0308 pin names	Board signals	i.MX RT117H pin names (numbers)
RESETB	CSI_CAM_RESET	GPIO_EMC_B2_14 (M4)
PWDN	CSI_PWDN	GPIO_SNVS_06 (M9)
HSYNC	CSI_HSYNC	GPIO_AD_15 (M14)
VSYNC	CSI_VSYNC	GPIO_AD_14 (N14)
INCLK	CSI_MCLK	GPIO_AD_13 (L12)
PCLK	CSI_PIXCLK	GPIO_AD_12 (P17)
SBCL	I2C6_SCL	GPIO_LPSR_07 (R8)
SBDA	I2C6_SDA	GPIO_LPSR_06 (P8)
D[0:7]	CSI_D[02:09]	GPIO_AD_[23:16] (J12, K12, K14, K13, L16, M16, N15, N17)

2.3.4 LEDs

The SLN-TLHMI-IOT board provides the following LEDs corresponding to the RGB and IR camera modules:

- A pair of white LEDs (D1 and D3) corresponding to the RGB camera module

- An IR LED (D2) corresponding to the IR camera module

The RGB and IR camera LEDs are connected to LED drivers, U200 and U201, respectively. The LED drivers can be controlled by GPIOs, which are configured as pulse width modulation (PWM) outputs of the i.MX RT117H MCU. The brightness of the RGB and IR camera LEDs can be adjusted automatically according to the ambient light intensity.

The figure below shows the circuit diagrams of the RGB and IR camera LEDs.

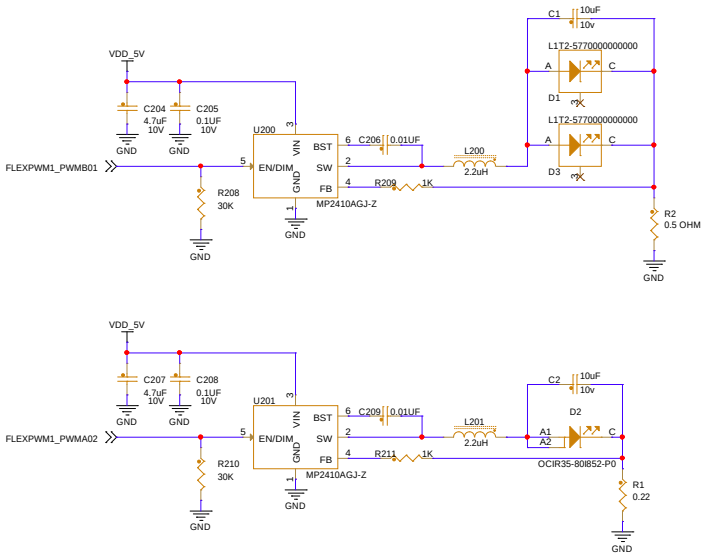

Figure 10. RGB and IR camera LEDs

Note: *Some initial SLN-TLHMI-IOT boards had R1 resistor with 1.0 Ω. For later boards, R1 resistor value was changed to 0.22 Ω. This change in resistor value gives better performance with new "Home Panel" application that is available in newer boards. To run the application on an older SLN-TLHMI-IOT board with optimal performance, you must perform the required modification for R1 resistor.*

The table below shows the i.MX RT117H MCU pins that drive RGB and IR camera LEDs on the SLN-TLHMI-IOT board.

Table 13. Driver pins for RGB and IR camera LEDs

LED	Board signal	i.MX RT117H pin name (number)
RGB camera LED	FLEXPWM1_PWMB01	GPIO_AD_03 (P15)
IR camera LED	FLEXPWM1_PWMA02	GPIO_AD_04 (M13)

2.4 Display module

The SLN-TLHMI-IOT board supports a 5.5 inch TFT LCD display (Rocktech RK055AHD091) with 720x1280 resolution, LED backlight, full viewing angle, MIPI interface, and capacitive touch panel. The RK055AHD091 LCD display is connected to the i.MX RT117H MCU via two-lane MIPI interface. The touch panel is controlled by the i.MX RT117H MCU via its I2C5 interface and several GPIOs.

The RK055AHD091 LCD display is installed on the board through a 40-pin FPC MIPI display connector (Wurth 68714014022). The figure below shows the circuit diagram of the display connector.

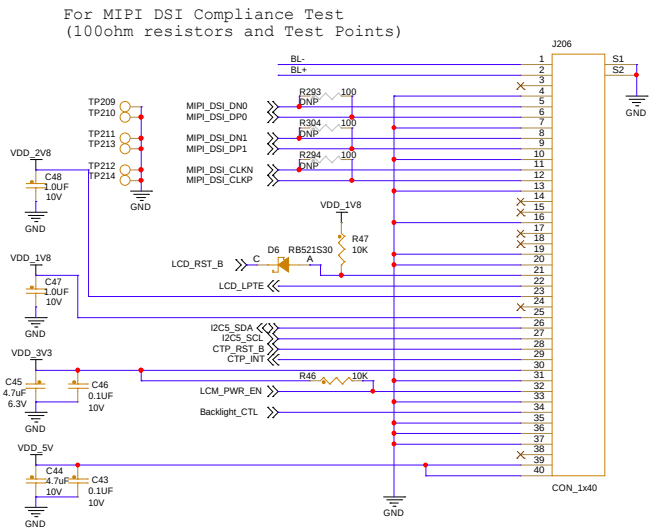

Figure 11. RK055AHD091 display connector

The table below shows signal mapping between the RK055AHD091 LCD display and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 14. RK055AHD091 – i.MX RT117H signal mapping

RK055AHD091 pin name	Board signal	i.MX RT117H pin name (number)
MIPI_TDN0	MIPI_DSI_DN0	MIPI_DSI_DN0 (A8)
MIPI_TDP0	MIPI_DSI_DP0	MIPI_DSI_DP0 (B8)
MIPI_TDN1	MIPI_DSI_DN1	MIPI_DSI_DN1 (A10)
MIPI_TDP1	MIPI_DSI_DP1	MIPI_DSI_DP1 (B10)
MIPI_TCN	MIPI_DSI_CLKN	MIPI_DSI_CLKN (A9)
MIPI_TCP	MIPI_DSI_CLKP	MIPI_DSI_CLKP (B9)
LRSTB	LCD_RST_B	GPIO_EMC_B2_12 (M2)
LPTE	LCD_LPTE	GPIO_AD_05 (P13)
CTP_SDA	I2C5_SDA	GPIO_LPSR_04 (N7)
CTP_SCL	I2C5_SCL	GPIO_LPSR_05 (N8)
CTP_RST	CTP_RST_B	GPIO_EMC_B2_11 (L4)
CTP_INT	CTP_INT	GPIO_EMC_B2_10 (R2)
POWER_EN	LCM_PWR_EN	GPIO_DISP_B2_15 (A4)
PWM	Backlight_CTL	GPIO_AD_06 (N13)

The backlight LEDs of the RK055AHD091 LCD display are driven by a boost converter composed of UM1663S, which is a highly integrated LED driver IC. The brightness of the backlight LED can be controlled by a GPIO that outputs a PWM signal.

The figure below shows the circuit diagram of the UM1663S boost driver.

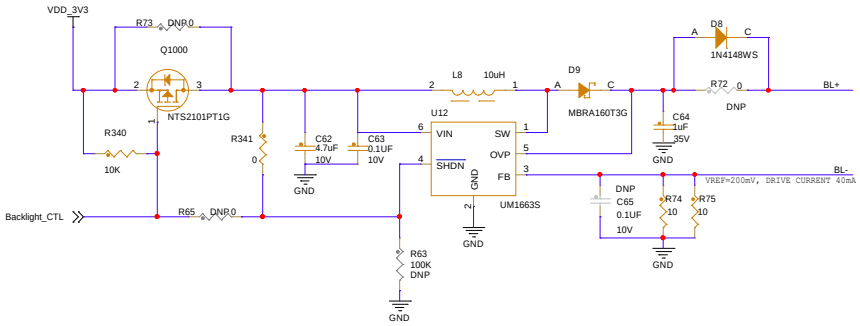

Figure 12. UM1663S boost driver

The table below shows signal mapping between the UM1663S boost driver and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 15. UM1663S – i.MX RT117H signal mapping

UM1663S pin name	Board signal	i.MX RT117H pin name (number)
SHDN	Backlight_CTL	GPIO_AD_06 (N13)

2.5 Wireless connectivity

The SLN-TLHMI-IOT board supports the Azurewave AW-AM510 advanced IEEE 802.11 a/b/g/n wireless LAN (WLAN) + Bluetooth 5.1 combo module, which is based on the highly integrated IW416 Wi-Fi 4 and Bluetooth 5.1 SoC.

The AW-AM510 module supports an SDIO device interface that conforms to the industry SDIO full-speed card specification. It allows the i.MX RT117H MCU to access the wireless SoC device using the SDIO bus protocol. It also supports a high-speed universal asynchronous receiver/transmitter (UART) interface, which is compliant to the industry standard 16550 specification. To provide physical transport between the Bluetooth SoC device and i.MX RT117H MCU for exchanging Bluetooth data, high-speed baud rates are supported.

An external low-power oscillator provides the 32 kHz clock to the AW-AM510 module. For the AW-AM510 module, the i.MX RT117H MCU can complete functions, such as reset, power down, and wake-up through GPIOs. The Bluetooth SoC device and Wi-Fi SoC device can also wake up the entire SLN-TLHMI-IOT system from Low-Power mode via GPIOs.

The figure below shows the circuit diagram of the WLAN+Bluetooth combo module AW-AM510.

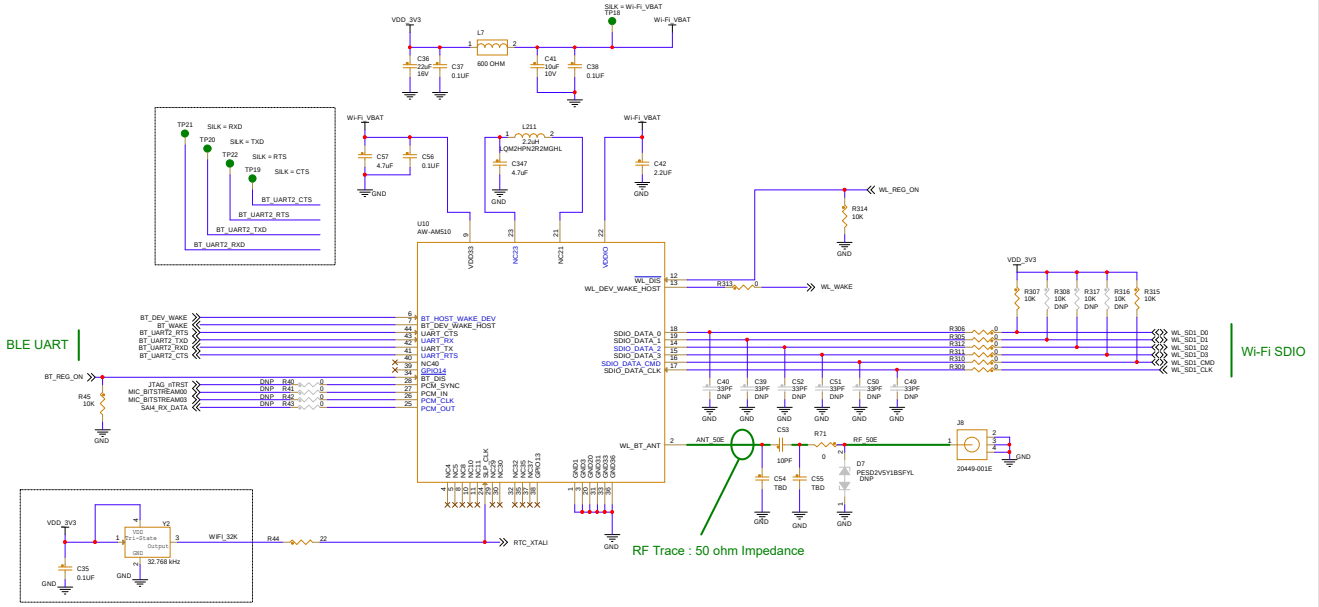

Figure 13. AW-AM510 module

The table below shows signal mapping between the WLAN+Bluetooth combo module AW-AM510 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 16. AW-AM510 – i.MX RT117H signal mapping

AW-AM510 pin name	Board signal	i.MX RT117H pin name (number)
BT_HOST_WAKE_ DEV	BT_DEV_WAKE	GPIO_SD_B2_05 (E14)
BT_DEV_WAKE_HOST	BT_WAKE	WAKEUP (T8)
UART_RTS	BT_UART2_RTS	GPIO_DISP_B2_13 (A5)
UART_TX	BT_UART2_TXD	GPIO_DISP_B2_10 (D9)
UART_RX	BT_UART2_RXD	GPIO_DISP_B2_11 (A6)
UART_CTS	BT_UART2_CTS	GPIO_DISP_B2_12 (B6)
BT_DIS	BT_REG_ON	GPIO_AD_35 (G17)
WL_DIS	WL_REG_ON	GPIO_AD_34 (J16)
WL_DEV_WAKE_ HOST	WL_WAKE	WAKEUP (T8)
SDIO_DATA_0	WL_SD1_D0	GPIO_SD_B1_02 (C15)
SDIO_DATA_1	WL_SD1_D1	GPIO_SD_B1_03 (B17)
SDIO_DATA_2	WL_SD1_D2	GPIO_SD_B1_04 (B15)
SDIO_DATA_3	WL_SD1_D3	GPIO_SD_B1_05 (A16)
SDIO_DATA_CMD	WL_SD1_CMD	GPIO_SD_B1_00 (B16)
SDIO_DATA_CLK	WL_SD1_CLK	GPIO_SD_B1_01 (D15)
PCM_SYNC	JTAG_nTRST	GPIO_LPSR_10 (R5)
PCM_IN	MIC_BITSTREAM00	GPIO_LPSR_09 (P5)
PCM_CLK	MIC_BITSTREAM03	GPIO_LPSR_12 (U5)
PCM_OUT	SAI4_RX_DATA	GPIO_LPSR_13 (U6)

2.6 Audio

The SLN-TLHMI-IOT board includes voice control and audio prompts, which are used alongside the onscreen animation to enhance the user experience.

The SLN-TLHMI-IOT board comes pre-assembled with a 3 W, mono, filter-less, class-D Diodes Incorporated PAM8013 amplifier, which has high PSRR and differential input. A 2 W PUI ASE02808MR-150-R speaker is also enclosed with the board.

Amplifier gain is fixed and defined by R20/R23 value. Volume control has to occur in the software domain. Audio stream (similar to PWM) is provided by the i.MX RT117H MQS interface and is filtered before feeding the analog audio amplifier. Although the amplifier is connected to MQS-RIGHT/MQS_LEFT (PWM) from i.MX RT117H, the incoming signal must be differential (complementary digital data).

The figure below shows the circuit diagram of the audio amplifier.

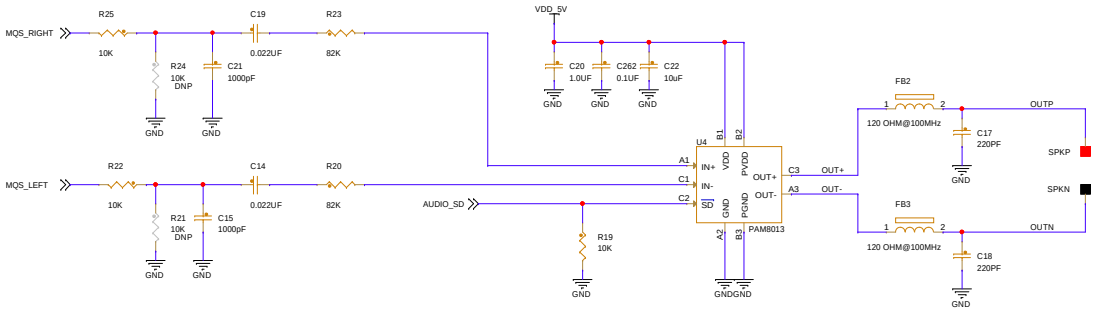

Figure 14. Class-D audio amplifier

The table below shows signal mapping between the audio amplifier PAM8013 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 17. PAM8013 – i.MX RT117H signal mapping

PAM8013 pin name	Board signal	i.MX RT117H pin name (number)
INP	MQS_RIGHT	GPIO_EMC_B1_40 (K1)
INN	MQS_LEFT	GPIO_EMC_B1_41 (L1)
SD	AUDIO_SD	GPIO_EMC_B2_19 (U2)

2.7 Sensors

The SLN-TLHMI-IOT board supports the following sensors:

- Two micro-electromechanical systems (MEMS) microphones
- One passive infrared (PIR) sensor

2.7.1 Microphones

The SLN-TLHMI-IOT board embeds two Knowles SPH0641LM4H-1 miniature, high-performance, low-power, bottom-port silicon digital microphones (M200 and M201) with single-bit PDM output. To allow data from the two microphones transmitting on the same data line, the SELECT pin of M200 is connected to VDD_1V8 whereas the SELECT pin of M201 is connected to GND. One of the microphones is sampled on the rising edge of the MIC_CLK signal and the other microphone on the falling edge of signal, by the MCU.

To achieve better signal-to-noise ratio (SNR) of the audio input stream, the microphones are powered by 1.8 V. An additional voltage-level translator NTB0102DP is required to interface to the i.MX RT117H MCU with the appropriate levels.

The figure below shows the circuit diagrams of the two microphones.

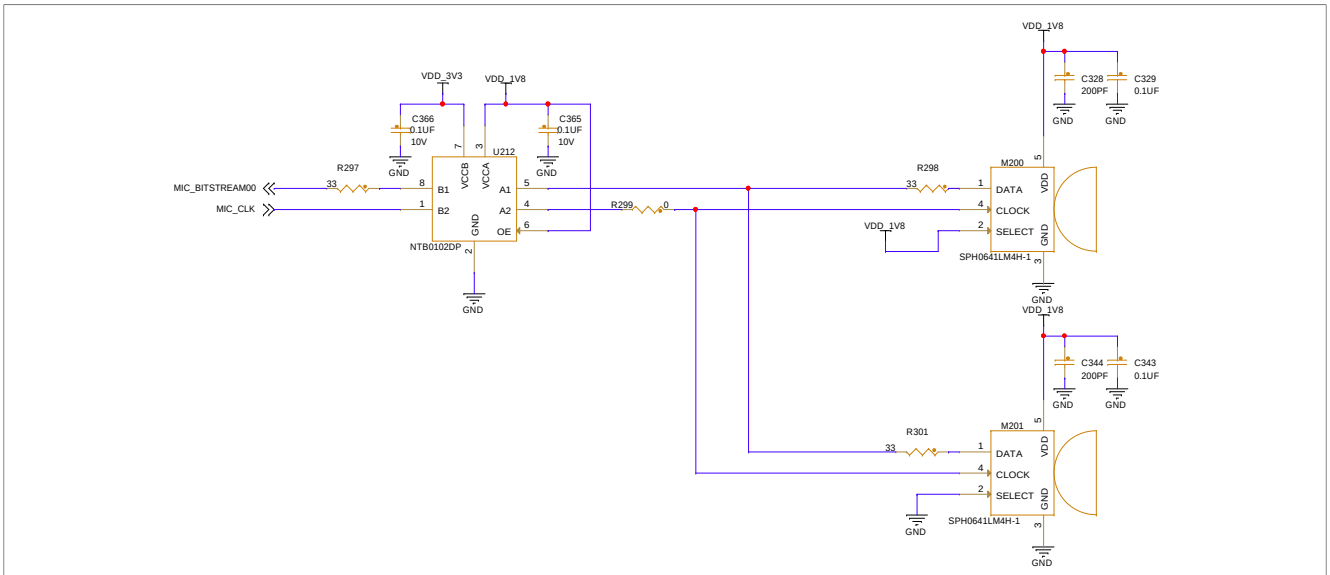

Figure 15. Microphones

The table below shows signal mapping between each microphone SPH0641LM4H-1 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 18. SPH0641LM4H-1 – i.MX RT117H signal mapping

SPH0641LM4H-1 pin name	Board signal	i.MX RT117H pin name (number)
DATA	MIC_BITSTREAM00	GPIO_LPSR_09 (P5)
CLOCK	MIC_CLK	GPIO_LPSR_08 (U8)

2.7.2 PIR sensor

To meet the low power consumption requirements of applications, a PIR sensor Murata IRA-S210ST01 is embedded on the front (top) side of the SLN-TLHMI-IOT board. The PIR sensor output signal is amplified and filtered before it triggers two comparators to generate a digital signal, which connects to the WAKEUP pin of the i.MX RT117H MCU and wakes up the entire system from deep sleep.

The figure below shows the circuit diagram of the PIR sensor.

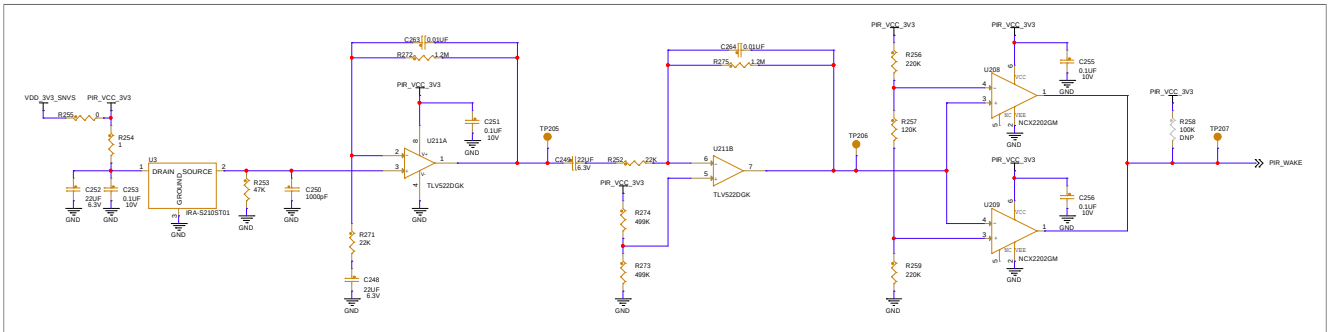

Figure 16. PIR sensor

Note: *You can also use some fully integrated digital PIR sensors to generate the WAKEUP signal to the i.MX RT117H MCU.*

The table below shows signal mapping between the PIR sensor IRA-S210ST01 and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 19. IRA-S210ST01 – i.MX RT117H signal mapping

IRA-S210ST01 pin name	Board signal	i.MX RT117H pin name (number)
PIR	PIR_WAKE	WAKEUP (T8)

2.8 Power circuitry

The SLN-TLHMI-IOT board can be powered from an external power source through a USB Type-C connector (J7). The 5 V input power (VDD_5V) is used to power the complete solution and it can be controlled by a jumper (J5).

To show the power ON status of the whole system, another jumper (J210) and an LED (D201) are used. If the jumper is shorted, then the LED indicates whether the whole system is powered ON.

The figure below shows the USB Type-C connector circuit diagram.

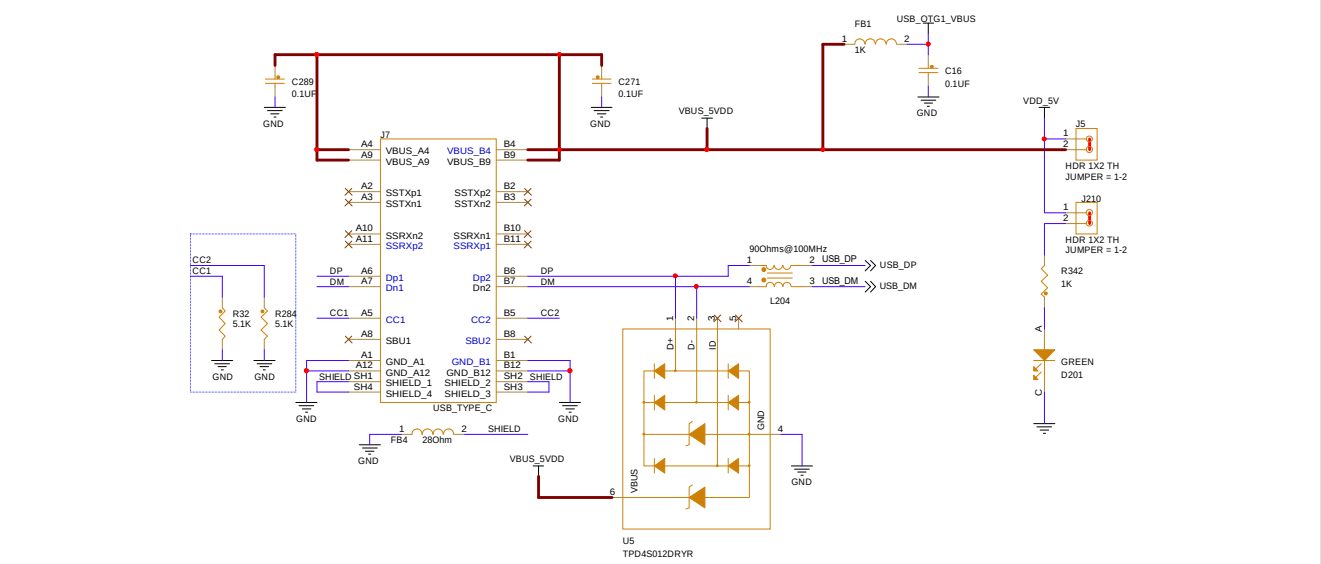

Figure 17. USB Type-C connector

For electrostatic discharge (ESD) protection, an ESD protection diode array, based on a four-channel transient voltage suppressor, is connected to the USB interface.

A DC-DC buck regulator (U207) generates the VDD_3V3 voltage to power the microcontroller, camera, display, and other onboard peripherals. The VDD_3V3 voltage respects the power specifications for every component embedded on the SLN-TLHMI-IOT board.

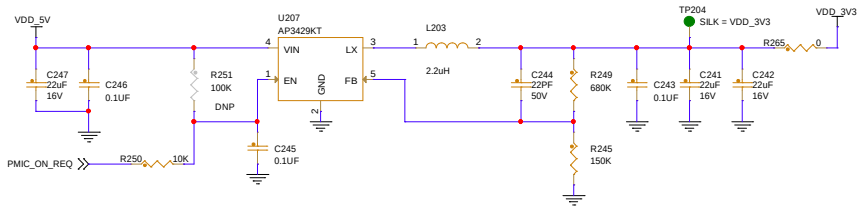

Figure 18. 3.3 V DC-DC buck regulator

A linear regulator (U202) generates the VDD_2V8 voltage to power the MIPI display and MIPI camera. A linear regulator (U204, not populated) can be populated to generate the VDD_1V2 voltage. Both are controlled by PMIC_STBY_REQ from the i.MX RT117H MCU.

The figure below shows the circuit diagram for the VDD_2V8 and VDD_1V2 voltage regulators.

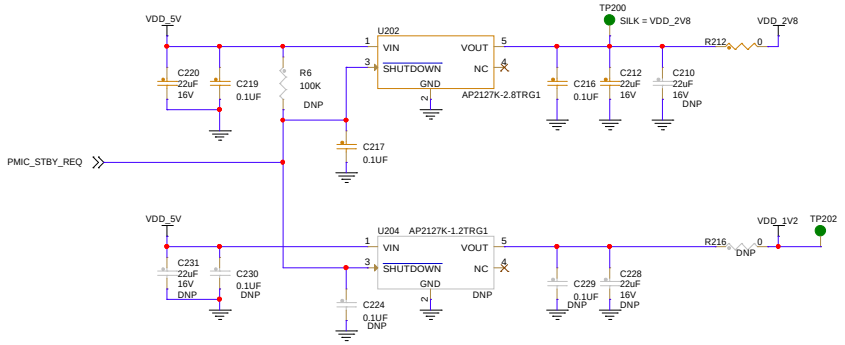

Figure 19. VDD_2V8 and VDD_1V2 voltage regulators

In addition, the board provides the following linear regulators to supply power to hardware components related to the Low-Power mode:

- U210: Generates the VDD_3V3_SNVS voltage
- U203: Generates the VDD_1V8 voltage

These regulators continue to supply power even after the system has entered the Low-Power mode. In the Low-Power mode, other regulators that supply power to the MCU and some board peripherals (such as sensors and display) are shut down.

The figure below shows the circuit diagram for the voltage regulators for the Low-Power mode.

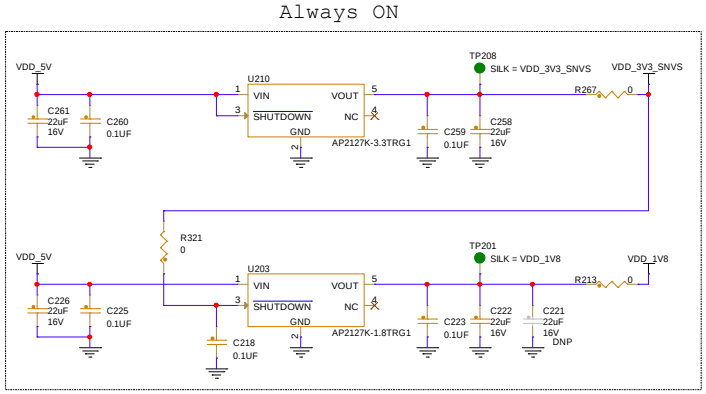

Figure 20. Voltage regulators for Low-Power mode

2.9 User interface buttons

The SLN-TLHMI-IOT board has five push buttons: SW0, SW1, SW2, SW3, and SW4. These buttons are placed on the back (bottom) side of the board. They are connected to the i.MX RT117H MCU through five GPIOs:

- SW0 button is connected to the WAKEUP pin of the i.MX RT117H MCU and it should be reserved to control low-power modes
- SW1, SW2, and SW3 buttons are connected to some i.MX RT117H GPIOs. They are used in default out-of-box experience (OOBE) software to select application and MSD software update functionality.
- SW4 button is connected to the POR pin of the MCU. Pressing SW4 resets the MCU.

The figure below shows the circuit diagrams of the user buttons.

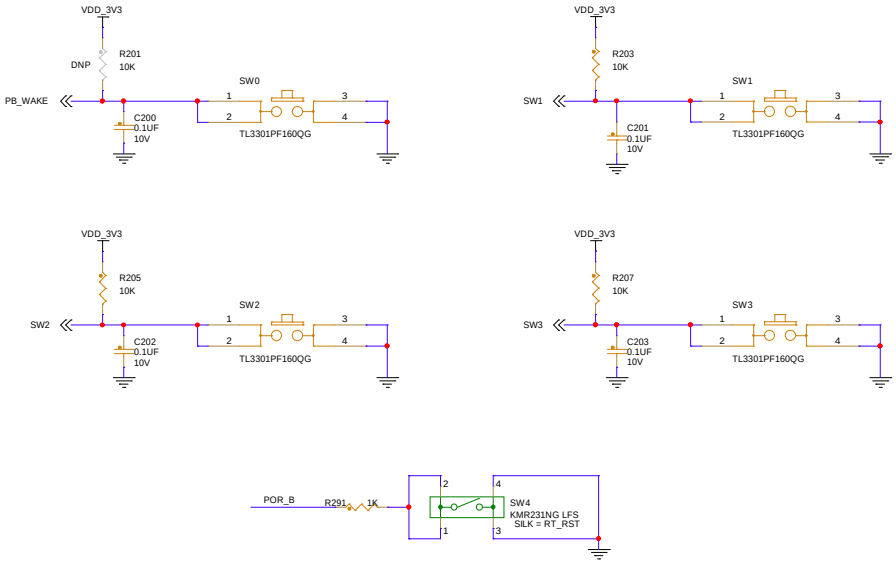

Figure 21. User buttons

The table below shows signal mapping between the user buttons and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 20. User button – i.MX RT117H signal mapping

User button	Board signal	i.MX RT117H pin name (number)
SW0	PB_WAKE	WAKEUP (T8)
SW1	SW1	GPIO_EMC_B2_05 (N1)
SW2	SW2	GPIO_EMC_B2_06 (T1)
SW3	SW3	GPIO_EMC_B2_07 (M3)
SW4	POR_B	POR (T10)

2.10 User LED

An RGB LED (APTF1616LSEKJ3ZGKQBC) is connected to the i.MX RT117H MCU through three GPIOs, which are configured as pulse width modulation (PWM) outputs to control color and brightness.

The figure below shows the circuit diagram of the user RGB LED.

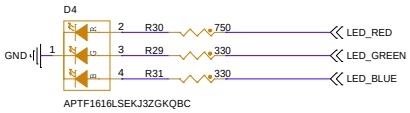

Figure 22. User RGB LED

The table below shows signal mapping between the user RGB LED and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 21. User RGB LED – i.MX RT117H signal mapping

LED	Board signal	i.MX RT117H pin name (number)
R_LED	LED_RED	GPIO_EMC_B2_00 (K2)
G_LED	LED_GREEN	GPIO_EMC_B2_01 (K4)
B_LED	LED_BLUE	GPIO_EMC_B2_02 (K3)

2.11 Debug interface

The i.MX RT117H MCU supports a JTAG/SWD interface for debugging and programming. The JTAG pins of the MCU are connected to a 10-pin JTAG header (J204) on the board for connecting an external debugger, for example, SEGGER J-Link probe.

The figure below shows the circuit diagram of the SLN-TLHMI-IOT debug interface.

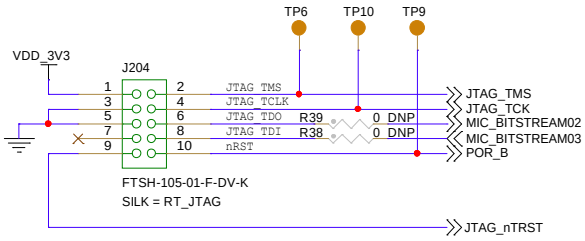

Figure 23. Debug interface

The table below shows signal mapping between the JTAG header and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 22. JTAG header – i.MX RT117H signal mapping

Header pin number	Board signal	i.MX RT117H pin name (number)
2	JTAG_TMS	GPIO_LPSR_15 (U7)
4	JTAG_TCK	GPIO_LPSR_14 (T6)
6	MIC_BITSTREAM02	GPIO_LPSR_11 (T5)
8	MIC_BITSTREAM03	GPIO_LPSR_12 (U5)
9	JTAG_nTRST	GPIO_LPSR_10 (R5)
10	POR_B	POR (T10)

2.12 Expansion connectors

To expand board functionality, the SLN-TLHMI-IOT board provides a pair of 8-position receptacles (J200 and J202) that supports I2C, UART, SPI, PWM, ADC, and GPIO interfaces. The connector pair is fully compliant with MikroElektronika Click boards.

The board also provides an additional 3-pin header (J201) for connecting additional PDM microphones. In addition, the board includes a general-purpose 6-pin header (J9), which supports UART interface and provides a GPIO for external connection and an option for external 3.3 V wake-up signal.

The figure below shows the circuit diagrams of the expansion connectors.

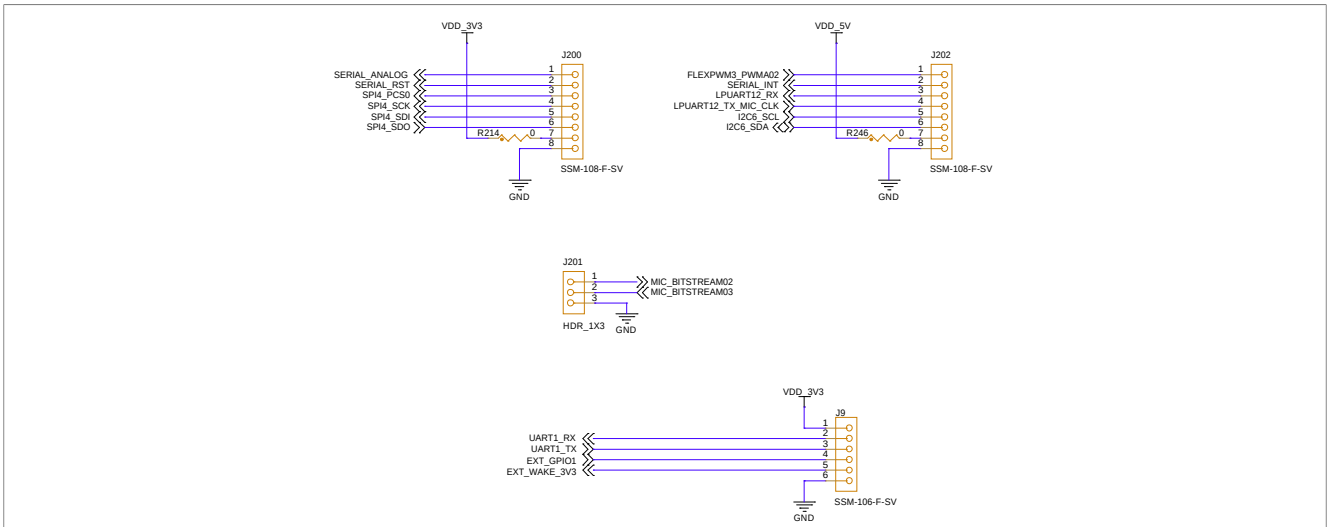

Figure 24. Expansion connectors

The table below shows signal mapping between the expansion connectors and i.MX RT117H MCU on the SLN-TLHMI-IOT board.

Table 23. Expansion connector – i.MX RT117H signal mapping

Pin number	Board signal	i.MX RT117H pin name (number)
J200		
1	SERIAL_ANALOG	GPIO_AD_33 (H17)
2	SERIAL_RST	GPIO_EMC_B2_20 (R3)
3	SPI4_PCS0	GPIO_SD_B2_01 (J14)
4	SPI4_SCK	GPIO_SD_B2_00 (J15)
5	SPI4_SDI	GPIO_SD_B2_03 (E15)
6	SPI4_SDO	GPIO_SD_B2_02 (H13)
7	VDD_3V3	Not applicable
8	GND	Not applicable
J202		
1	FLEXPWM3_PWMA02	GPIO_EMC_B2_04 (M1)
2	SERIAL_INT	GPIO_DISP_B2_14 (A7)
3	LPUART12_RX	GPIO_LPSR_01 (R6)
4	LPUART12_TX_MIC_CLK	GPIO_LPSR_00 (N6)
5	I2C6_SCL	GPIO_LPSR_07 (R8)
6	I2C6_SDA	GPIO_LPSR_06 (P8)
7	VDD_5V	Not applicable

Table 23. Expansion connector – i.MX RT117H signal mapping*...continued*

Pin number	Board signal	i.MX RT117H pin name (number)
8	GND	Not applicable
J201		
1	MIC_BITSTREAM02	GPIO_LPSR_11 (T5)
2	MIC_BITSTREAM03	GPIO_LPSR_12 (U5)
3	GND	Not applicable
J9		
1	VDD_3V3	Not applicable
2	UART1_RX	GPIO_DISP_B2_09 (D8)
3	UART1_TX	GPIO_DISP_B2_08 (B5)
4	EXT_GPIO1	GPIO_EMC_B2_03 (R1)
5	EXT_WAKE_3V3	WAKEUP (T8)
6	GND	Not applicable

3 Low-power optimizations

The SLN-TLHMI-IOT board supports the Low-Power mode where only the VDD_5V, VDD_3V3_SNVS, and VDD_1V8 signals are active.

To wake up the SLN-TLHMI-IOT system from the Low-Power mode, the board supports the following wake-up sources and some combinations of them. All these wake-up sources form a set of Low-Power mode configurations for the SLN-TLHMI-IOT board.

- SW0 push button
- PIR sensor
- Wi-Fi radio
- Bluetooth Low Energy (BLE) radio
- External 3.3 V wake-up signal

You can configure the SLN-TLHMI-IOT wake-up source using the SW8 DIP switch. The table below describes all supported Low-Power mode configurations for the SLN-TLHMI-IOT board. All other configurations are not supported and may lead to uncontrolled power state.

Table 24. Low-Power mode configurations

Configuration	SW8[1] (SWO)	SW8[2] (PIR)	SW8[3] (Wi-Fi)	SW8[4] (BLE/EXT)
Configuration 1	ON	OFF	OFF	OFF
Configuration 2	OFF	ON	OFF	OFF
Configuration 3	OFF	OFF	ON	OFF
Configuration 4	OFF	OFF	OFF	ON
Configuration 5	ON	ON	OFF	OFF
Configuration 6	ON	OFF	ON	OFF
Configuration 7	ON	OFF	OFF	ON
Configuration 8	OFF	ON	ON	OFF
Configuration 9	OFF	ON	OFF	ON

The figure below shows the circuit diagram of the SW8 DIP switch.

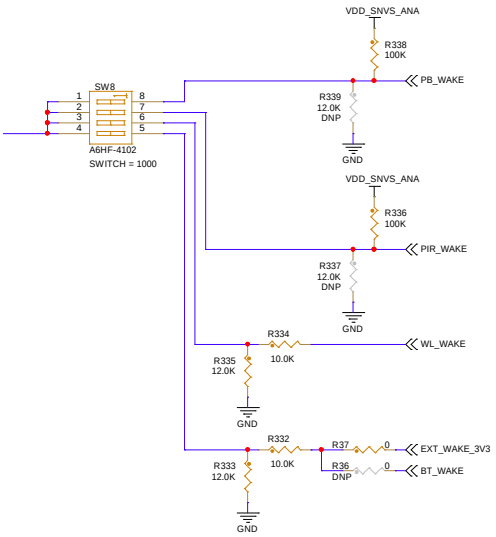

Figure 25. SW8 DIP switch

4 Revision history

The table below summarizes the revisions to this document.

Table 25. Revision history

Revision	Date	Topic cross-reference	Change description
1	17 April 2023	Section 2.3.4	Updated R1 resistor value in Figure 10 from 1.0 to 0.22 and added a note below the figure
0	4 November 2022		Initial release

5 Legal information

5.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. - NXP B.V. is not an operating company and it does not distribute or sell products.

5.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com

Date of release: 17 April 2023
Document identifier: MCU-SMHMI-HDUG