

# MOSFET – Dual, N-Channel, Logic Level, POWERTRENCH®

40 V, 12 A, 8.2 mΩ

## FDMC9430L-F085

### Features

- Typical  $R_{DS(on)} = 6.3\text{ m}\Omega$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 12\text{ A}$
- Typical  $Q_{g(tot)} = 15\text{ nC}$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 12\text{ A}$
- UIS Capability
- This Device is Pb-Free, Halide Free and RoHS Compliant
- AEC Qualified AEC-Q101

### Applications

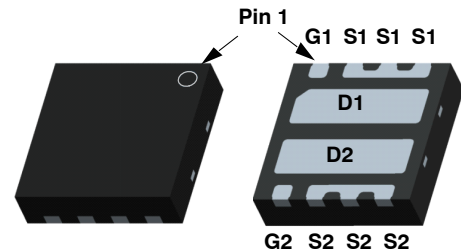
- Battery Protection
- Load Switching
- Point of Load

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 10$ ) (Note 1) $T_C = 25^\circ\text{C}$	12	A
	Pulsed Drain Current $T_C = 25^\circ\text{C}$	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	21.6	mJ
$P_D$	Power Dissipation	11.4	W
	Derate Above $25^\circ\text{C}$	0.1	W/ $^\circ\text{C}$
$T_J, T_{stg}$	Operating and Storage Temperature	$-55$ to $+150$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	13	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction-to-Ambient (Note 3)	65	$^\circ\text{C}/\text{W}$

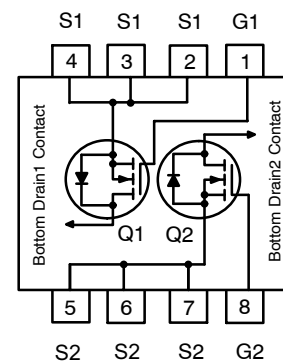
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 40\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a  $1\text{ in}^2$  pad of 2 oz copper.



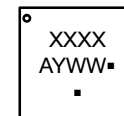
WDFN8  
3x3, 0.65P  
CASE 511DG

### PIN ASSIGNMENT



Dual N-Channel MOSFET

### MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC9430L-F085	WDFN8 (Pb-Free, Halide Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDMC9430L-F085

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

B <sub>VDSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	40	-	-	V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	-	-	1	μA
			T <sub>J</sub> = 150°C (Note 4)	-	-	0.2	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±12 V	-	-	±100	nA	

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1	1.8	3	V		
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	I <sub>D</sub> = 10 A, V <sub>GS</sub> = 4.5 V	-	8.9	11.5	mΩ		
			I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V	T <sub>J</sub> = 25°C	-		6.3	8.0
				T <sub>J</sub> = 150°C (Note 4)	-		10.2	13.0

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	984	-	pF	
C <sub>oss</sub>	Output Capacitance		-	315	-		
C <sub>rss</sub>	Reverse Transfer Capacitance		-	18	-		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0.5 V, f = 1 MHz	-	1.1	-	Ω	
Q <sub>g(ToT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10 V	V <sub>DD</sub> = 32 V, I <sub>D</sub> = 12 A	-	15	22	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 to 1 V		-	0.9	-	
Q <sub>gs</sub>	Gate-to-Source Gate Charge			-	2.6	-	
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge		-	2.1	-		

### SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	-	-	13	ns
t <sub>d(on)</sub>	Turn-On Delay		-	7	-	
t <sub>r</sub>	Rise Time		-	2	-	
t <sub>d(off)</sub>	Turn-Off Delay		-	17	-	
t <sub>f</sub>	Fall Time		-	2	-	
t <sub>off</sub>	Turn-Off Time		-	-	28	

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source-to-Drain Diode Voltage	I <sub>SD</sub> = 12 A, V <sub>GS</sub> = 0 V	-	-	1.2	V
		I <sub>SD</sub> = 6 A, V <sub>GS</sub> = 0 V	-	-	1.1	
t <sub>rr</sub>	Reverse-Recovery Time	V <sub>DD</sub> = 32 V, I <sub>F</sub> = 12 A, di <sub>SD</sub> /dt = 100 A/μs	-	32	48	ns
Q <sub>rr</sub>	Reverse-Recovery Charge		-	16	24	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

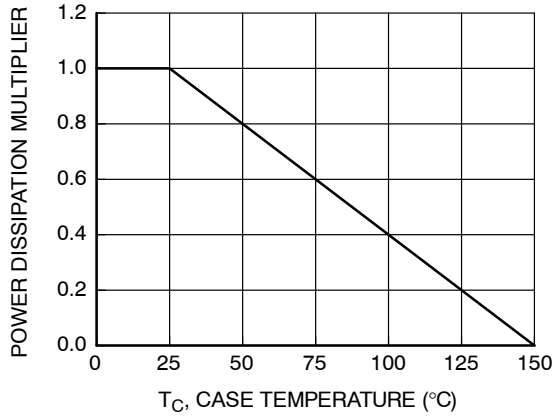


Figure 1. Normalized Power Dissipation vs. Case Temperature

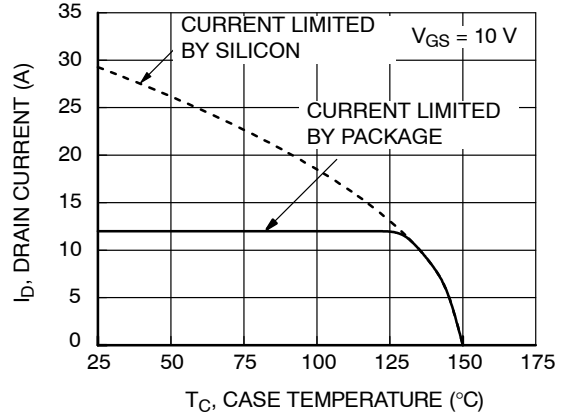


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

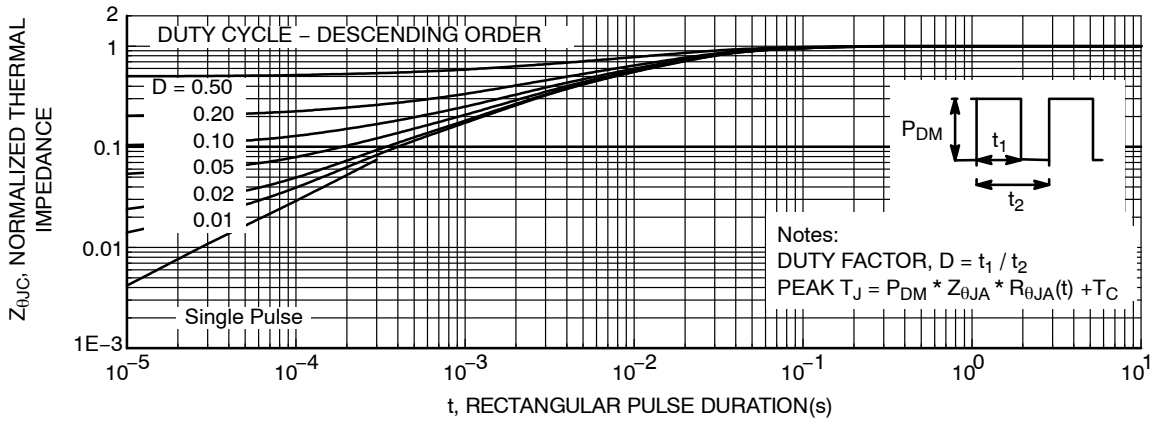


Figure 3. Normalized Maximum Transient Thermal Impedance

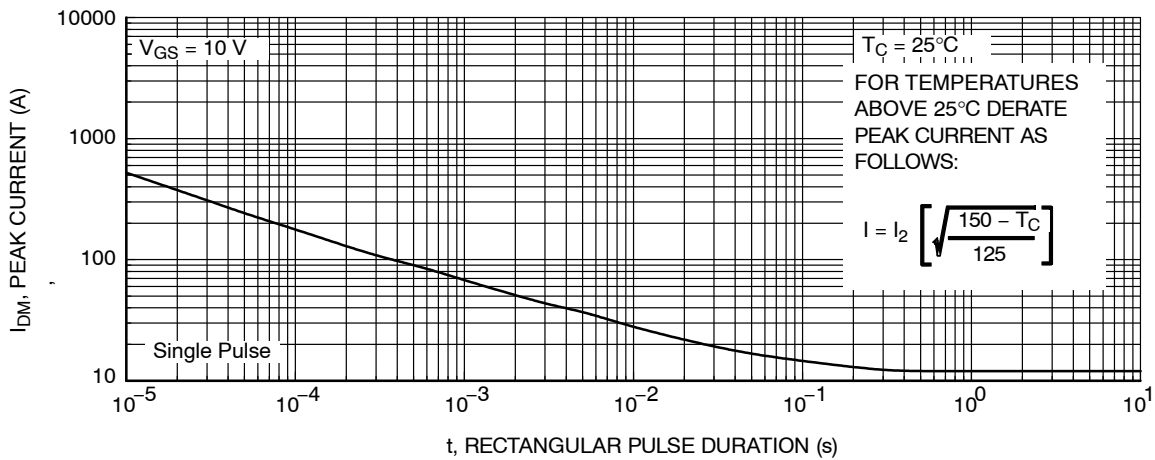


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

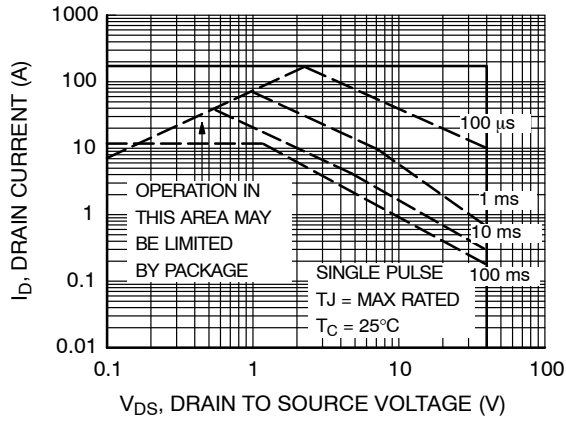
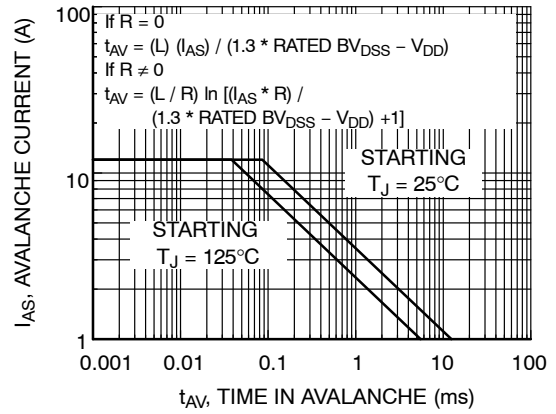


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to onsemi Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

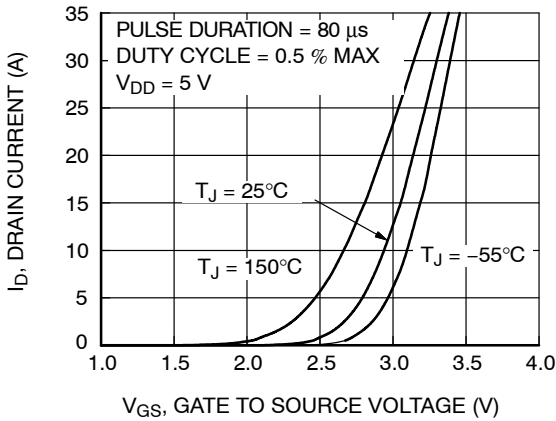


Figure 7. Transfer Characteristics

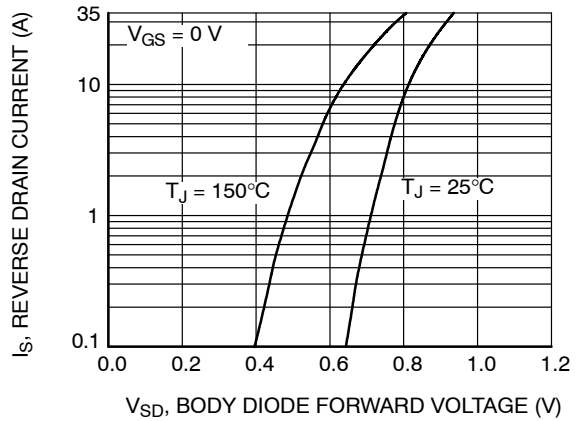


Figure 8. Forward Diode Characteristics

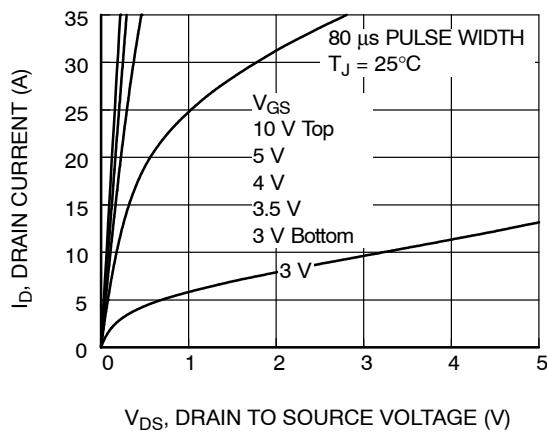


Figure 9. Saturation Characteristics

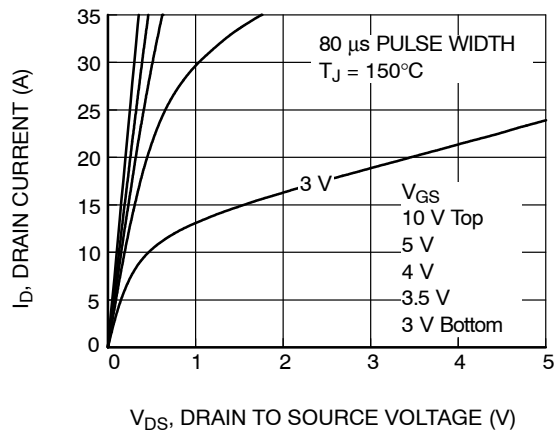


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

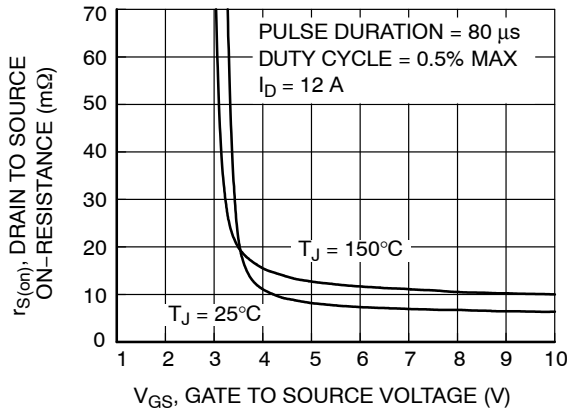


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

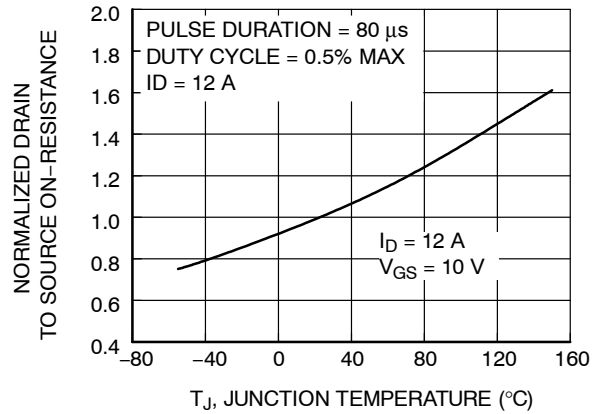


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

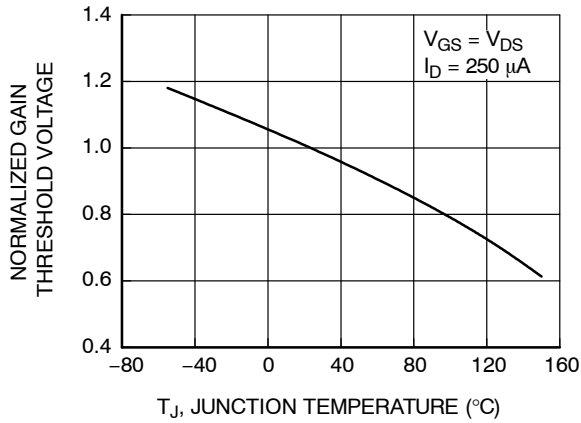


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

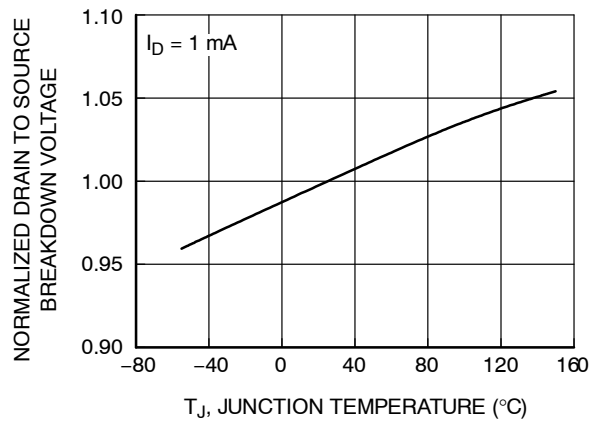


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

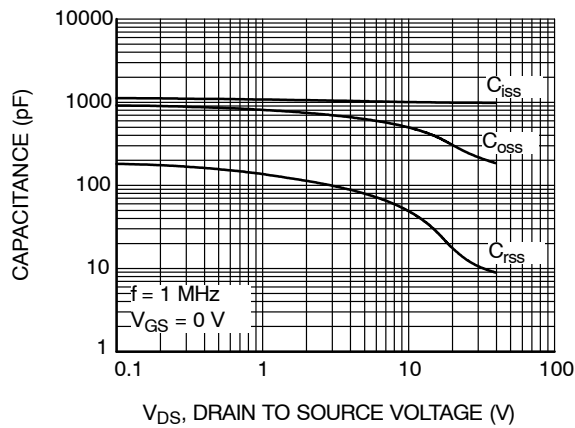


Figure 15. Capacitance vs. Drain-to-Source Voltage

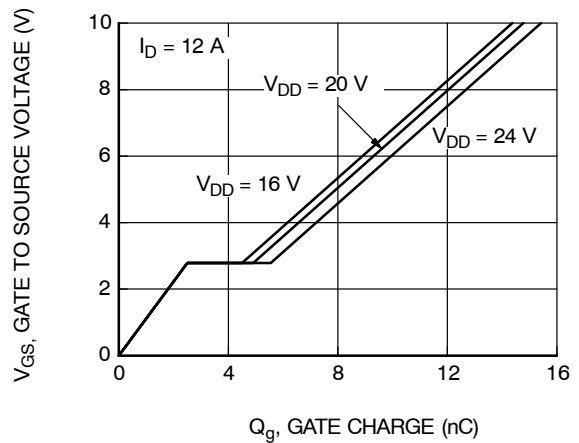
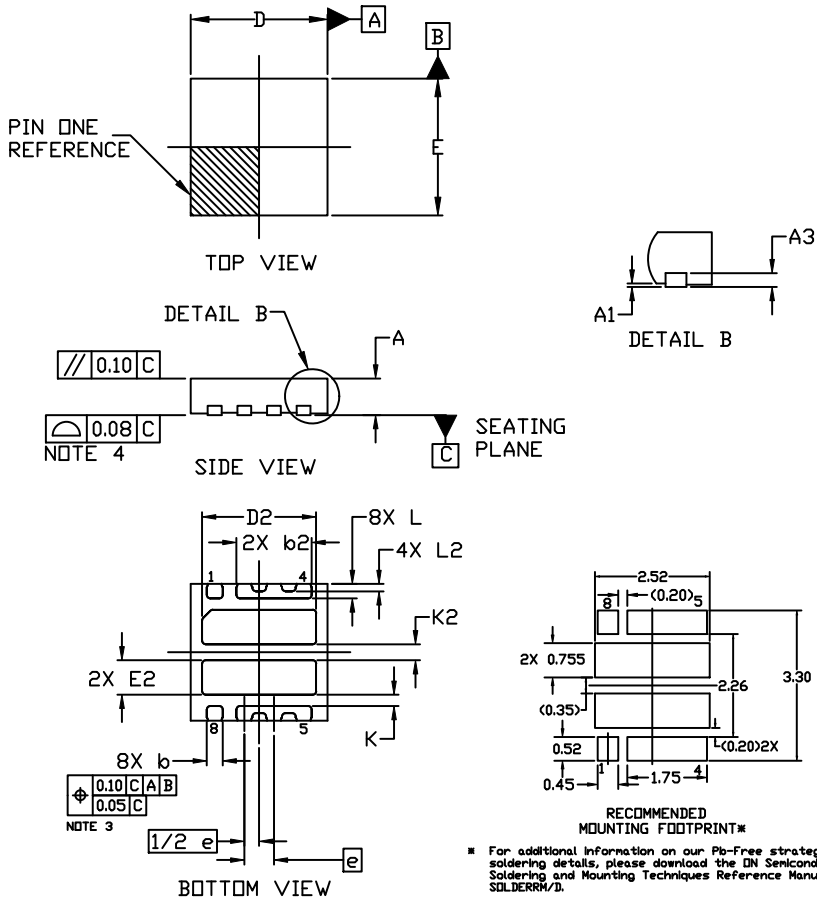


Figure 16. Gate Charge vs. Gate-to-Source Voltage

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**WDFN8 3x3, 0.65P**  
**CASE 511DG**  
**ISSUE A**

DATE 12 FEB 2019

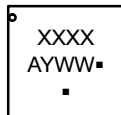


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
<i>b</i>	0.30	0.35	0.40
<i>b</i> 2	1.65 REF		
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
<i>e</i>	0.65 BSC		
K	0.25	---	---
K2	0.35 REF		
L	0.27	0.32	0.37
L2	0.163 REF		

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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