

Feature	MitySOM-AM62	MitySOM-C10L	MitySOM-AM57(F) ⁷	MityDSP-L138F-A7 ⁷	MitySOM-A10S	MitySOM-5CSX	MitySOM-335x	MityDSP-L138(F) ⁷	MityDSP-6455F	MityDSP-6711F
DSP Processor	None	None	Up to 2 C66x	C674x	None	None	None	C674x	C6454 / 55 ⁵	C6711
Max Speed	---	---	750 MHz	456 MHz	---	---	---	456 MHz	1200 MHz	200 MHz
L1 Program Cache	---	---	32 KB (per core)	32 KB	---	---	---	32 KB	32 KB	4 KB
L1 Data Cache	---	---	32 KB (per core)	32 KB	---	---	---	32 KB	32 KB	4 KB
Internal RAM	---	---	288 KB	256 KB	---	---	---	256 KB	2048 KB	64 KB
ARM Processor	Cortex-A53	NIOS II Softcore	Cortex-A15	ARM926EJ-S	Cortex-A9	Cortex-A9	Cortex-A8	ARM926EJ-S	None	None
Cores	Quad	N/A	Dual	Single	Dual	Single/Dual	Single	Single	---	---
Max Speed	1400 MHz	---	1500 MHz	456 MHz	1500 MHz	925 MHz	1000 MHz	456 MHz	---	---
L1 Program Cache	32 KB	---	32 KB (per core)	16 KB	32 KB (per core)	32 KB (per core)	32 KB	16 KB	---	---
L1 Data Cache	32 KB	---	32 KB (per core)	16 KB	32 KB (per core)	32 KB (per core)	32 KB	16 KB	---	---
L2 Cache	512 KB	---	2 MB (shared)	256 KB	512 KB (shared)	512 KB (shared)	256 KB	256 KB	---	---
Internal RAM	---	---	2.5 MB	8 KB	256 KB	64 KB	64 KB	8 KB	---	---
FPGA	None	Cyclone 10 LP	Artix-7 XC7A50T or XC7A15T	Artix-7 XC7A50T or XC7A15T	Arria 10SX	Cyclone V SoC	None	XC6SLX45 or XC6SLX16 (optional) ⁴	X3CS4000 or X3CS2000	XC3S400 or XC3S1000
Slices	---	up to 81,264 LE	up to 52,160 LE	up to 52,160 LE	up to 480,000 LE	up to 110,000 LE	---	up to 6,822	up to 27648	up to 7680
Logic Cells	---	---	up to 8150 ALM	up to 8150 ALM	up to 183,590 ALM	up to 41,509 ALM	---	up to 43,661	up to 62208	up to 17280
Block RAM	---	up to 2,745Kb	up to 2.7Mb MLAB	up to 2.7Mb MLAB	up to 4.2Mb MLAB	up to 621Kb MLABs	---	up to 2,088 Kb	up to 1,728 Kb	up to 432 Kb
Memory										
Max CPU RAM	4 GB DDR4	32MB HyperRAM	4 GB DDR3	256 MB DDR2	6 GB DDR4	4 GB DDR3	1 GB	256 MB	128 MB	up to 32 MB
CPU RAM Throughput	3.2 GB/sec	200 MB/sec	up to 5.3 GB/sec	600 MB/sec	8.5 GB/sec	TBD	800 MB/sec	532 MB/sec	2000 MB/sec	400 MB/sec
Max NOR FLASH	256 MB	32 MB	32 MB	16 MB	---	48 MB	8 M	8 M	16 M	up to 16 MB
Max NAND FLASH	128 GB	---	N/A	512 MB	8 GB	---	1 GB	512 MB	None	None
Max FPGA RAM	---	---	N/A	N/A	2 GB	512 MB	---	N/A	64 M	up to 32 M ¹
FPGA RAM Throughput	---	---	N/A	N/A	4.26 GB/sec	TBD	---	N/A	400 MB/sec	400 MB/sec
Interface	SO-DIMM DDR4	SO-DIMM DDR4		SO-DIMM-200		MXM 3.0 Type	SO-DIMM-204	SO-DIMM-200	SO-DIMM-200	SO-DIMM-144
Required Voltage	3.3V	5V	5V	3.3V	5V or 12V	5V	3.3V - 5V	3.3V	3.3V	3.3V, 2.5V, 1.23V
Avail FPGA I/O	---	up to 192	up to 96	96	up to 168	up to 137	---	88	140	100
Peripherals										
Ethernet MAC	2 x 10/100/1000	N/A	2 x PRU 10/100, 2 x 10/100/1000	10/100	3 x 10/100/1000	2 x 10/100/1000	2 x 10/100/1000	10/100	10/100/1000	0 ³
McBSP Ports	N/A	N/A	N/A	2	N/A	N/A	N/A	2	2	2
LCD	2	N/A	1	1	N/A	N/A	1	1	N/A	0 ²
VPIF	N/A	N/A	N/A	1	N/A	N/A	N/A	1	N/A	N/A
MMC/SD	2	N/A	3	1	1	1	3	1	0 ⁶	0 ⁶
SATA	N/A	N/A	1	1	N/A	N/A	N/A	1	N/A	N/A
I2C	3	N/A	3	2 ⁶	5	4	2	2 ⁶	1 ⁶	0 ⁶
SPI	3	N/A	3	2 ⁶	2 Master/2 Slave	2	2	2 ⁶	0 ⁶	0 ⁶
USB	2	N/A	1 x 2.0; 1 x 3.0	2	1	2	2	2	0 ⁶	0 ⁶
UARTS	7	N/A	10	3 ⁶	2	2	6	3 ⁶	1 ⁶	1 ⁶
CAN	3	N/A	2	N/A	N/A	2	2	N/A	N/A	N/A
PCIe	N/A	N/A	N/A	N/A	PCIe x 8	PCIe x4	N/A	N/A	N/A	N/A
Transceivers	N/A	N/A	2	N/A	12 x 11.3 Gbps	6 x 3.125 Gbps	N/A	N/A	N/A	N/A
Availability	Production 2023	Production 2023	In Production	Production 2023	In Production	In Production	In Production	In Production	In Production	In Production
Introduction Date	2022	2022	2020	2022	2018	2013	2012	2010	2006	2004

Notes:

1. FPGA and CPU share RAM via DSP EMIF, 100 MHz clock rate maximum.
2. LCD interface core is available for the FPGA to drive local and remote LCD display.
3. Soft FPGA MAC cores are available for 10/100 Mbit Ethernet Phy Control.
4. Spartan-6 features a 6 input LUT allowing for significantly more logic in the same number of slices when compared to a Spartan-3.
5. TMS6455 Option Including 8 Rocket I/O ports is available upon request.
6. The listed peripheral interfaces are available from the DSP/ARM. Additional interfaces can be created in modules with FPGA's.
7. These modules are available with or without the FPGA.

