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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2014

FDA16N50LDTU

N-Channel UniFET^{TM} MOSFET

500 V, 16.5 A, 380 mΩ

Features

- $R_{DS(on)}$ = 310 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 8.3 A
- Low Gate Charge (Typ. 32 nC)
- Low C_{rss} (Typ. 20 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- PDP TV
- Uninterruptible Power Supply

Description

UniFET^{TM} MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-3PN
(L-forming)
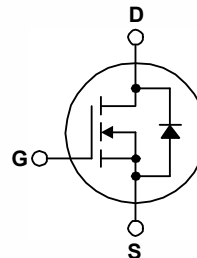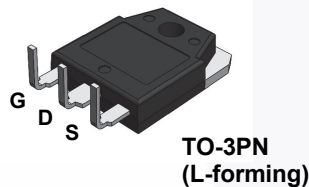
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDA16N50LDTU	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		16.5	A
		- Continuous (T_C = 100°C)		9.9	
I_{DM}	Drain Current	- Pulsed	(Note 1)	66	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	780	mJ
I_{AR}	Avalanche Current		(Note 1)	16.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	20.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		205	W
		- Derate Above 25°C		2.1	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	^{o}C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	^{o}C

Thermal Characteristics

Symbol	Parameter	FDA16N50LDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	^{o}C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA16N50LDTU	FDA16N50	TO-3PN (L-forming)	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250~\mu A$, $V_{GS} = 0$ V, $T_J = 25^oC$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250~\mu A$, Referenced to 25^oC	-	0.50	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500$ V, $V_{GS} = 0$ V	-	-	20	μA
		$V_{DS} = 500$ V, $T_C = 125^oC$	-	-	200	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30$ V, $V_{DS} = 0$ V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250~\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10$ V, $I_D = 8.3$ A	-	0.31	0.38	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40$ V, $I_D = 8.3$ A	-	23	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1 MHz	-	1495	1945	pF
C_{oss}	Output Capacitance		-	235	310	pF
C_{rss}	Reverse Transfer Capacitance		-	20	30	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400$ V, $I_D = 16$ A, $V_{GS} = 10$ V	-	32	45	nC
Q_{gs}	Gate to Source Gate Charge		-	8.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	14	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250$ V, $I_D = 16$ A, $V_{GS} = 10$ V, $R_G = 25~\Omega$	-	40	90	ns
t_r	Turn-On Rise Time		-	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		-	65	140	ns
t_f	Turn-Off Fall Time	(Note 4)	-	80	170	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	16.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	66	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_{SD} = 16.5$ A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_{SD} = 16$ A, $dI_F/dt = 100$ A/μs	-	490	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.0	-	μC

Notes:
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 5.1 mH, I_{AS} = 16.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 16.5 A, di/dt ≤ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical Characteristics

Typical Performance Characteristics
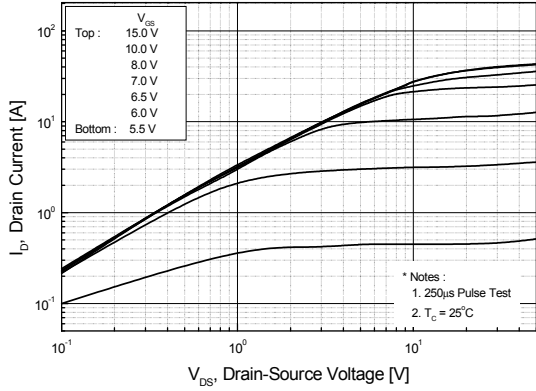
Figure 1. On-Region Characteristics

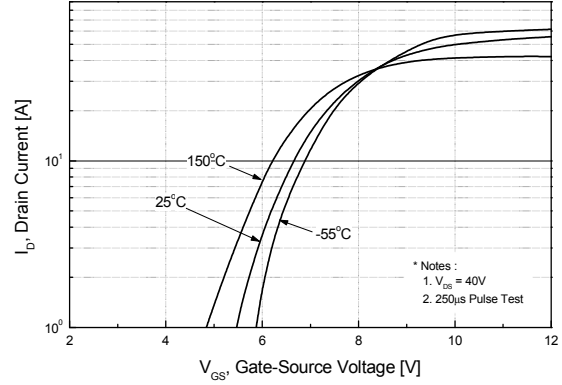### Figure 2. Transfer Characteristics

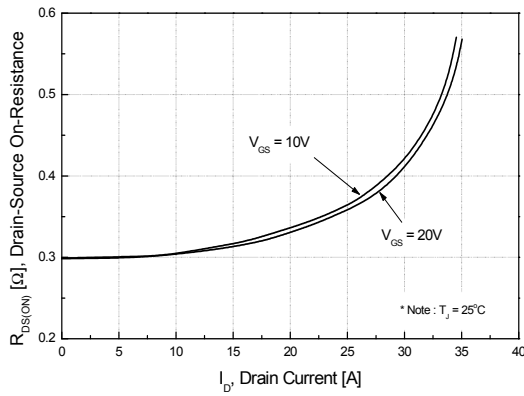### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue
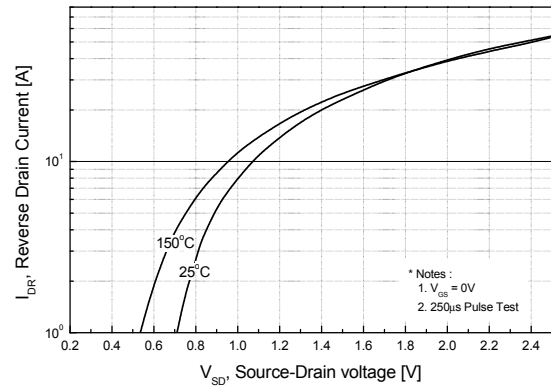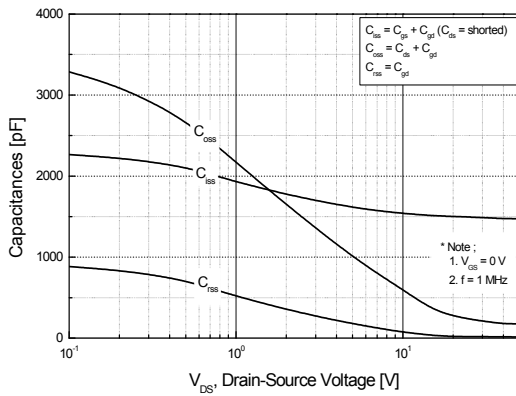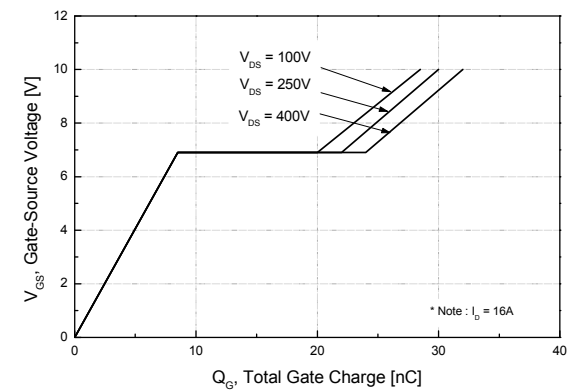

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Performance Characteristics (Continued)
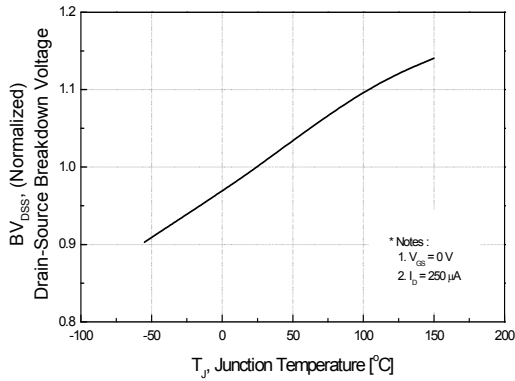
Figure 7. Breakdown Voltage Variation vs. Temperature

* Notes :
1. V_{GS} = 0 V
2. I_D = 250 µA

Figure 8. On-Resistance Variation vs. Temperature

* Notes :
1. V_{GS} = 10 V
2. I_D = 8.3 A
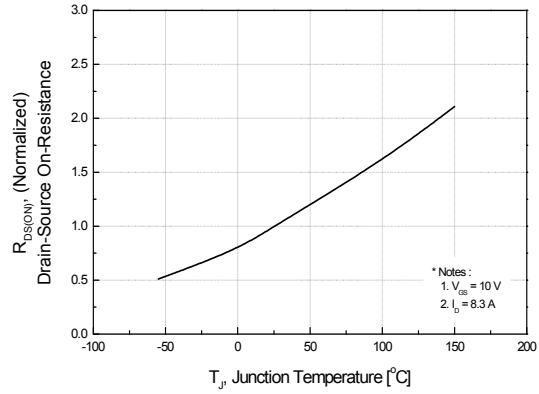
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

10 µs
100 µs
1 ms
10 ms
100 ms
DC

* Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse
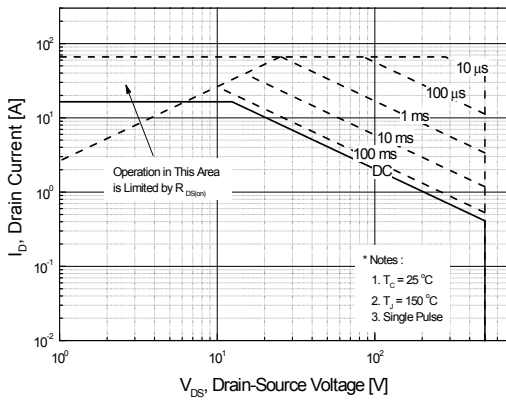
Figure 10. Maximum Drain Current vs. Case Temperature
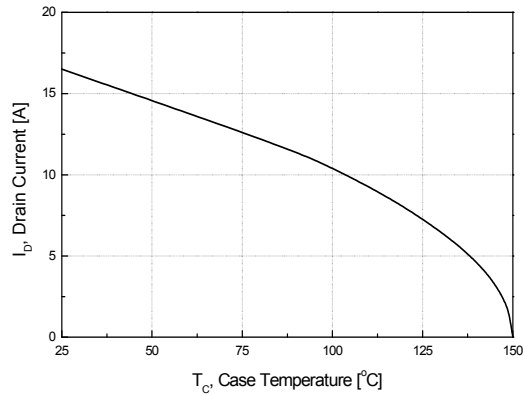
Figure 11. Transient Thermal Response Curve

single pulse

* Notes :
1. $Z_{θJC}(t)$ = 0.6 °C/W Max.
2. Duty Factor, D = t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{θJC}(t)$
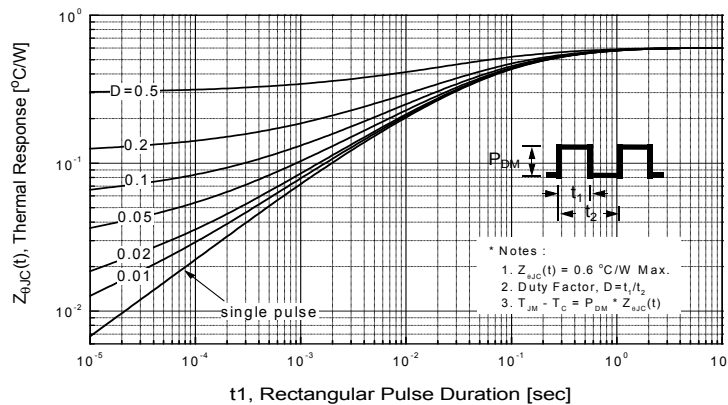
Figure 12. Gate Charge Test Circuit & Waveform
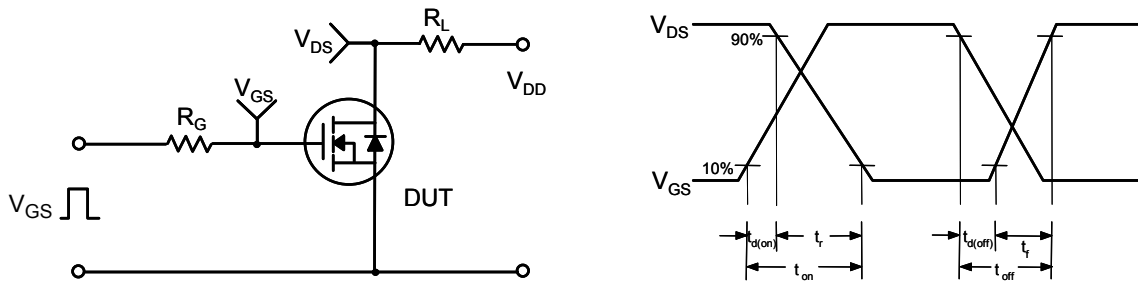
Figure 13. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \quad \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$
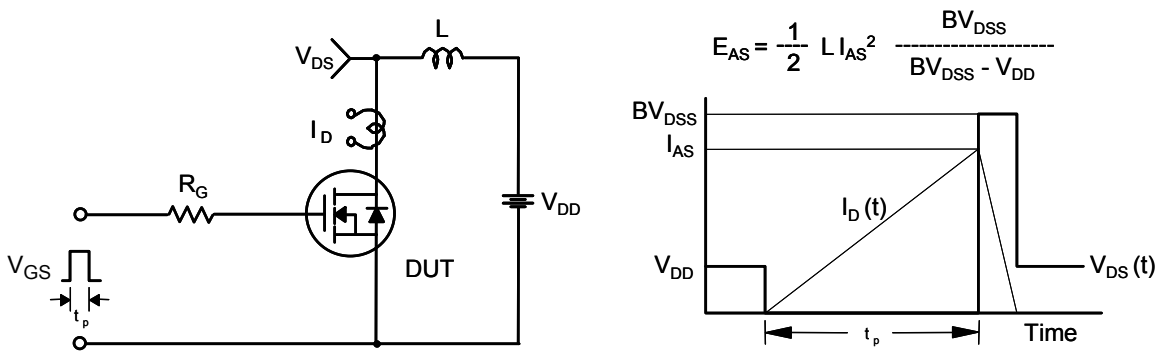
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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DUT

V$_{DS}$

+

−

I$_{SD}$

L

Driver

R$_G$

Same Type
as DUT

V$_{DD}$

V$_{GS}$

• dv/dt controlled by R$_G$
• I$_{SD}$ controlled by pulse period

V$_{GS}$
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I$_{SD}$
(DUT)

I$_{FM}$, Body Diode Forward Current

di/dt

I$_{RM}$

Body Diode Reverse Current

V$_{DS}$
(DUT)

Body Diode Recovery dv/dt

V$_{SD}$

V$_{DD}$

Body Diode
Forward Voltage Drop

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

5.00
4.60

1.65
1.45

16.20
15.40

5.20
4.80

3°

13.80
13.40

∅ 3.30
3.10

20.10
19.70

18.90
18.50

16.96
16.56

∅ 7.20
6.80

1

3

⚠E 4.45
3.95

(1.85)

3.70
3.30

3°

2.20
1.80

⚠E 5.25
4.75

4°

3.20
2.80

(R0.60)

1.20
0.80

⚠E 9.25
8.75

⊕ ∅ 0.55 Ⓜ

0.75
0.55

5.45

5.45

(R0.50)
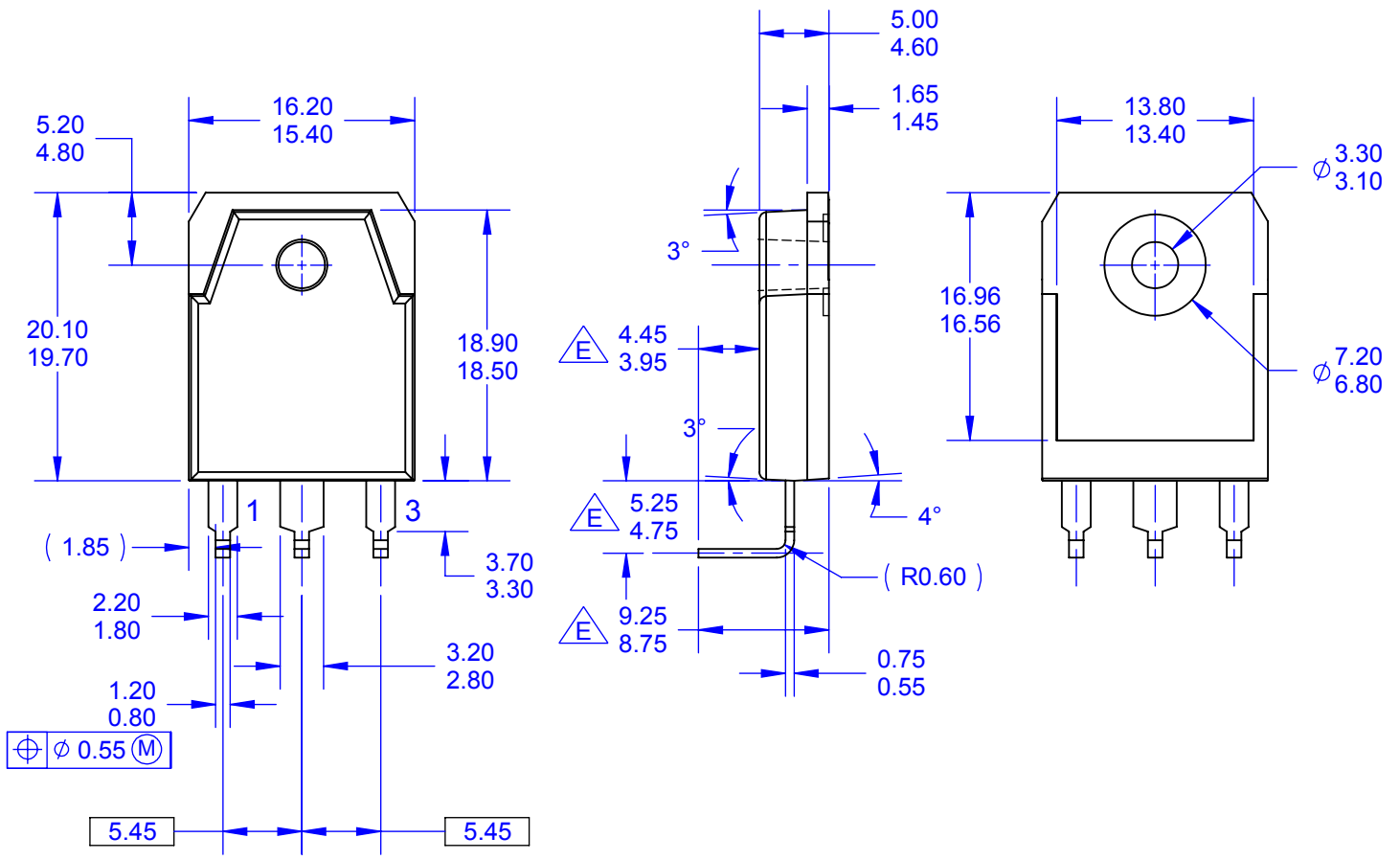
NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE REFERENCE EIAJ SC-65
     PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER
     ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS,
     MOLD FLASH, AND TIE BAR EXTRUSSIONS.

⚠E DOES NOT COMPLY EIAJ SC-65.

F) DRAWING FILE NAME: TO3PN03CREV1.
G) FAIRCHILD SEMICONDUCTOR.

PUBLICATION ORDERING INFORMATION