**Please note that Cypress is an Infineon Technologies Company.**
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

AN INFINEON TECHNOLOGIES COMPANY

# THIS SPEC IS OBSOLETE

Spec No: 002-08447

Spec Title: S6AP412A 3CH DC/DC CONVERTER WITH I2C INTERFACE AND INTERNAL SW FETS

Replaced by: None

# S6AP412A

# 3ch DC/DC Converter with I²C Interface and Internal SW FETs

S6AP412A contains 2ch buck DC/DC converter and 1ch buck-boost DC/DC converter. One of the buck DC/DC converter is available for Multi-phase method. Multi-phase DC/DC converter is possible to load high current until 4A. S6AP412A can supply the main power line in several systems by using only its chip. The current mode control is adopted for the DC/DC converter, and it is possible to use the small chip inductor with the high switching frequency operation which contains internal switching FETs. S6AP412A contains the output setting resistor and the phase compensation circuit, and contributes to reduce the number of external components and its mount area. Also it contains the CTL input pin which can control the ON/OFF for each DC/DC converter, the Power Good signal output pin and I²C communication interface, therefore it is easy to design the power supply sequence. It is possible to tune in the output voltage exactly using the I²C communication.



## Features

- Operating input voltage range: 2.5V to 5.5V (Maximum rating: 6.5V)
- Output voltage setting range: DD1*:0.7V to 1.32V (20mV/step)
  DD2*:1.2V to 1.95V (50mV/step)
  DD3*:2.8Vto 3.5V (100mV/step)
- Maximum output current: DD1:4A, DD2:1.2A, DD3:0.6A
- Internal switching FETs, output voltage setting resistor, phase compensation circuit and output discharge resistor (all DC/DC converters)
- Buck-boost DC/DC converter is seamless to change operation mode
- Soft start time setting range: 1 ms to 16 ms (approximately 1ms/step)
- Switching frequency for the DC/DC converter: 3 MHz
- Communication interface: I²C (ON/OFF, Output voltage, Soft start time)
- Internal PFM/PWM auto switching mode
- Each DC/DC converter Power Good function (open drain)
- Several protection functions: Under voltage lockout (UVLO), Over current protection (OCP), Thermal shut down (TSD)
- Small package: QFN32 (5mm × 5mm × 0.71mm, 0.5mm pitch)

*: DD1, DD2, DD3 : DC/DC converter block 1,2,3

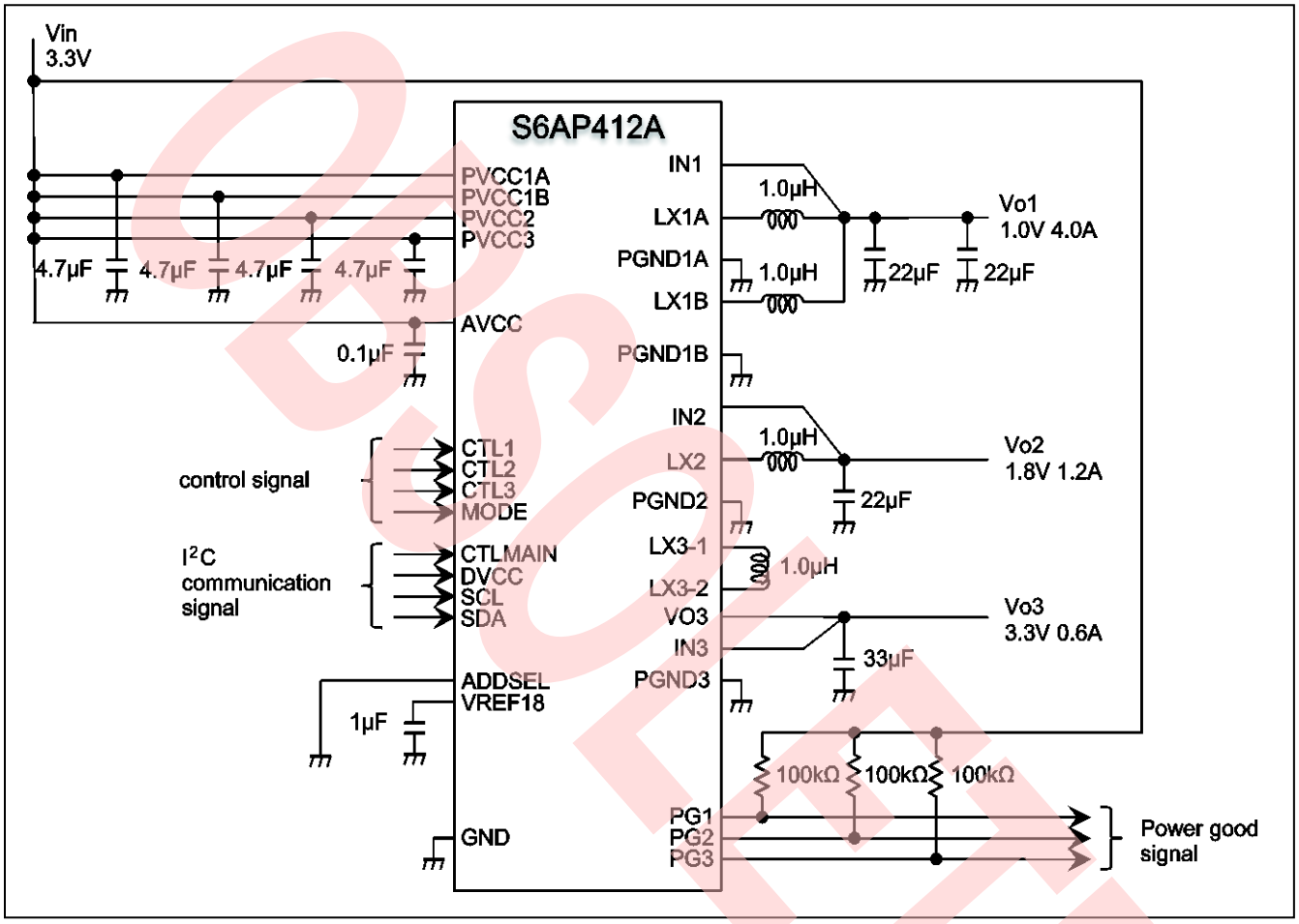
## Applications

Network equipment, Factory automation, Security system, Surveillance camera, Electrical music instrument, Multi-function printer, Scanner, Printer, Copy machine, Home appliances,Data storage (HDD, SSD), Mobile equipment for Li+ battery (1 cell)

# Contents

## 1. Application Circuit Example

**Figure 1. Application Circuit**



## 2. Recommended Application Specification

**[Input Voltage Range]**

| Input voltage Vin(V) | | |
|---|---|---|
| Min | Typ | Max |
| 2.5 | 3.3 | 5.5 |

**[Output specification]**

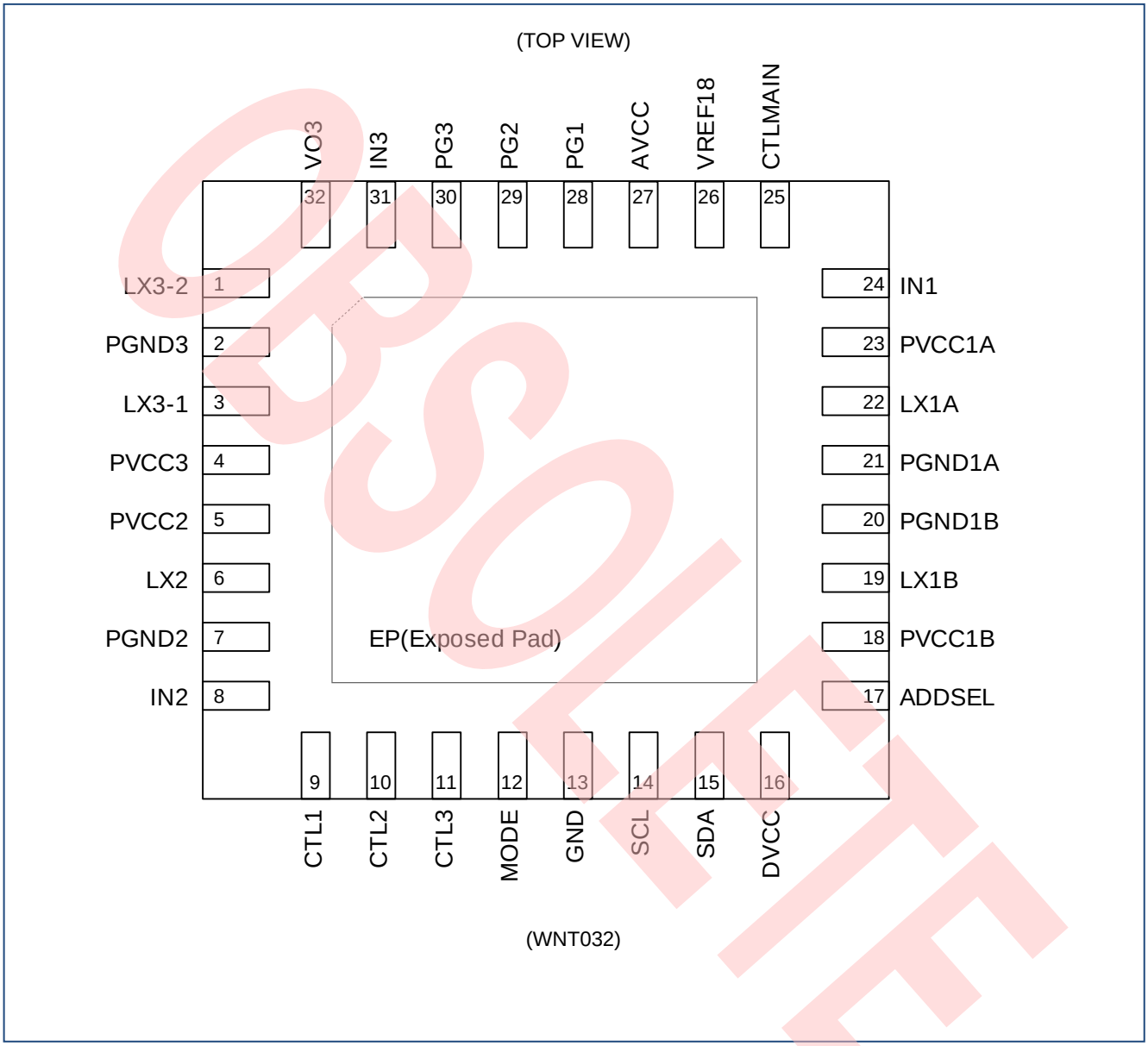
(Ta=+25°C)

| Channel | Symbol | Accuracy | Output Voltage (V) | | | Output Current(mA) | Limit Current(mA) | Mode | Switching Frequency (MHz) | Inductor(µH) | Output Capacitance (µF) | Soft-start Time (ms) | Discharge Resistance (kΩ) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Max | Min | | | | | | | |
| DD1 | VO1 | ±1.2% | 0.692 | 0.700 | 0.708 | 4000 | (4800) | Buck (synchronous rectification) Multi Phase C-mode | 3.0 | 1.0 | 22 | 1 to 16ms<br>At the time of 1.0V setting, the details are cf. Contents 17 | 5.0 | Multi PhaseBuilt-in SWFET Built-in output setting resistors Built-in phase compensation circuit |
| | | | 0.711 | 0.720 | 0.729 | | | | | | | | | |
| | | | 0.731 | 0.740 | 0.749 | | | | | | | | | |
| | | | 0.751 | 0.760 | 0.769 | | | | | | | | | |
| | | | 0.771 | 0.780 | 0.789 | | | | | | | | | |
| | | | 0.790 | 0.800 | 0.810 | | | | | | | | | |
| | | | 0.810 | 0.820 | 0.830 | | | | | | | | | |
| | | | 0.830 | 0.840 | 0.850 | | | | | | | | | |
| | | | 0.850 | 0.860 | 0.870 | | | | | | | | | |
| | | | 0.869 | 0.880 | 0.891 | | | | | | | | | |
| | | | 0.889 (*1) | 0.900 (*1) | 0.911 (*1) | | | | | | | | | |
| | | | 0.909 | 0.920 | 0.931 | | | | | | | | | |
| | | | 0.929 | 0.940 | 0.951 | | | | | | | | | |
| | | | 0.948 | 0.960 | 0.972 | | | | | | | | | |
| | | | 0.968 | 0.980 | 0.992 | | | | | | | | | |
| | | | 0.988 (*1) | 1.000 (*1) | 1.012 (*1) | | | | | | | | | |
| | | | 1.008 | 1.020 | 1.032 | | | | | | | | | |
| | | | 1.028 | 1.040 | 1.052 | | | | | | | | | |
| | | | 1.047 | 1.060 | 1.073 | | | | | | | | | |
| | | | 1.067 | 1.080 | 1.093 | | | | | | | | | |
| | | | 1.087 (*1) | 1.100 (*1) | 1.113 (*1) | | | | | | | | | |
| | | | 1.107 | 1.120 | 1.133 | | | | | | | | | |
| | | | 1.126 | 1.140 | 1.154 | | | | | | | | | |
| | | | 1.146 | 1.160 | 1.174 | | | | | | | | | |
| | | | 1.166 | 1.180 | 1.194 | | | | | | | | | |
| | | | 1.186 (*1) | 1.200 (*1) | 1.214 (*1) | | | | | | | | | |
| | | | 1.205 | 1.220 | 1.235 | | | | | | | | | |
| | | | 1.225 | 1.240 | 1.255 | | | | | | | | | |
| | | | 1.245 | 1.260 | 1.275 | | | | | | | | | |
| | | | 1.265 | 1.280 | 1.295 | | | | | | | | | |
| | | | 1.284 | 1.300 | 1.316 | | | | | | | | | |
| | | | 1.304 | 1.320 | 1.336 | | | | | | | | | |

| Channel | Symbol | Accuracy | Output Voltage (V) | | | Output Current(mA) | Limit Current(mA) | Mode | Switching frequency(MHz) | Inductor(µH) | Output Capacitance(µF) | Soft-start Time (ms) | Discharge Resistance (kΩ) | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Max | Min | | | | | | | |
| DD2 | VO2 | ±1.2% | 1.186 (*1) | 1.200 (*1) | 1.214 (*1) | 1200 | (1500) | Buck (synchronous rectification) C-mode | 3.0 | 1.0 | 10 | 1 to 16ms<br>At the time of 1.8V setting, the details are cf. Contents 17 | 5.0 | Built-in SWFET<br>Built-in output setting resistors<br>Built-in phase compensation circuit |
| | | | 1.235 | 1.250 | 1.265 | | | | | | | | | |
| | | | 1.284 | 1.300 | 1.316 | | | | | | | | | |
| | | | 1.334 (*1) | 1.350 (*1) | 1.366 (*1) | | | | | | | | | |
| | | | 1.383 | 1.400 | 1.417 | | | | | | | | | |
| | | | 1.433 | 1.450 | 1.467 | | | | | | | | | |
| | | | 1.482 (*1) | 1.500 (*1) | 1.518 (*1) | | | | | | | | | |
| | | | 1.531 | 1.550 | 1.569 | | | | | | | | | |
| | | | 1.581 | 1.600 | 1.619 | | | | | | | | | |
| | | | 1.630 | 1.650 | 1.670 | | | | | | | | | |
| | | | 1.680 | 1.700 | 1.720 | | | | | | | | | |
| | | | 1.729 | 1.750 | 1.771 | | | | | | | | | |
| | | | 1.778 (*1) | 1.800 (*1) | 1.822 (*1) | | | | | | | | | |
| | | | 1.828 | 1.850 | 1.872 | | | | | | | | | |
| | | | 1.877 | 1.900 | 1.923 | | | | | | | | | |
| | | | 1.927 | 1.950 | 1.973 | | | | | | | | | |
| DD3 | VO3 | ±1.8% | 2.74 (*1) | 2.80 (*1) | 2.86 (*1) | 600 | (750) | Buck-boost (synchronous rectification) C-mode | 3.0 | 1.0 | 22 | 1 to 16ms<br>At the time of 3.3V setting, the details are cf. Contents 17 | 5.0 | Built-in SWFET<br>Built-in output setting resistors<br>Built-in phase compensation circuit |
| | | | 2.84 | 2.90 | 2.96 | | | | | | | | | |
| | | | 2.94 (*1) | 3.00 (*1) | 3.06 (*1) | | | | | | | | | |
| | | | 3.04 | 3.10 | 3.16 | | | | | | | | | |
| | | | 3.14 | 3.20 | 3.26 | | | | | | | | | |
| | | | 3.23 (*1) | 3.30 (*1) | 3.37 (*1) | | | | | | | | | |
| | | | 3.33 | 3.40 | 3.47 | | | | | | | | | |
| | | | 3.43 (*1) | 3.50 (*1) | 3.57 (*1) | | | | | | | | | |

*1: default (It is selectable with the default output voltage)

## 3. Pin Configuration

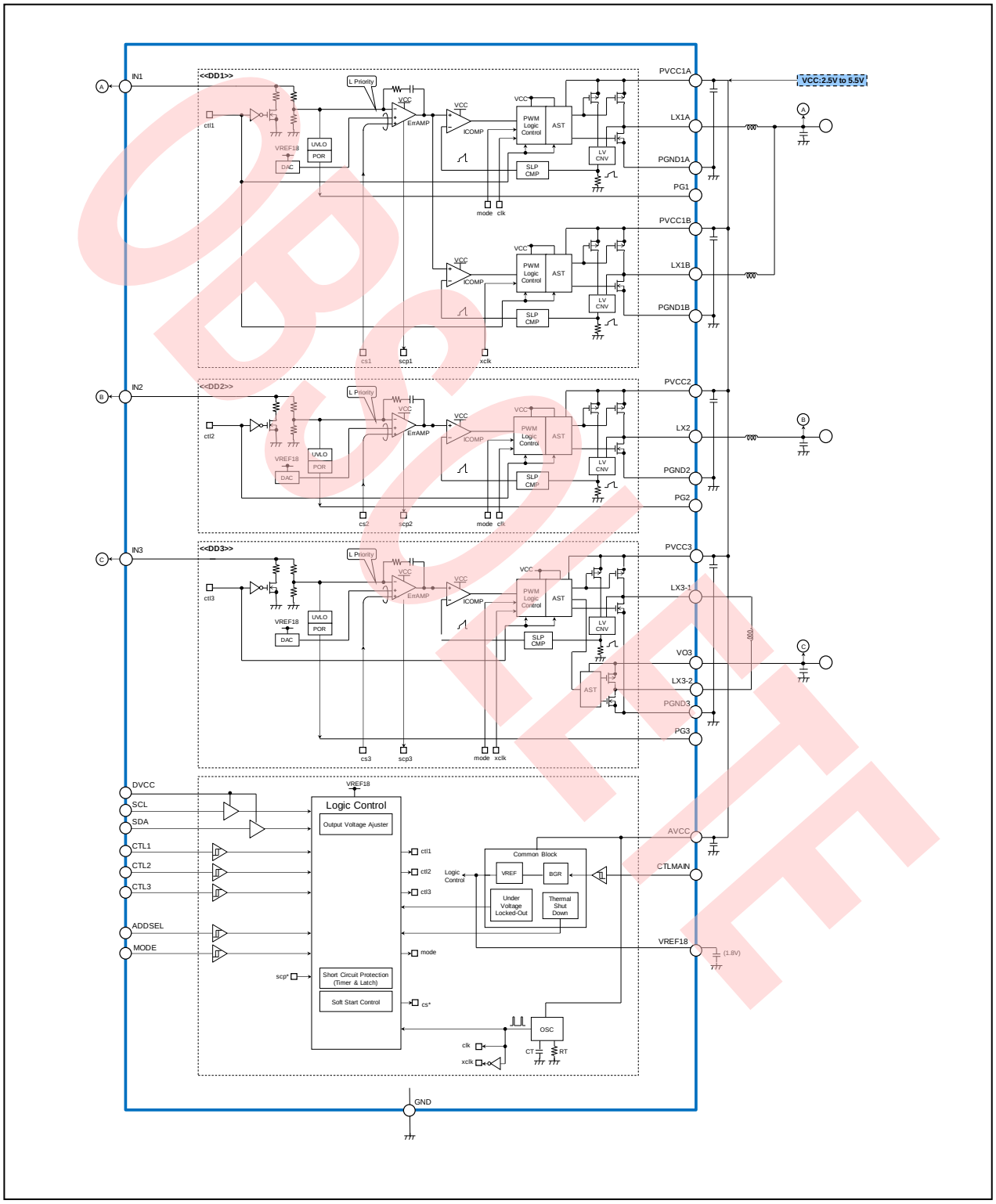


## 4. Pin Descriptions

| Block | Pin Name | Pin Number | I/O | Description | Pull-down Resistor | Unused DD1 | Unused DD2 | Unused DD3 | Unused $I^2C$ |
|---|---|---|---|---|---|---|---|---|---|
| DD1 Multi-phase | IN1 | 24 | I | DD1 output voltage feedback | - | GND | - | - | - |
| | PVCC1A | 23 | - | DD1 Phase1 output block power supply | - | AVCC | - | - | - |
| | LX1A | 22 | O | DD1 Phase1 inductor connection | - | Open | - | - | - |
| | PG1 | 28 | O | DD1 Power Good output | - | GND | - | - | - |
| | PGND1A | 21 | - | DD1 Phase1 output block ground | - | GND | - | - | - |
| | PVCC1B | 18 | - | DD1 Phase2 output block power supply | - | AVCC | - | - | - |
| | LX1B | 19 | O | DD1 Phase2 inductor connection | - | Open | - | - | - |
| | PGND1B | 20 | - | DD1 Phase2 output block ground | - | GND | - | - | - |
| DD2 Buck | IN2 | 8 | I | DD2 output voltage feedback | - | - | GND | - | - |
| | PVCC2 | 5 | - | DD2 output block power supply | - | - | AVCC | - | - |
| | LX2 | 6 | O | DD2 inductor connection | - | - | Open | - | - |
| | PG2 | 29 | O | DD2 Power Good output | - | - | GND | - | - |
| | PGND2 | 7 | - | DD2 output block ground | - | - | GND | - | - |
| DD3 Buck-boost | IN3 | 31 | I | DD3 output voltage feedback | - | - | - | GND | - |
| | PVCC3 | 4 | - | Power supply for DD3 output block | - | - | - | AVCC | - |
| | VO3 | 32 | O | Output voltage for DD3 | - | - | - | GND | - |
| | LX3-1 | 3 | O | DD3 inductor connection1 | - | - | - | Open | - |
| | LX3-2 | 1 | O | DD3 inductor connection2 | - | - | - | Open | - |
| | PG3 | 30 | O | Output for DD3 Power Good | - | - | - | GND | - |
| | PGND3 | 2 | - | Ground for DD3 output block | - | - | - | GND | - |
| CTL | CTLMAIN | 25 | I | Control for reference voltage output | Exist | - | - | - | - |
| | CTL1 | 9 | I | DD1 control | Exist | Open | - | - | - |
| | CTL2 | 10 | I | DD2 control | Exist | - | Open | - | - |
| | CTL3 | 11 | I | DD3 control | Exist | - | - | Open | - |
| $I^2C$ | DVCC | 16 | I | Power supply for $I^2C$ communication | - | - | - | - | GND |
| | SCL | 14 | I | Clock for $I^2C$ communication | - | - | - | - | Open |
| | SDA | 15 | I/O | Data for $I^2C$ communication | Exist | - | - | - | Open |
| | ADDSEL | 17 | I | Switch for slave address | - | - | - | - | Open |

| Block | Pin Name | Pin Number | I/O | Description | Pull-down Resistor | Unused DD1 | Unused DD2 | Unused DD3 | Unused I²C |
|---|---|---|---|---|---|---|---|---|---|
| Reference control | AVCC | 27 | - | Power supply for reference voltage | - | - | - | - | - |
| | MODE | 12 | I | Select for DC/DC converter operation mode (H: PFM/PWM mode, L=PWM mode, common for all DCDC converter ) | Exist | - | - | - | - |
| | VREF18 | 26 | O | Output reference voltage | - | - | - | - | - |
| | GND | 13 | - | Ground for reference voltage | - | - | - | - | - |
| | GND | EP | - | Ground for reference voltage | - | - | - | - | - |

## 5. Block Diagram



## 6. Absolute Maximum Ratings

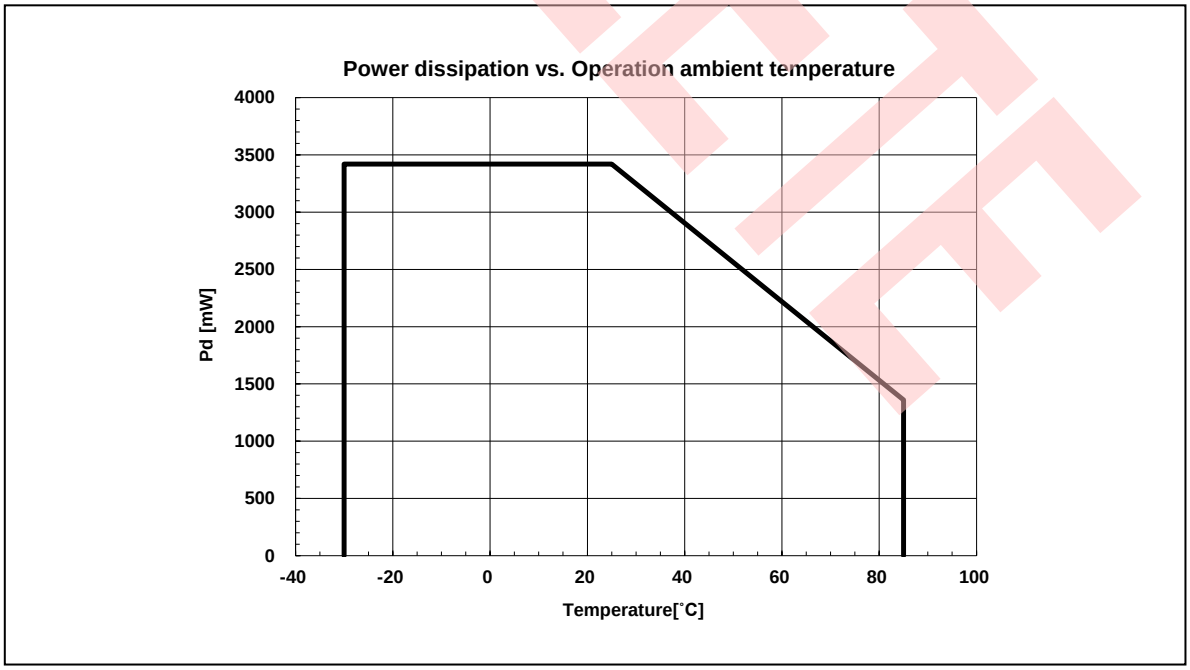
| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power supply voltage | $V_{VCC1}$ | AVCC,PVCC input voltage | -0.3 | 6.5 | V |
| | $V_{VCC2}$ | DVCC input voltage | -0.3 | 6.5 | V |
| Terminal voltage | $V_{CTL1}$ | CTL1,CTL 2,CTL3 input voltage | -0.3 | 6.5 | V |
| | $V_{CTL2}$ | CTLMAIN input voltage | -0.3 | 6.5 | V |
| | $V_{MODE}$ | MODE input voltage | -0.3 | 6.5 | V |
| | $V_{LOGIC}$ | SDA,SCL input voltage | -0.3 | 6.5 | V |
| | $V_{ADD}$ | ADDSEL input voltage | -0.3 | 6.5 | V |
| | $V_{PG}$ | PG1, PG2, PG3 drain voltage | -0.3 | 6.5 | V |
| | $V_{OUT}$ | IN1, IN2, IN3 input voltage | -0.3 | 6.5 | V |
| LX voltage | $V_{LX}$ | LX1, LX2, LX3 voltage | -1.0 | 6.5 | V |
| Permission loss | $P_D$ | Ta≤+25°C<br>Thermal resistance (θja): (29.2°C /W(*1)) | 0 | 3420 | mW |
| Maximum junction temperature | $T_{jmax}$ | - | - | +125 | °C |
| Storage temperature | $T_{STG}$ | - | -55 | +125 | °C |

*1: When the IC is mounted on 74mm × 74mm four-layer square epoxy board. IC is mounted on a four-layer epoxy board, which terminal bias, and the IC's thermal pad is connected to the epoxy board.

**WARNING:**

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

**Figure 2. Power Dissipation vs. Operation Ambient Temperature**



## 7. Recommended Operating Conditions

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 1. Reference control block | | | | | | |
| Power supply voltage | $V_{VCC}$ | AVCC | 2.5 | 3.3 | 5.5 | V |
| Output current for reference voltage | $I_{REF}$ | VREF18 | -1 | - | 0 | mA |
| Operating temperature | $T_a$ | - | -30 | +25 | +85 | °C |
| 2. DC/DC channel | | | | | | |
| Power supply voltage | $V_{VCC}$ | PVCC1, PVCC2, PVCC3 | 2.5 | 3.3 | 5.5 | V |
| Input voltage | $V_{OUT}$ | IN1,IN2 | 0 | - | AVCC | V |
| Input voltage | $V_{OUT}$ | IN3 | 0 | - | 5.5 | V |
| PG input voltage | $V_{PG}$ | PG1, PG2, PG3 | 0 | - | 5.5 | V |
| 3. Input block | | | | | | |
| Input voltage | $V_{CTL}$<br>$V_{MODE}$ | CTL1, CTL 2, CTL3, MODE<br>CTLMAIN | 0 | - | AVCC | V |
| 4. $I^2C$ communication block | | | | | | |
| Power supply voltage | $V_{VCC}$ | DVCC | 1.70 | - | 3.50 | V |
| Input voltage | $V_{LOGIC}$ | SDA,SCL | 0 | - | DVCC | V |
| Input voltage | $V_{ADD}$ | ADDSEL | 0 | - | AVCC | V |

**WARNING:**

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

# 8. Electrical Characteristics

## 8.1 Reference Control Block

(AVCC = PVCC1A=PVCC1B=PVCC2=PVCC3 = 3.3V, supply, PGND1A=PGND1B=PGND2=PGND3=GND=0V. Ta = +25°C, unless otherwise noted. )

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 1. Reference voltage | | [ VREF18 ] | | | | |
| Output voltage | $V_{VREF1}$ | VREF18 pin = 0mA | 1.773 | 1.800 | 1.827 | V |
| | $V_{VREF2}$ | AVCC pin = 2.5V to 5.5V<br>VREF18 pin = 0mA | 1.768 | 1.800 | 1.832 | V |
| | $V_{VREF3}$ | VREF18 pin = 0mA to -1mA | 1.768 | 1.800 | 1.832 | V |
| 2. Under voltage lockout | | [ VCC UVLO ] | | | | |
| Threshold voltage | $V_{TH}$ | AVCC rising | 2.156 | 2.20 | 2.244 | V |
| Hysteresis width | $V_H$ | - | - | 0.20(*1) | - | V |
| 3. Over current protection | | [ OCP ] | | | | |
| Timer | $t_{OCP1}$ | DD1, DD2, DD3 | 0.9 | 1 | 1.1 | ms |
| 4. Thermal shut down | | [ TSD ] | | | | |
| Stop temperature | $T_{TSDH}$ | - | 125(*2) | 150 | - | °C |
| 5. Input block (CTL,MODE,CTLMAIN) | | [ CTL,MODE,CTLMAIN ] | | | | |
| Input voltage | $V_{IH}$ | CTL1, CTL2, CTL3,MODE pin<br>CTLMAIN pin | AVCC ×0.7 | - | AVCC | V |
| Input voltage | $V_{IL}$ | CTL1, CTL2, CTL3,MODE pin<br>CTLMAIN pin | 0 | - | 0.4 | V |
| Input current | $I_{CTLH}$<br>$I_{MODEH}$ | CTL1, CTL2, CTL3,MODE pin = 3.3V<br>CTLMAIN pin = 3.3V | 2.5 | 3.3 | 4.7 | µA |
| | $I_{CTLL}$<br>$I_{MODEL}$ | CTL1, CTL2, CTL3,MODE pin = 0V<br>CTLMAIN pin = 0V | - | - | 1 | µA |
| Input pull-down resistor | $R_P$ | CTL1, CTL2, CTL3,MODE pin<br>CTLMAIN pin | - | 1(*1) | - | MΩ |
| 6. Consumption current (DC/DC converter block) | | | | | | |
| Power supply current | $I_{VCCS1}$ | CTL1, CTL2, CTL3 pin = 0V<br>CTLMAIN pin = 0V | - | 0 | 1.0 | µA |
| | $I_{VCCS2}$ | CTL1, CTL2, CTL3 pin = 0V<br>CTLMAIN pin =3.3V | - | 30 | 45 | µA |
| | $I_{VCC}$ | DD1,DD2,DD3=ON,MODE=3.3V,<br>All DD are 0mA<br>(operation mode: PFM/PWM mode) | - | 430 | 630 | µA |
| | $I_{VCC}$ | DD1,DD2,DD3=ON,MODE=0V<br>All DD are 0mA<br>(operation mode: Fixed PWM mode) | - | 18 | 27 | mA |

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

### 8.2 DD1

AVCC = PVCC1A=PVCC1B=PVCC2=PVCC3 = 3.3V, supply,
PGND1A=PGND1B=PGND2=PGND3=GND=0V. Ta = +25°C, unless otherwise noted. )

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 1. DC/DC converter block | | [ DD1 ] | | | | |
| Output voltage | $V_{OUT}$ | IOUT = -10mA,<br>Output voltage setting: 1.0V | 0.988 | 1.000 | 1.012 | V |
| Input stability | $V_{LINE}$ | IOUT = -10mA,<br>PVCC1= 2.5V to 5.5V | -5 | - | +5 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -4000mA<br>(Fixed PWM mode) | -10 | - | +10 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -4000mA<br>(PFM/PWM mode) | -10 | - | +15 | mV |
| IN1 input impedance | $R_{IN}$ | IN1 = 2.0V | - | 190(*1) | - | kΩ |
| SW PMOS-Tr<br>on resistance | $R_{PMOS}$ | LX1A,1B = -30mA | - | 120(*1) | - | mΩ |
| SW NMOS-Tr<br>on resistance | $R_{NMOS}$ | LX1A,1B = 30mA | - | 80(*1) | - | mΩ |
| SW PMOS-Tr<br>leakage current | $I_{LEAK}$ | LX1A,1B = 0V | -3 | - | - | µA |
| SW NMOS-Tr<br>Leakage current | $I_{LEAK}$ | LX1A,1B = 3.3V | - | - | 3 | µA |
| Over current<br>protection value | $I_{LIMIT}$ | L=1.0µH | 4900(*2) | - | - | mA |
| PFM/PWM mode<br>changeover current | $I_{PFM}$ | L=1.0µH | - | 100(*1) | - | mA |
| Discharge resistor | $R_{DIS}$ | - | - | 5(*1) | - | kΩ |
| Soft start time | Tss | Soft start time setting: 1ms | 0.9 | 1 | 1.1 | ms |
| Switching frequency | $f_{OSC}$ | - | 2.7 | 3.0 | 3.3 | MHz |

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

### 8.3 DD2

(AVCC = PVCC1A=PVCC1B=PVCC2=PVCC3 = 3.3V, supply, PGND1A=PGND1B=PGND2=PGND3=GND=0V. Ta = +25°C, unless otherwise noted. )

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 2. DC/DC converter block | | [ DD2 ] | | | | |
| Output voltage | $V_{OUT}$ | IOUT = -10mA, Output voltage setting:1.8V | 1.778 | 1.800 | 1.822 | V |
| Input stability | $V_{LINE}$ | IOUT = -10mA PVCC2= 2.5V to 5.5V | -5 | - | +5 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -1200mA (Fixed PWM mode) | -10 | - | +10 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -1200mA (PFM/PWM mode) | -10 | - | +20 | mV |
| IN2 input impedance | $R_{IN}$ | IN2 = 2.0V | - | 150(*1) | - | kΩ |
| SW PMOS-Tr on resistance | $R_{PMOS}$ | LX2 = -30mA | - | 190(*1) | - | mΩ |
| SW NMOS-Tr on resistance | $R_{NMOS}$ | LX2 = 30mA | - | 135(*1) | - | mΩ |
| SW PMOS-Tr leakage current | $I_{LEAK}$ | LX2 = 0V | -3 | - | - | µA |
| SW NMOS-Tr leakage current | $I_{LEAK}$ | LX2 = 3.3V | - | - | 3 | µA |
| Over current protection value | $I_{LIMIT}$ | L=1.0µH | 1500(*2) | - | - | mA |
| PFM/PWM mode changeover current | $I_{PFM}$ | L=1.0µH | - | 65(*1) | - | mA |
| Discharge resistor | $R_{DIS}$ | - | - | 5 | - | kΩ |
| Soft start time | Tss | Soft start time setting:1ms | 0.9 | 1 | 1.1 | ms |
| Switching frequency | $f_{OSC}$ | - | 2.7 | 3.0 | 3.3 | MHz |

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

### 8.4 DD3

(AVCC = PVCC1A=PVCC1B=PVCC2=PVCC3 = 3.3V,
supply, PGND1A=PGND1B=PGND2=PGND3=GND=0V. Ta = +25°C, unless otherwise noted. )

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 3. DC/DC converter block [ DD3 ] | | | | | | |
| Output voltage | $V_{OUT}$ | IOUT = -10mA, Output voltage setting:3.3V | 3.241 | 3.300 | 3.359 | V |
| Input stability | $V_{LINE}$ | IOUT = -10mA, PVCC3= 2.5V to 5.5V | -5 | - | +5 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -600mA (Fixed PWM mode) | -10 | - | +10 | mV |
| Load stability | $V_{LOAD}$ | IOUT = -1mA to -600mA (PFM/PWM mode) | -10 | - | +15 | mV |
| IN2 input impedance | $R_{IN}$ | IN3 = 2.0V | - | 550(*1) | - | kΩ |
| SW PMOS-Tr on resistance | $R_{PMOS}$ | LX3-1 = -30mA | - | 115(*1) | - | mΩ |
| SW NMOS-Tr on resistance | $R_{NMOS}$ | LX3-1 = 30mA | - | 140(*1) | - | mΩ |
| SW PMOS-Tr on resistance | $R_{PMOS}$ | LX3-2 = -30mA | - | 155(*1) | - | mΩ |
| SW NMOS-Tr on resistance | $R_{NMOS}$ | LX3-2 = 30mA | - | 220(*1) | - | mΩ |
| SW PMOS-Tr leakage current | $I_{LEAK}$ | LX3-1 = 0V | -3 | - | - | µA |
| SW NMOS-Tr leakage current | $I_{LEAK}$ | LX3-1 = 3.3V | - | - | 1 | µA |
| SW PMOS-Tr leakage current | $I_{LEAK}$ | LX3-2 = 0V | -3 | - | - | µA |
| SW NMOS-Tr leakage current | $I_{LEAK}$ | LX3-2 = 3.3V | - | - | 1 | µA |
| Over current protection value | $I_{LIMIT}$ | L=1.0µH | 1000(*2) | - | - | mA |
| PFM/PWM mode changeover current | $I_{PFM}$ | L=1.0µH | - | 200(*1) | - | mA |
| Discharge resistor | $R_{DIS}$ | - | - | 5(*1) | - | kΩ |
| Soft start time | Tss | Soft start time setting:1ms | 0.9 | 1 | 1.1 | ms |
| Switching frequency | $f_{OSC}$ | - | 2.7 | 3.0 | 3.3 | MHz |

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

## 8.5 Digital Block

(AVCC = PVCC1A=PVCC1B=PVCC2=PVCC3 = 3.3V, supply, PGND1A=PGND1B=PGND2=PGND3=GND=0V. Ta = +25°C, unless otherwise noted. )

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 1. Power Good block | | [ Power Good ] | | | | |
| Output voltage | $V_{OL}$ | PG1, PG2, PG3 $I_{OL}$ = 1mA | - | - | 0.4 | V |
| Output current | $I_{OL}$ | PG1, PG2, PG3 | 1 | - | - | mA |
| Low voltage detection | $V_{TH}$ | IN1, IN2, IN3 = falling | - | Vo ×0.90(*1) | - | V |
| Power on detection | $V_{TH}$ | IN1, IN2, IN3 = rising | - | Vo ×0.93(*1) | - | V |
| 2. $I^2C$ block | | [ $I^2C$ ] | | | | |
| Input voltage | $V_{IH}$ | SCL,SDA | DVCC ×0.7 | - | DVCC | V |
| | $V_{IL}$ | SCL,SDA | 0 | - | DVCC ×0.3 | V |
| Input current | $I_{IH}$ | SCL,SDA DVCC = 3.3V | - | - | 10 | µA |
| | $I_{IL}$ | SCL,SDA DVCC = 3.3V | -10 | - | - | µA |
| Output voltage | $V_{OL}$ | SDA $I_{OL}$ = 3mA | - | - | 0.4 | V |
| Output current | $I_{OL}$ | SDA | 3 | - | - | mA |
| 3. ADDSEL block | | [ ADDSEL ] | | | | |
| Input voltage | $V_{IH}$ | ADDSEL | AVCC ×0.7 | - | AVCC | V |
| Input voltage | $V_{IL}$ | ADDSEL | 0 | - | 0.4 | V |
| Input current | $I_{ADD}$ | ADDSEL = 3.3V | 2.5 | 3.3 | 4.7 | µA |
| | $I_{ADD}$ | ADDSEL = 0V | - | - | 1 | µA |
| Input pull-down resistor | $R_P$ | ADDSEL | - | 1(*1) | - | MΩ |

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

## 9. Operation Mode List

**Table 1. Operation Mode List**

| | Mode | Stand-by | Stand-by2 | Normal | Error Detection |
|---|---|---|---|---|---|
| CTL signal | CTLMAIN (external) | L | H | H | H |
| | CTL1 (external/I²C) | L | L | H/L(*1) | X |
| | CTL2 (external/I²C) | L | L | H/L(*1) | X |
| | CTL3 (external/I²C) | L | L | H/L(*1) | X |
| Operation Block | Reference | OFF | ON | ON | ON |
| | Digital | OFF | ON | ON | ON |
| | DD1 | OFF | OFF | ON/OFF | OFF |
| | DD2 | OFF | OFF | ON/OFF | OFF |
| | DD3 | OFF | OFF | ON/OFF | OFF |
| I²C communication | I²C communication | disable | enable | enable | enable |
| Protection operating | Thermal shut down (TSD) | Not available | Not available | available | (*2) |
| | Over current protection (OCP) | Not available | Not available | available | (*2) |

*1: normal mode means that CTLMAIN pin is "H" level and each DD CTL pin is "H" level

*2: This state is after each err detection. Error state will release, when the power supply voltage or CTLMAIN pin will turn off and on.

**Priority of the External CTL pin and I²C Communication**

| CTLMAIN (External) | CTL1, CTL2, CTL3 (External) | 30h Resistor (I²C) | Relevant Channel |
|---|---|---|---|
| H | H | 1 | ON |
| H | H | 0 | ON |
| H | L | 1 | ON |
| H | L | 0 | OFF |
| L | X | disable | OFF |

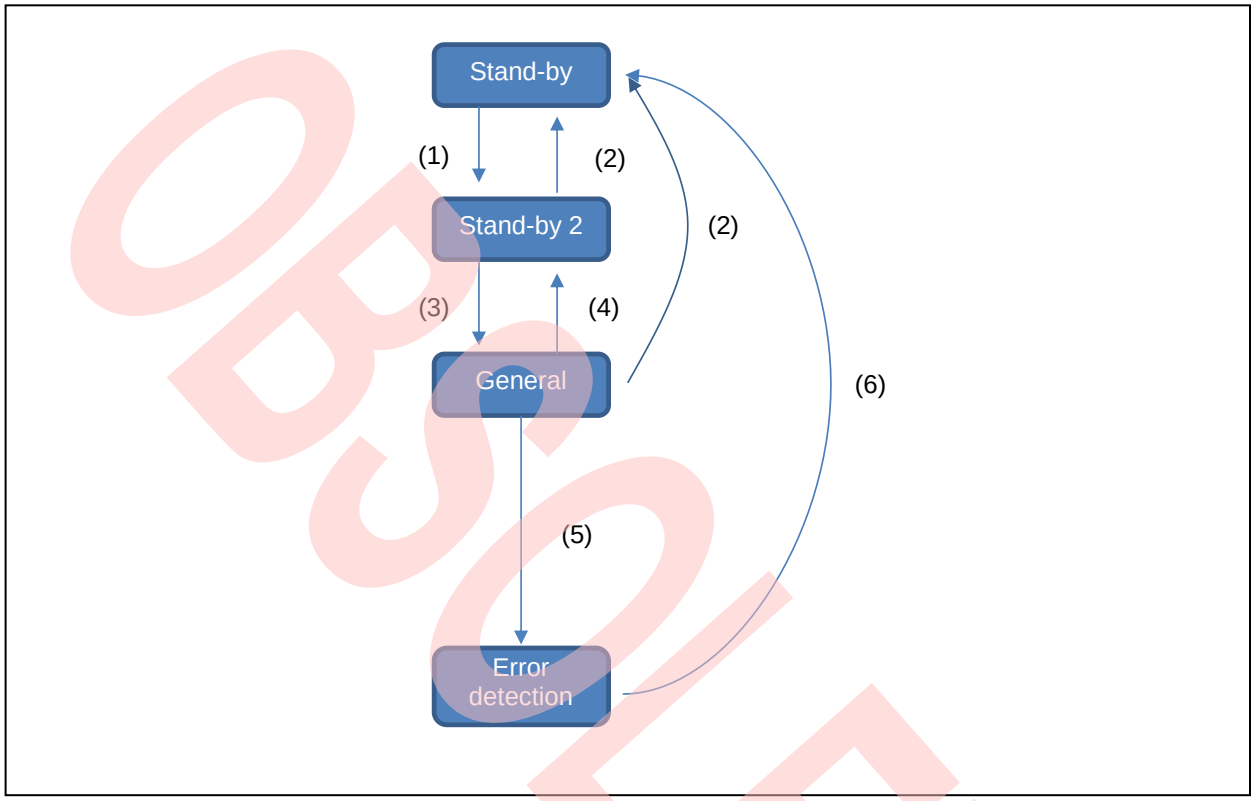
**Priority of the External MODE pin and I²C Communication**

| MODE (External) | 20h Resistor (I²C) | Operation Mode |
|---|---|---|
| H | 1 | PFM/PWM |
| H | 0 | PFM/PWM |
| L | 1 | PFM/PWM |
| L | 0 | Fixed PWM |

**Notes:**

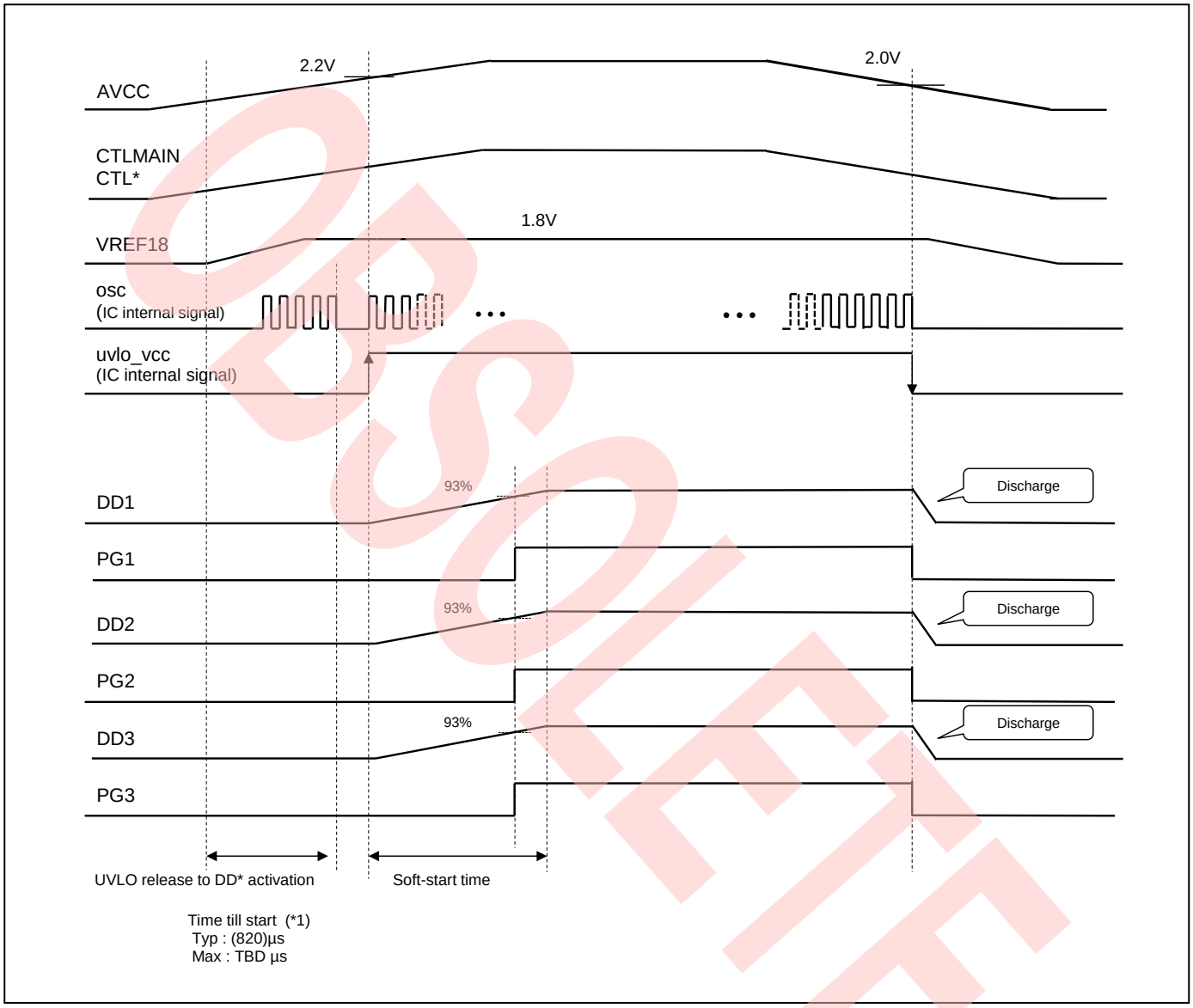
- The I²C communication is valid after the reference control block and digital block activation setting the external CTLMAIN pin to "H" level.
- Please attention below note about ON/OFF control of DD1, DD2, DD3 by I²C communication.
  When each DD control is turned off by I²C communication and external CTL pin remains "H" level, DCDC converter keep operating.

## 10. State Transition Diagram




(1) External CTLMAIN pin is "H" level.
(2) External CTLMAIN pin is "L" level.
(3) External CTL pin or $I^2C$ communication "relevant CH_ON"
(4) External CTL pin or $I^2C$ communication "relevant CH_OFF"
(5) Error detection (TSD, OCP 1ms continuation)
(6) Turning on the power supply again (equal to or less than uvlo_vcc rest voltage) or setting CTLMAIN to "L" level

## 11. Turning ON and OFF Sequence (AVCC=CTLMAIN, CTL1, CTL2, CTL3)



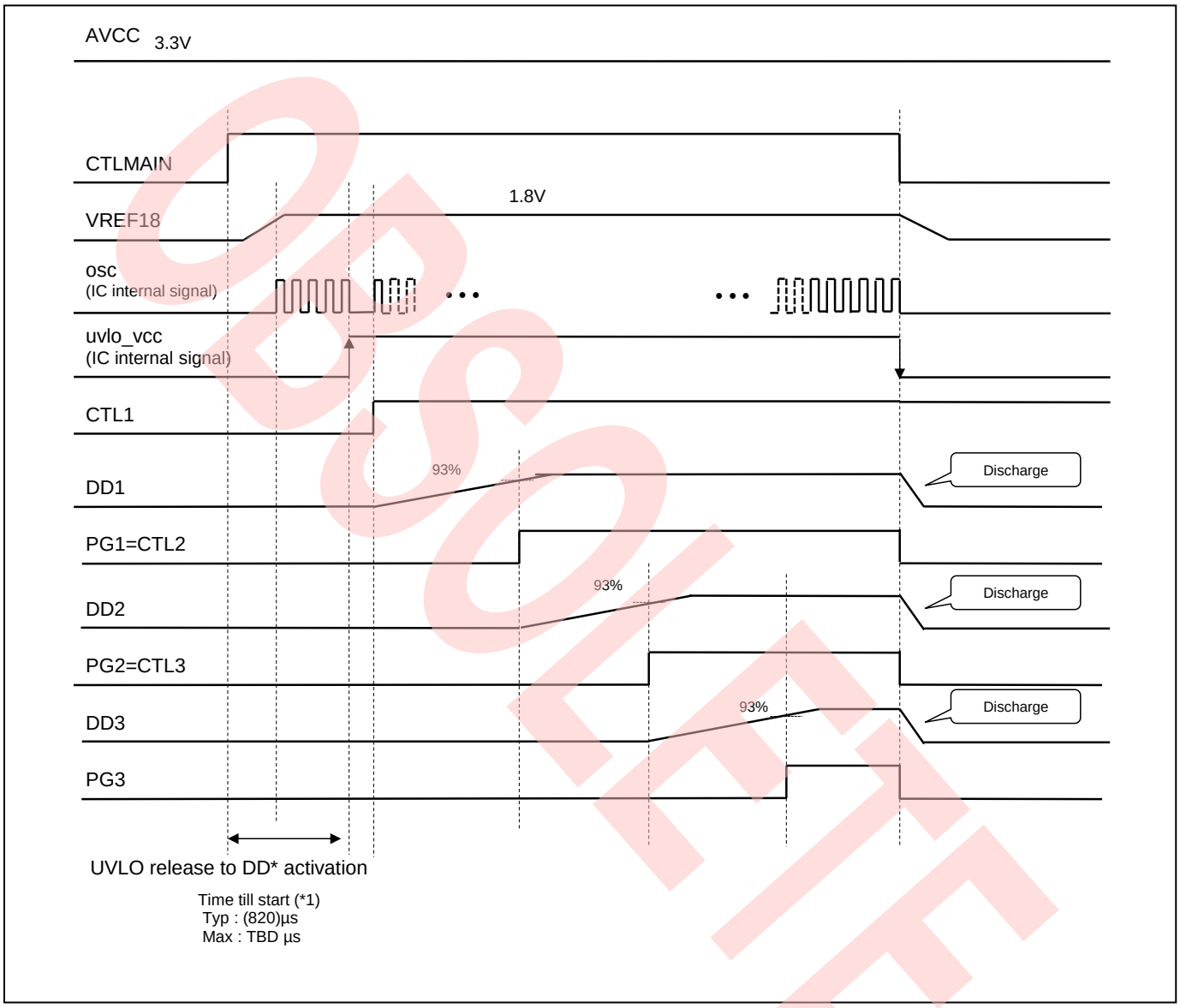



*1: CTL1, CTL2, CTL3

*2: DD1, DD2, DD3

*3: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0µF

## 12. Turning ON and OFF Sequence (AVCC →CTLMAIN→CTL1→CTL2→ CTL3)

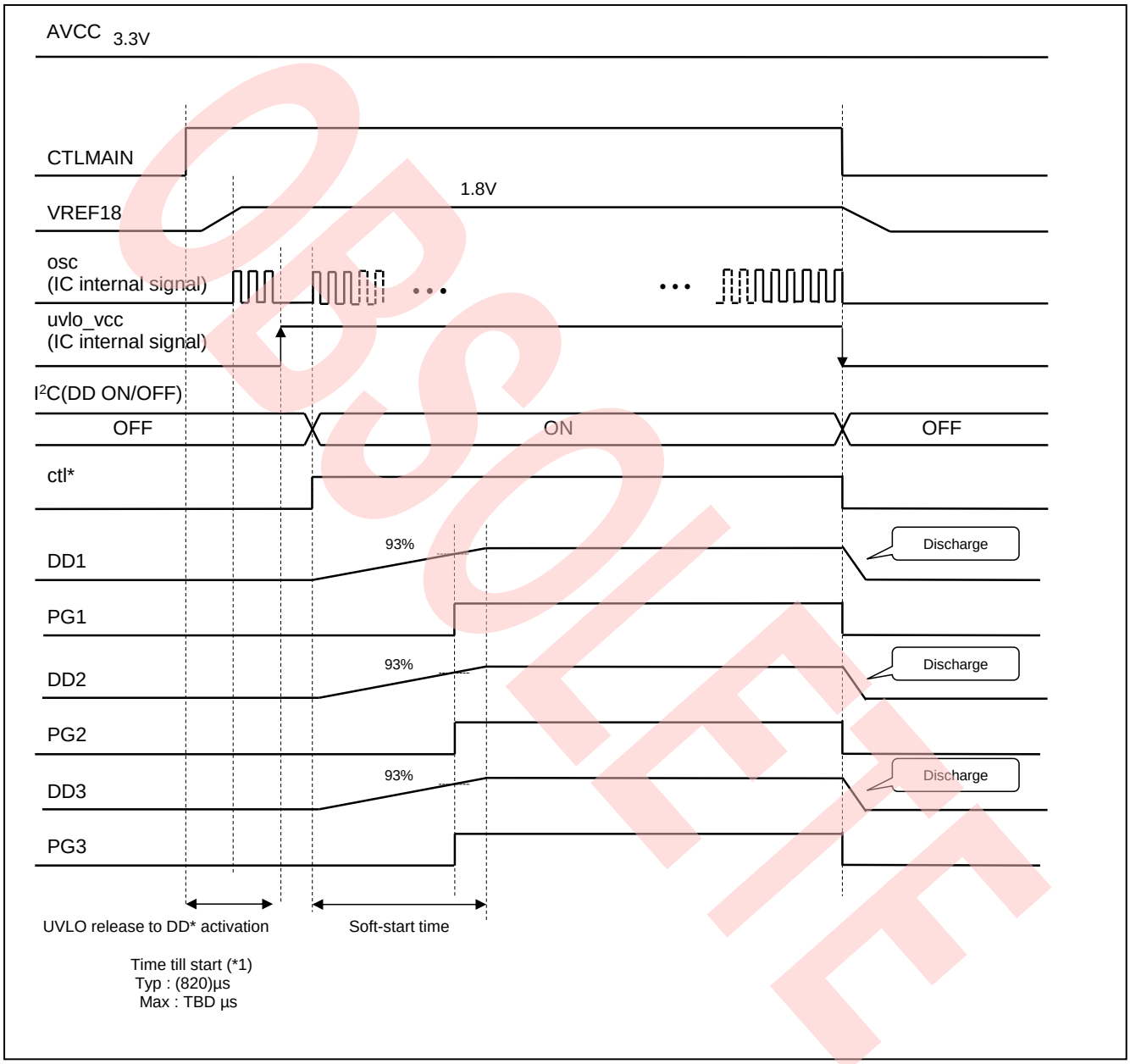





*1: DD1, DD2, DD3

*2: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0µF

## 13. Turning ON and OFF Sequence (AVCC→CTLMAIN→I²C)






*1: CTL1, CTL2, CTL3

*2: DD1, DD2, DD3

*3: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0µF

## 14. CTL Pin, MODE Pin, ADDSEL Pin Threshold Voltage

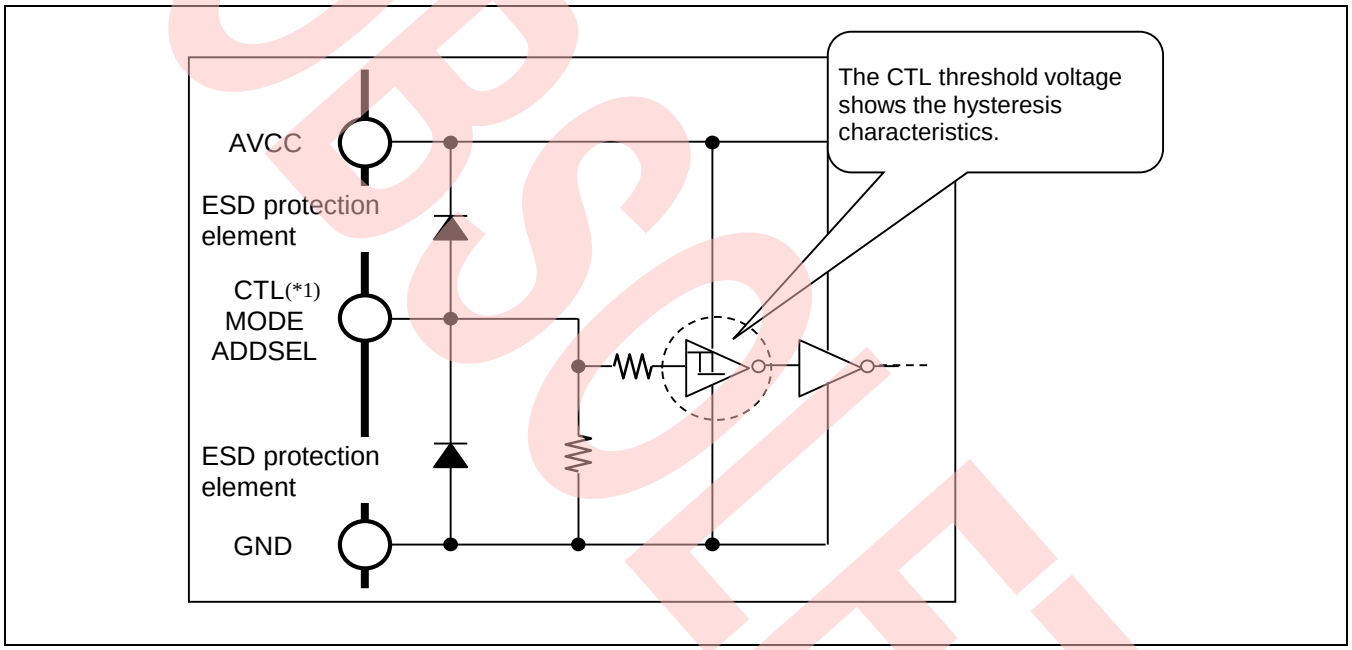
The input circuit structure for the CTL(*1) pin is the schmitt trigger style, and the threshold voltage shows the hysteresis characteristics when CTL(*1) OFF to ON and ON to OFF.

(See "CTL(*1) pin equivalent circuit diagram" below.)

Also, the threshold voltage level depends on the VCC pin voltage.

Moreover, make sure to input either the "H" level (>"VCC×0.7"V) or "L" level (<0.4V) to the CTL(*1) and MODE and ADDSEL pin when in use.

**Figure 3. CTL (*1), MODE, ADDSEL Pin Equivalent Circuit Diagram**




*1: CTLMAIN, CTL1, CTL2, CTL3

## 15. Protection Operation Sequence

**Over Current Protection (DD channel)**

The DD channel monitors the peak current of FET at any time during the operation. When the DD output becomes the over current state, the output voltage is decreased. Afterward, the timer operation is performed and the output stops after about 1ms progress.

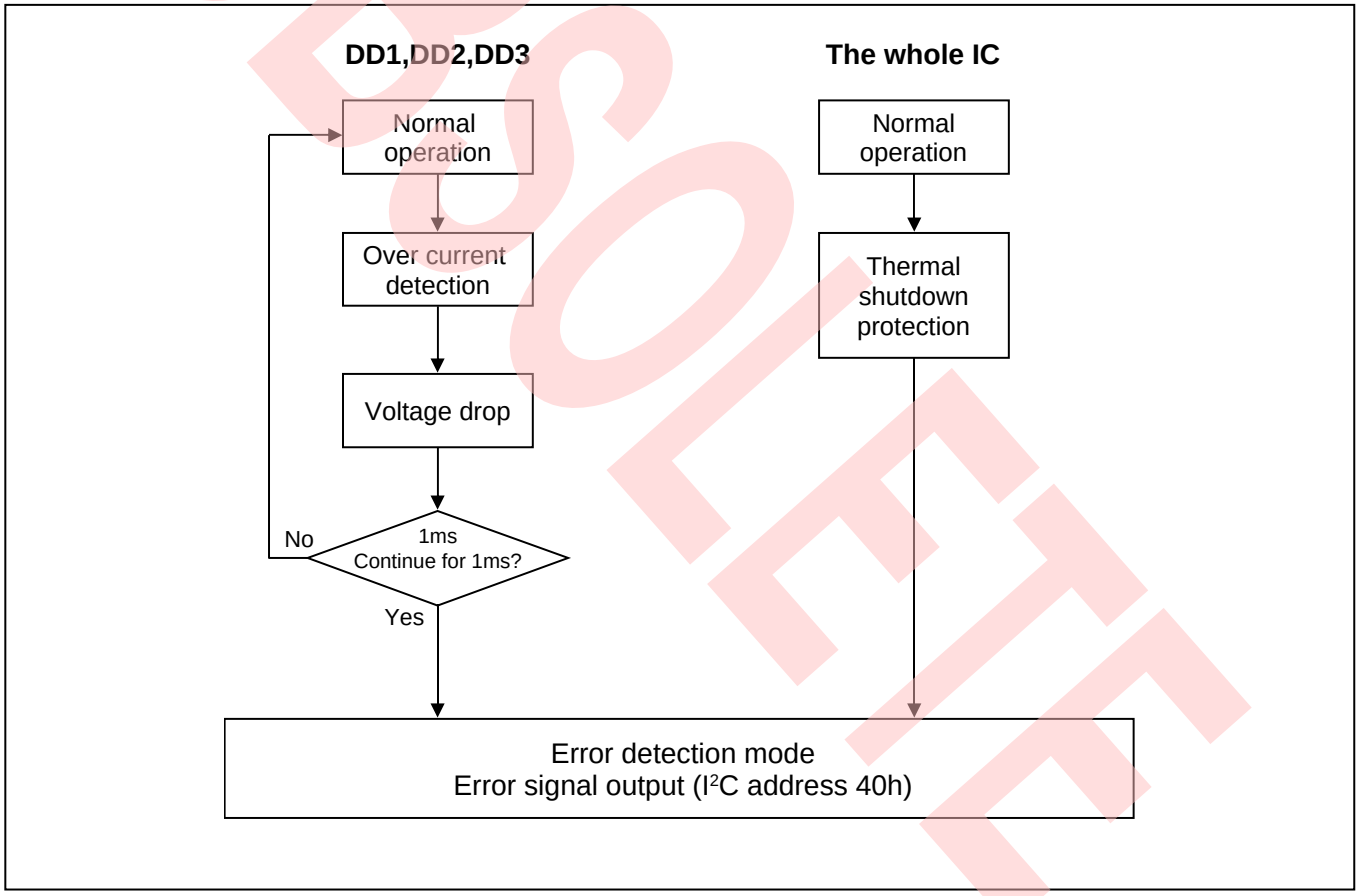
When one of each DD channel stops operation by over current protection, all DD channels stop operation.

**Thermal Shut Down**

If the temperature at the junction part reaches +150°C, the thermal shutdown protection circuit turns all channels off.

**Error Detection Sequence**

**Figure 4. Error Detection Sequence**




**Error Detection Mode Release**

It is necessary to turn the power supply turning on again, or to turn CTLMAIN turning on again to release the error detection mode.

## 16. Operation Condition, Stop Circuit and Release Condition for Protection Circuit

| Channel | Operation Whilst Under Protection | Over Current Protection (OCP) | Under Voltage Lockout Protection (UVLO) | Thermal Shutdown Protection (TSD) |
|---|---|---|---|---|
| DD1,DD2,DD3 | Discharge | Operating condition:<br>After about 1ms progress in the over current condition<br><br>Process during protection operation:<br>DD1, DD2, DD3 stop<br><br>Recovery condition:<br>(1) Power supply reasserted<br>(2) CTLMAIN reasserted | Operating condition: Input voltage drop<br><br>Process during protection operation:<br>DD1, DD2, DD3 stop<br><br>Recovery condition:<br>Input voltage rise<br><br>UVLO operates only when CTLMAIN is "H" (at VREF18 output). | Operating condition:<br>Chip temperature increment<br><br>Process during protection operation:<br>DD1, DD2, DD3 stop<br><br>Recovery condition:<br>(1) Power supply reasserted<br>(2) CTLMAIN reasserted<br><br>Only when CTLMAIN is in the "H" state and CTL(*1) is in the "H" state, or when DD(*2) in operating condition by $I^2C$, will operate. |
| Error output (address 40h) | - | Write "1" when detecting OCP | No change | Write "1" when detecting TSD |

Thermal shutdown protection (TSD) operation during over current protection timer operation
When the thermal shutdown protection (TSD) operated during the over current protection (OCP) timer operation, the thermal shutdown protection has priority.
Operation when releasing under voltage lockout protection (UVLO)

- DD1,DD2,DD3,DD4: Activation following the condition for CTL(*1) pin or $I^2C$

**Note:**

- When VREF18 decreases at the time of UVLO operation, $I^2C$ register is reset, and all DD does OFF.
  It is necessary to let you do ON by CTL(*1) pin and communication again to let DD have ON."

*1: CTL1, CTL2, CTL3

*2: DD1, DD2, DD3

## 17. DD Soft Start Operation

The soft-start operation for DD1, DD2 and DD3 is enabled in order to prevent the rush current during the DD activation. The soft-start time can be controlled by $I^2C$.

About output voltage changing option, soft start time is showed by follow equation.

Tss=Tslp × Vset/Vdef (ms)

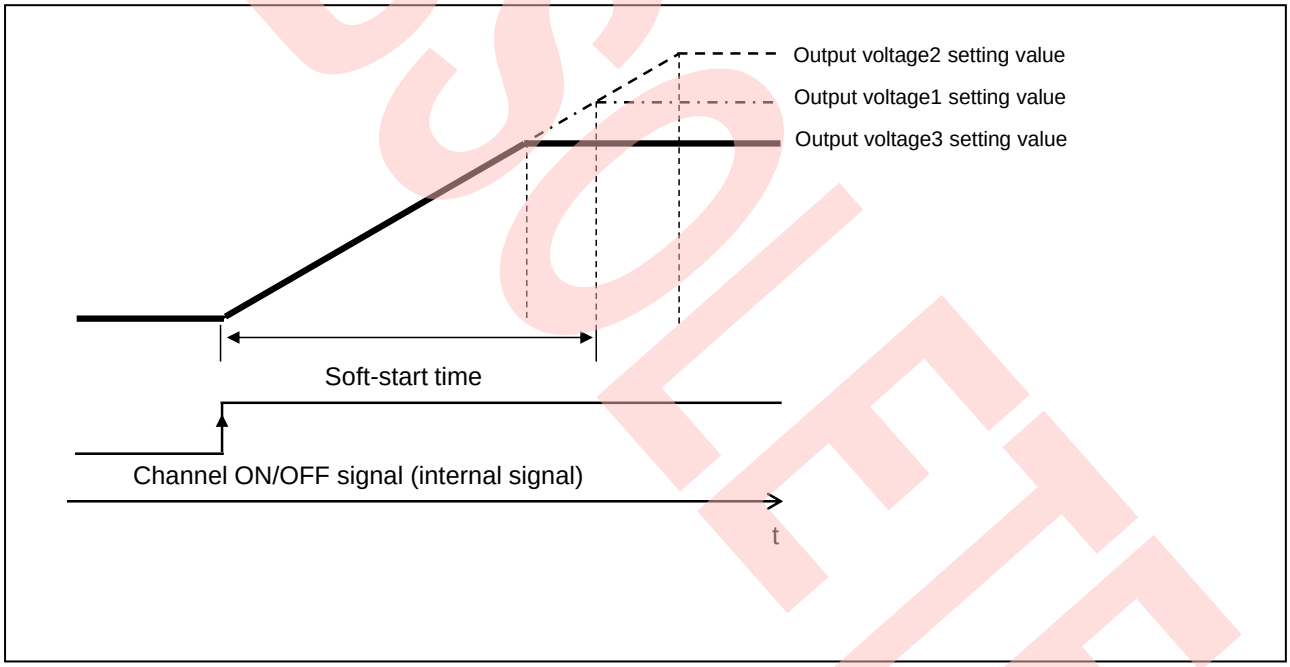
Tss: soft start time

Tslp: slope coefficient of soft start

Vset: output voltage setting

Vdef: DD1=1.0, DD2=1.8, DD3=3.3

**Figure 5. DD Soft Start**



## 18. Discharge Operation

**DD Channel**

When executing the DD OFF operation at the channel ON/OFF signal, the DC/DC smooth capacitance charged for each output voltage is discharged using resistor for discharge which is set in the IC and the output voltage is decreased gradually. However, the discharge time changes depending on the DC/DC converter load current.

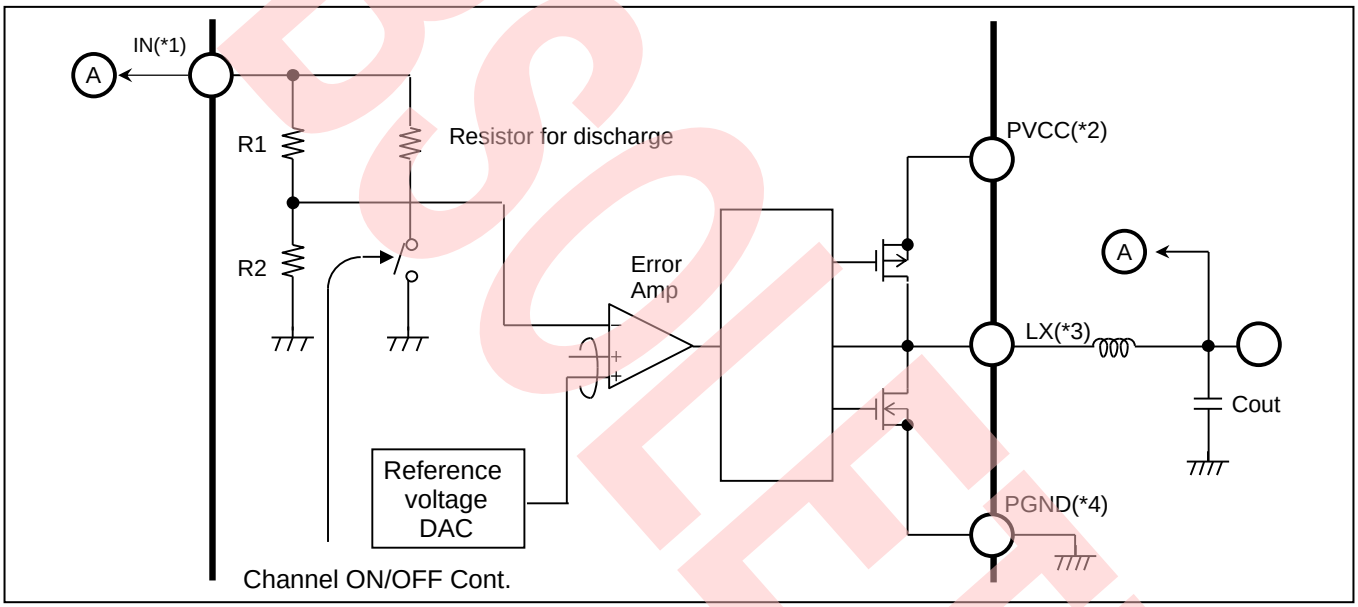
The discharge time is calculated by the following equation.

Discharge time (time till the output becomes 10% without load)

$toff(s) \approx 2.3 \times R\_DIS \times C_{OUT}$ (F)

**Note:**

- See the table in Electrical Characteristics for the discharge resistor value.




*1: IN1, IN2, IN3

*2: PVCC1, PVCC2, PVCC3

*3: LX1, LX2, LX3

*4: PGND1, PGND2, PGND3

## 19. PG Function

The following pins for each channel Power Good output are prepared.

**PG1**

It is the pin for DD1 Power Good output.

When the output voltage exceeds 93% of the setting value at the DD1 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD1 OFF mode.

**PG2**

It is the pin for DD2 Power Good output.

When the output voltage exceeds 93% of the setting value at the DD2 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD2 OFF mode.

**PG3**

It is the pin for DD3 Power Good output.

When the output voltage exceeds 93% of the setting value at the DD3 ON mode, "H" is output.

Also, when the output voltage becomes equal or lower than 90% of the setting value after the "H" output, "L" is output. "L" is output at the DD3 OFF mode.

# 20. I²C Interface

## 20.1 Structure of I²C Interface

The I²C interface executes the data communication in 1 byte (8-bit) units using two signal lines (bus), a SCL (serial clock line) and a SDA (serial data line).

This bus is connected to multiple devices;

master: device to generate the clock signal and to control the data transfer (CPU and so on)

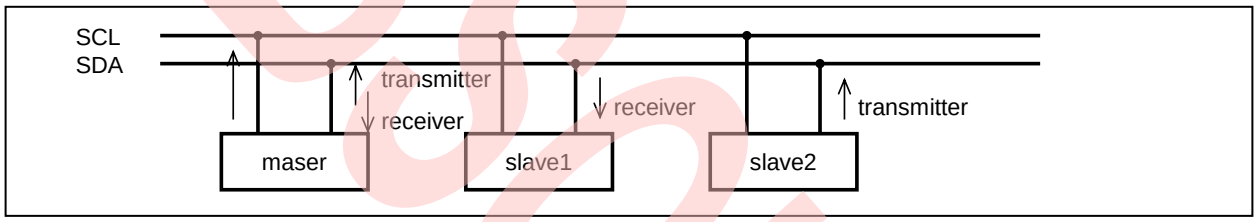
slave: device that an address is specified by a master.
This IC is set as the slave and has no function to be the master.

Each device is defined due to the communication direction as described below.

transmitter: device to send data to bus

receiver: device to receive data from bus

The IC has the function both transmitter and receiver.




The IC defines the followings;

Write : data is transmitted from master and the IC receives data

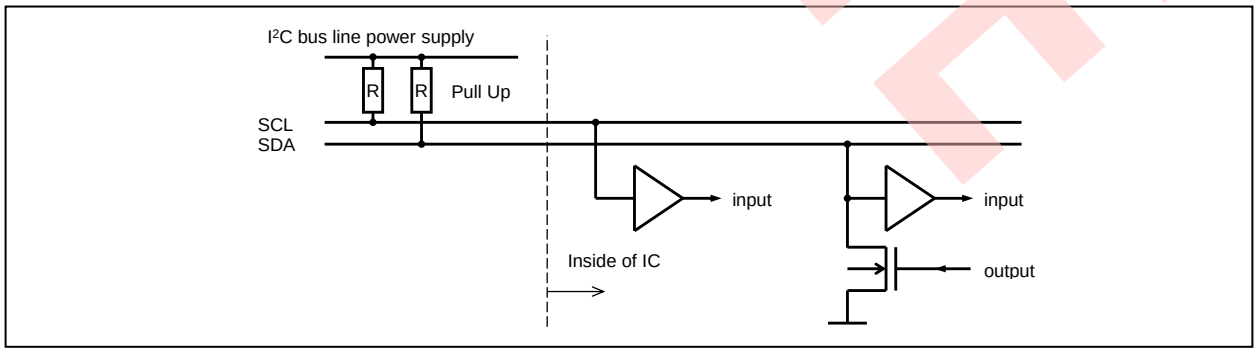
Read : The IC transmits data and master receives data.

## 20.2 Definition of Signal Lines

SCL and SDA are connected to the power supply by the pull-up resistor.
The output circuit is the open Drain output.
When a bus is not used (waiting state), the open "H" is set changing the open Drain to the OFF state.

**Note:**

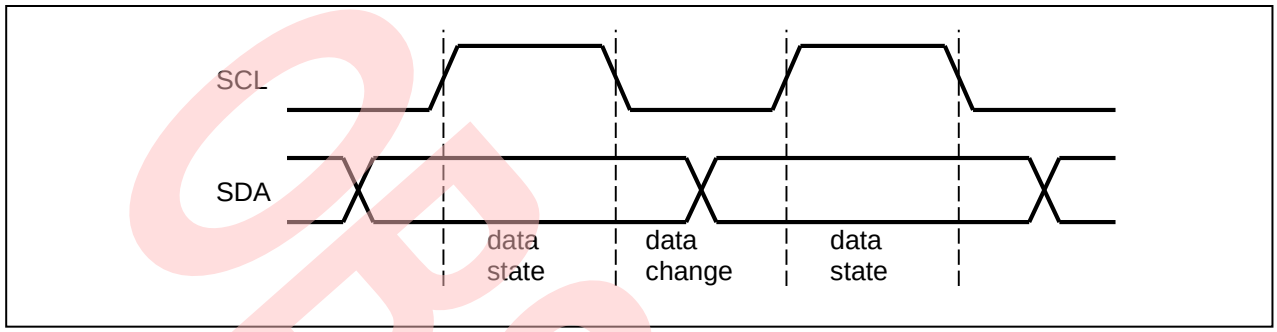
- SCL and SDA pins adopt a different ESD protection system from standard I²C specification because of ESD enhancement (see 22 I/O Pin Equivalent Circuit Diagram). When the power supply is in the bus line, do not shut off the power supply for an IC (DVCC).



### 20.3 Validity of Data

Data has the following characteristics;

- Change when SCL is the "L" level
- Valid if the state is kept while SCL is the "H" level.

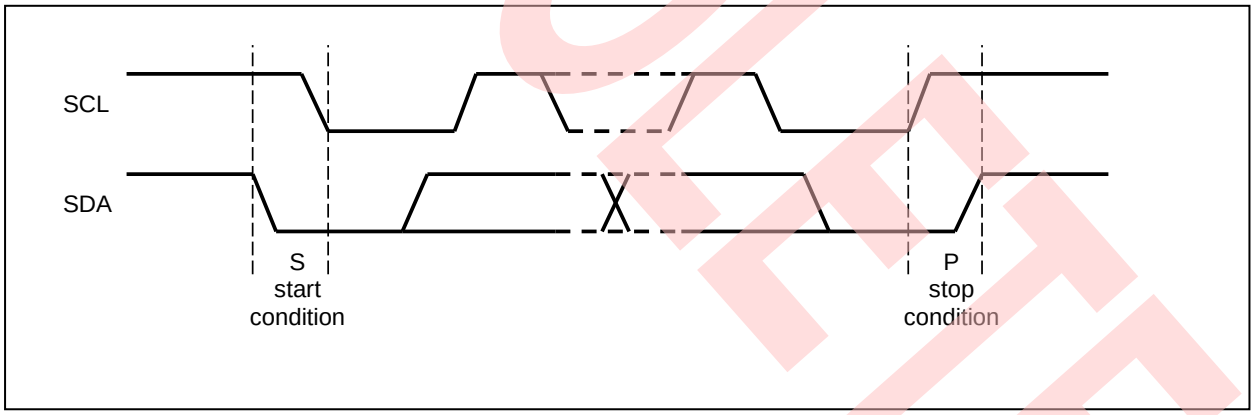



The SDA signal change means the start or stop condition when SCL is the "H" level.

### 20.4 Definition of Start and Stop Condition

The start and stop conditions are output from the master and shows start and stop of communications to the slave.

- Start: SDA changes from "H" to "L" when SCL is "H".
- Stop: SDA changes from "L" to "H" when SCL is "H".



## 20.5 ACK Signal

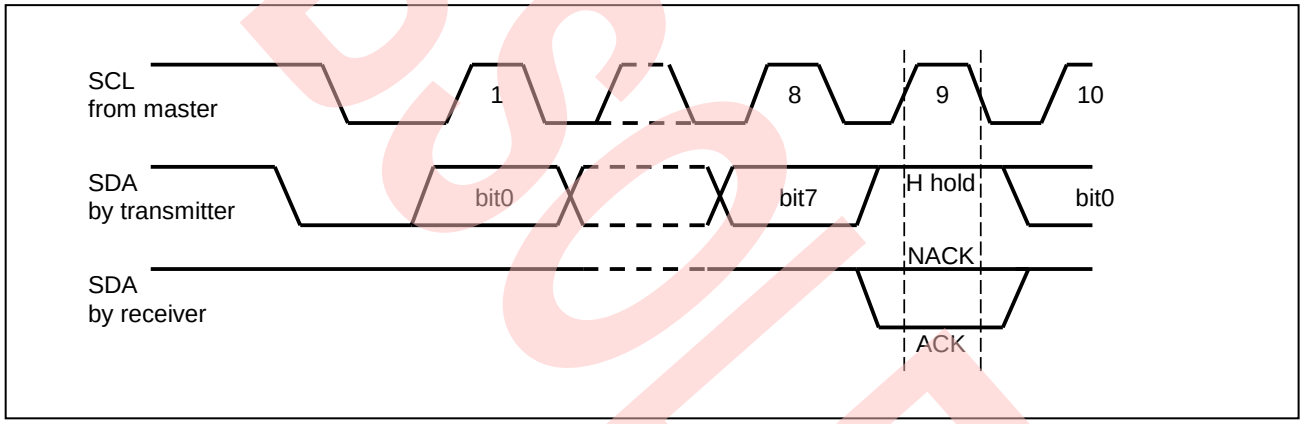
This is a signal to confirm the data reception during communication.
The receiver replies the ACK signal to show the data reception to a transmitter every time
1 byte (8-bit) of data is received. The ACK signal is sent in 9clk after sending data 8-bit matching to the SCL signal that the master generates.

- A transmitter keeps SDA output "open H" in SCL9clk.
- A receiver informs the data reception situation to a transmitter outputting the followings in SCL 9 clk;

  when data was received : SDA output "L" (ACK)

  when no data was received : SDA output "open H" (NACK)

However, if the master is changed to the receiver, ACK is not replied after the last data reception because the bus keeps open stopping the data transmission to the slave transmitter. In this case, the slave transmitter opens the bus (open H) and is set to the stop condition reception waiting state from the master.



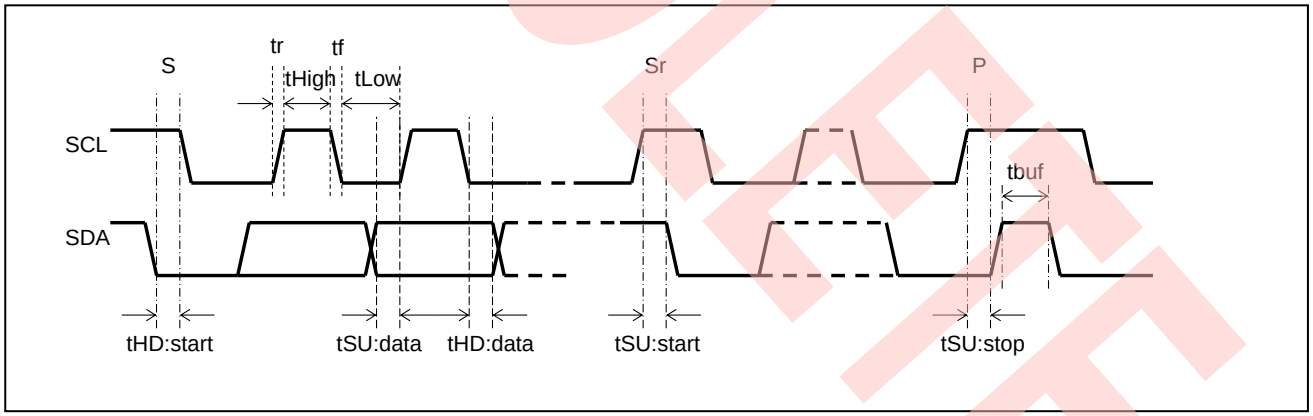
## 20.6 I²C Interface Input Timing

(within recommended operating conditions)

| Parameter | Symbol | Value | | | | Unit |
|---|---|---|---|---|---|---|
| | | SCL=100kHz | | SCL=400kHz | | |
| | | Min | Max | Min | Max | |
| SCL clock frequency | fSCL | - | 100 | - | 400 | kHz |
| Start condition hold time | $t_{HD:start}$ | 4.0 | - | 0.6 | - | µs |
| Restart condition setup time | $t_{SU:start}$ | 4.7 | - | 0.6 | - | µs |
| Stop condition setup time | $t_{SU:stop}$ | 4.0 | - | 0.6 | - | µs |
| Stop to Start bus open time | $t_{buf}$ | 4.7 | - | 1.3 | - | µs |
| SCL "L" time | $t_{Low}$ | 4.7 | - | 1.3 | - | µs |
| SCL "H" time | $t_{High}$ | 4.0 | - | 0.6 | - | µs |
| SCL/SDA rising time | $t_r$ | - | 1.0 | - | 0.3 | µs |
| SCL/SDA falling time | $t_f$ | - | 0.3 | - | 0.3 | µs |
| Data hold time | $t_{HD:data}$ | 0.0 | - | 0.0 | - | µs |
| Data setup time | $t_{SU:data}$ | 0.25 | - | 0.10 | - | µs |
| SCL/SDA capacitor load | $C_b$ | - | 400 | - | 400 | pF |

VIH/VIL level reference

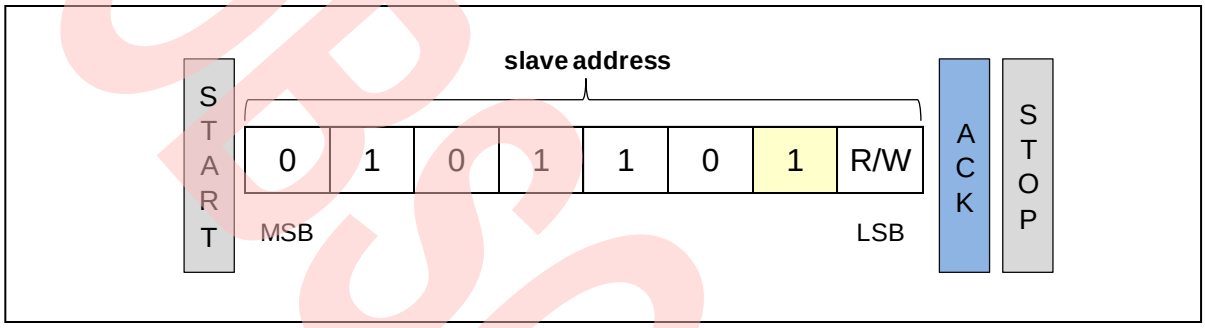
Conform to I²C bus specifications



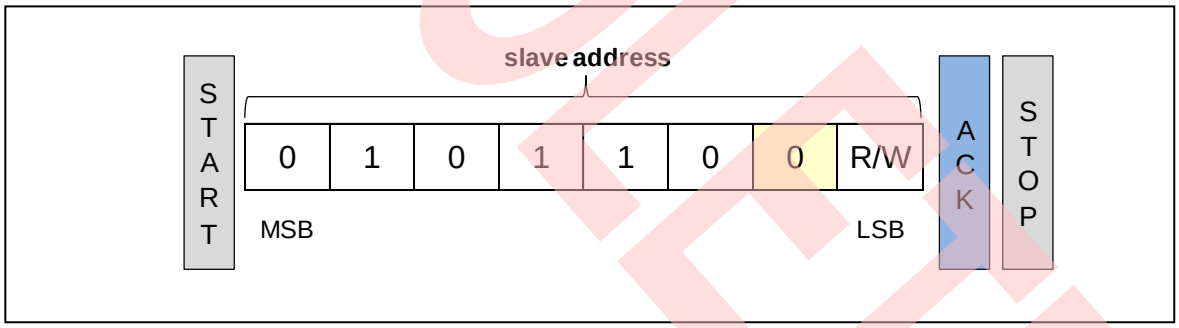
## 20.7 Slave Address

This is a slave address when communicating with the $I^2C$ interface.
The slave address of this IC is set by the first seven bits as shown below.
The seventh bit follows the ADDSEL pin and "0"/"1" are variable.
The eighth bit is called the least significant bit (LSB) and determines the message direction. The bit "0" shows that information will be written from the master to the slave.
The bit "1" shows that the master reads information from the slave.
This does not support the general call address.

When the ADDSEL pin is in "H"



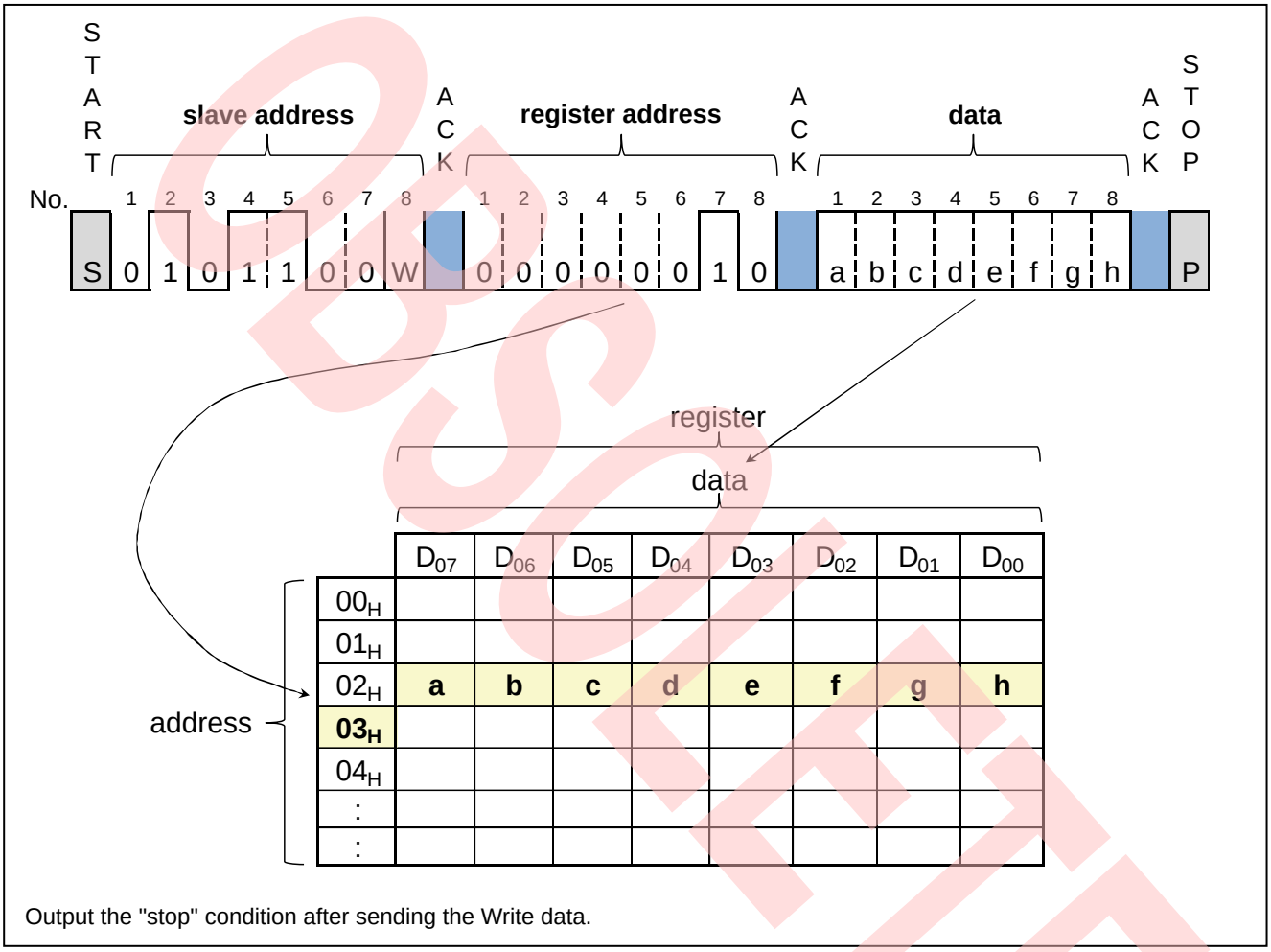

When the ADDSEL pin is in "L"



## 20.8 Bit Structure of Data on I²C Interface

1. Writing Data to Register and Reading Data

The data line is sent/received in the order from the most significant bit (MSB) to the least significant bit (LSB).




Output the "stop" condition after sending the Write data.

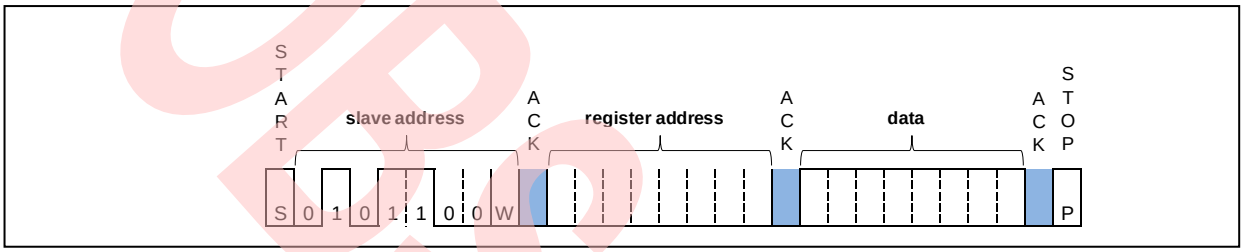
: Signal which a master sends, : Signal which this IC sends

2. I²C Interface Data Format

About I²C Communication

1. When a different slave address comes, non-matching ID is informed by not replying ACK after receiving the slave address.
2. All registers write to internal registers in the ACK signal after receiving the 8-bit data of each setting.
3. If a non-existing register address is specified, data is not written to a register.
4. Output the "stop" condition after sending the write data.

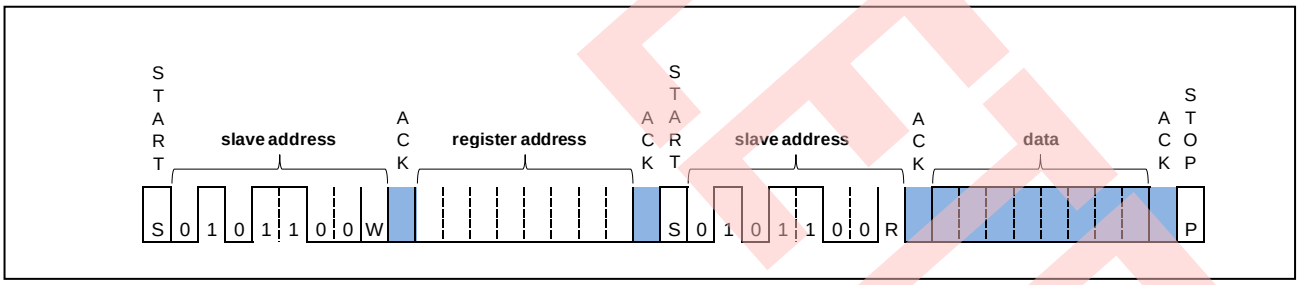
<Write(W)>




Write is allowed per one address. (Sequential writing is not allowed.)
Send register address and data as one unit.

: Signal which a master sends, : Signal which this IC sends

<Read(R)>




Read is allowed per one address. Be sure to perform read by specifying the register addresses.
(Sequential reading is not allowed.)

: Signal which a master sends, : Signal which this IC sends

## 21. Structure of I²C Interface and Data

**Table 2. Register Map**

| | Address | Data | | | | | | | | | Writing Timing | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | d07 | d06 | d05 | d04 | d03 | d02 | d01 | d00 | Default | | |
| Output voltage | $00_H$ | 0 | 0 | 0 | D04 | D03 | D02 | D01 | D00 | $0F_H$ | ACK | DD1 output voltage setting |
| | $01_H$ | 0 | 0 | 0 | 0 | D03 | D02 | D01 | D00 | $0C_H$ | ACK | DD2 output voltage setting |
| | $02_H$ | 0 | 0 | 0 | 0 | 0 | D02 | D01 | D00 | $05_H$ | ACK | DD3 output voltage setting |
| | $03_H$ | 0 | 0 | 0 | (*1) | (*1) | (*1) | (*1) | (*1) | $0F_H$ | ACK | Unused |
| Soft start | $10_H$ | 0 | 0 | 0 | 0 | D03 | D02 | D01 | D00 | $00_H$ | ACK | DD1 soft-start time setting |
| | $11_H$ | 0 | 0 | 0 | 0 | D03 | D02 | D01 | D00 | $00_H$ | ACK | DD2 soft-start time setting |
| | $12_H$ | 0 | 0 | 0 | 0 | D03 | D02 | D01 | D00 | $00_H$ | ACK | DD3 soft-start time setting |
| | $13_H$ | 0 | 0 | 0 | 0 | (*1) | (*1) | (*1) | (*1) | $00_H$ | ACK | Unused |
| DD operation mode | $20_H$ | 0 | 0 | 0 | 0 | (*1) | D02 | D01 | D00 | $00_H$ | ACK | DD operation mode setting<br>"0": Fixed PWM mode,<br>"1": PFM/PWM mode |
| ON/OFF | $30_H$ | 0 | 0 | 0 | 0 | (*1) | D02 | D01 | D00 | $00_H$ | ACK | DD output ON/OFF setting<br>"0": Output OFF / "1": Output ON |
| Error | $40_H$ | 0 | 0 | 0 | D04 | (*1) | D02 | D01 | D00 | $00_H$ | - | DD error state monitoring register (read only)<br>"0": Normal / "1": Error detection |
| PG | $50_H$ | 0 | 0 | 0 | 0 | (*1) | D02 | D01 | D00 | $00_H$ | - | DD PG state monitoring register (read only)<br>"0": Non-output / "1": output |
| For test | $EX_H$ | - | - | - | - | - | - | - | - | - | - | Disabled |
| For test | $FX_H$ | - | - | - | - | - | - | - | - | - | - | Disabled |

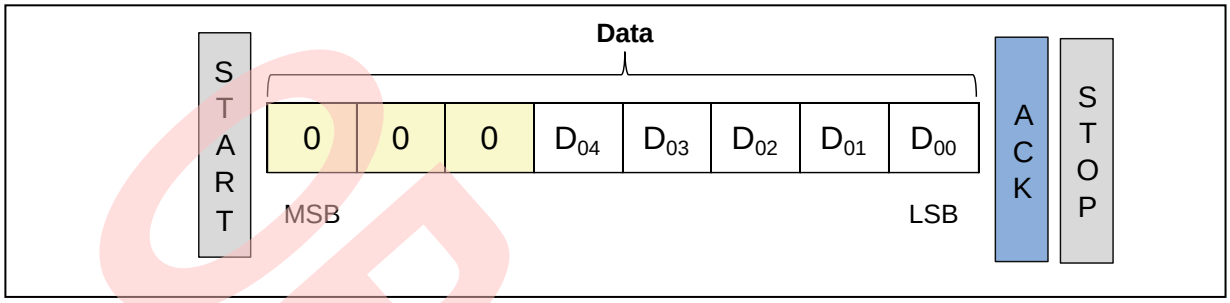
*1: Unused register. Write/read is possible, but does not influence IC movement.

**Note:**

- Address $FX_H$ and address $EX_H$ are for test.
  Donot write/read $FX_H$ and $EX_H$.

## 21.1 About DD1 Output Voltage Setting

- Address $00_H$ DD1 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD1 is controlled by writing data to address $00_H$.




Address $00_H$: For DD1 output voltage setting
$D_{04}$ to $D_{00}$: Set the output voltage

**DD1 Output Voltage Setting Table**

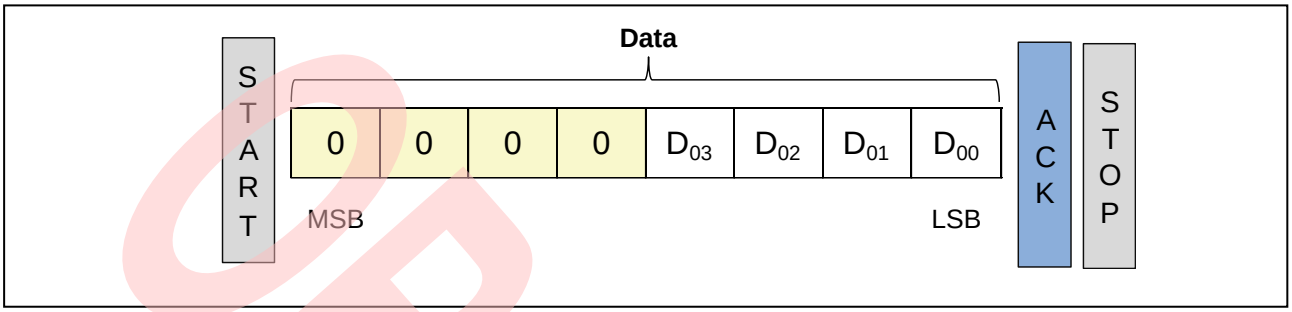
| Data | Output Voltage (V) |
|---|---|
| $00_H$ | 0.700 |
| $01_H$ | 0.720 |
| $02_H$ | 0.740 |
| $03_H$ | 0.760 |
| $04_H$ | 0.780 |
| $05_H$ | 0.800 |
| $06_H$ | 0.820 |
| $07_H$ | 0.840 |
| $08_H$ | 0.860 |
| $09_H$ | 0.880 |
| $0A_H$ | 0.900 (*1) |
| $0B_H$ | 0.920 |
| $0C_H$ | 0.940 |
| $0D_H$ | 0.960 |
| $0E_H$ | 0.980 |
| $0F_H$ | 1.000 (*1) |

| Data | Output Voltage (V) |
|---|---|
| $10_H$ | 1.020 |
| $11_H$ | 1.040 |
| $12_H$ | 1.060 |
| $13_H$ | 1.080 |
| $14_H$ | 1.100 (*1) |
| $15_H$ | 1.120 |
| $16_H$ | 1.140 |
| $17_H$ | 1.160 |
| $18_H$ | 1.180 |
| $19_H$ | 1.200 (*1) |
| $1A_H$ | 1.220 |
| $1B_H$ | 1.240 |
| $1C_H$ | 1.260 |
| $1D_H$ | 1.280 |
| $1E_H$ | 1.300 |
| $1F_H$ | 1.320 |

*1: Preset value

## 21.2 About DD2 Output Voltage Setting

- Address $01_H$ DD2 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD2 is controlled by writing data to address $01_H$.




address$01_H$: For DD2 output voltage setting
$D_{03}$ to $D_{00}$: Set the output voltage

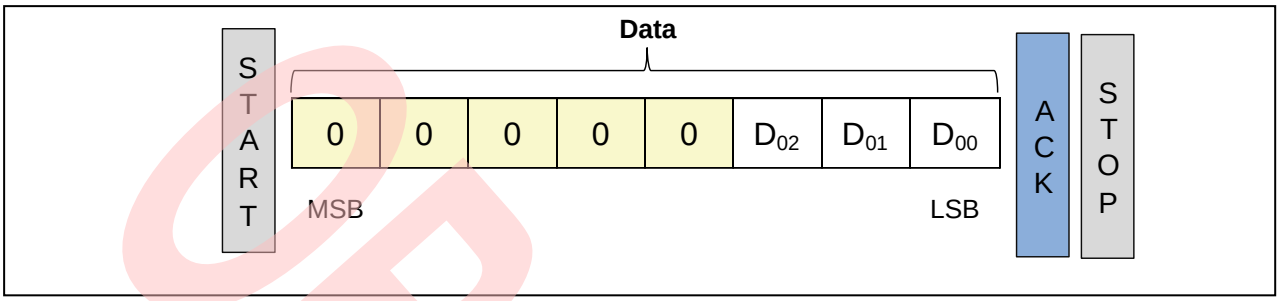
**DD2 Output Voltage Setting Table**

| Data | Output Voltage (V) |
|---|---|
| $00_H$ | 1.200 (*1) |
| $01_H$ | 1.250 |
| $02_H$ | 1.300 |
| $03_H$ | 1.350 (*1) |
| $04_H$ | 1.400 |
| $05_H$ | 1.450 |
| $06_H$ | 1.500 (*1) |
| $07_H$ | 1.550 |
| $08_H$ | 1.600 |
| $09_H$ | 1.650 |
| $0A_H$ | 1.700 |
| $0B_H$ | 1.750 |
| $0C_H$ | 1.800 (*1) |
| $0D_H$ | 1.850 |
| $0E_H$ | 1.900 |
| $0F_H$ | 1.950 |

*1: Preset value

## 21.3 About DD3 Output Voltage Setting

- Address $02_H$ DD3 is allocated as resisters for the DC/DC output voltage setting.
- The DC/DC output voltage setting of DD3 is controlled by writing data to address $02_H$.




address$02_H$: For DD3 output voltage setting
D02 to D00: Set the output voltage

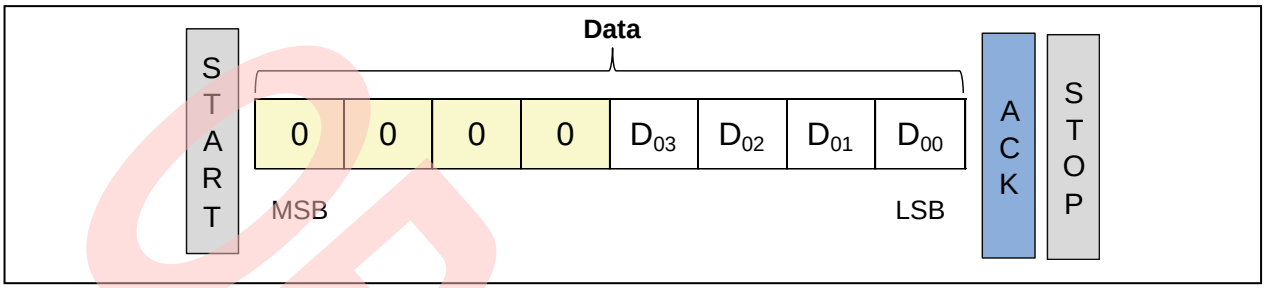
**DD3 Output Voltage Setting Table**

| Data | Output Voltage(V) |
|---|---|
| $00_H$ | 2.80 (*1) |
| $01_H$ | 2.90 |
| $02_H$ | 3.00 (*1) |
| $03_H$ | 3.10 |
| $04_H$ | 3.20 |
| $05_H$ | 3.30 (*1) |
| $06_H$ | 3.40 |
| $07_H$ | 3.50 (*1) |

*1: Preset value

## 21.4 About Soft Start Time

- Address $10_H$ to $12_H$ are allocated as registers for the soft start time control.
- The soft start time control is controlled by writing data to addresses $10_H$ to $12_H$.




address$10_H$: For DD1 soft start time setting
address$11_H$: For DD2 soft start time setting
address$12_H$: For DD3 soft start time setting
$D_{03}$ to $D_{00}$: Set the soft start time

Tss=Tslp × Vset/Vdef (ms)

Tss: soft start time

Tslp: slope coefficient of soft start:refer to follow table

Vset: output voltage setting

Vdef: DD1=1.0, DD2=1.8, DD3=3.3

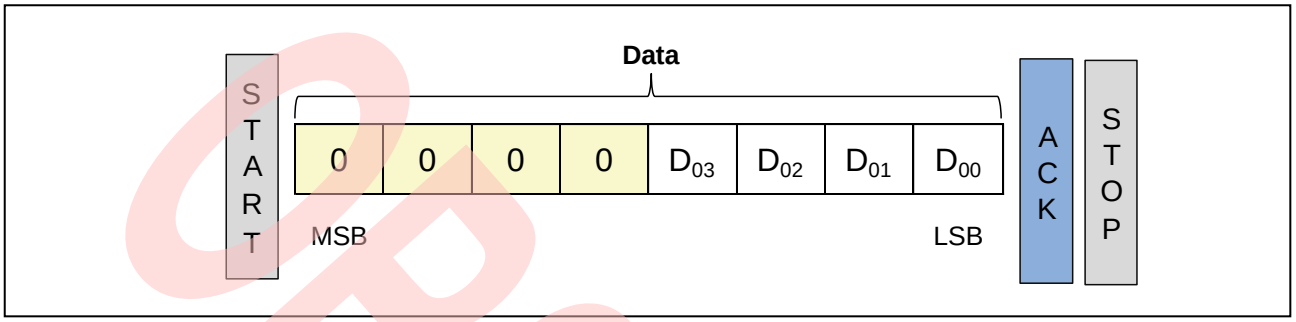
**Soft Start Time Setting**

| Data | Tslp | Remarks |
|---|---|---|
| $00_H$ | 1.0 | DD1,DD2,DD3 (*1) |
| $01_H$ | 2.0 | |
| $02_H$ | 3.0 | |
| $03_H$ | 4.0 | |
| $04_H$ | 5.0 | |
| $05_H$ | 6.0 | |
| $06_H$ | 7.0 | |
| $07_H$ | 8.0 | |
| $08_H$ | 9.0 | |
| $09_H$ | 10.0 | |
| $0A_H$ | 11.0 | |
| $0B_H$ | 12.0 | |
| $0C_H$ | 13.0 | |
| $0D_H$ | 14.0 | |
| $0E_H$ | 15.0 | |
| $0F_H$ | 16.0 | |

*1: Preset value

## 21.5 DC/DC Operation Mode

- Address $20_H$ is allocated as a register for the DC/DC operation mode control.
- The DC/DC operation mode is controlled by writing data to address $20_H$.



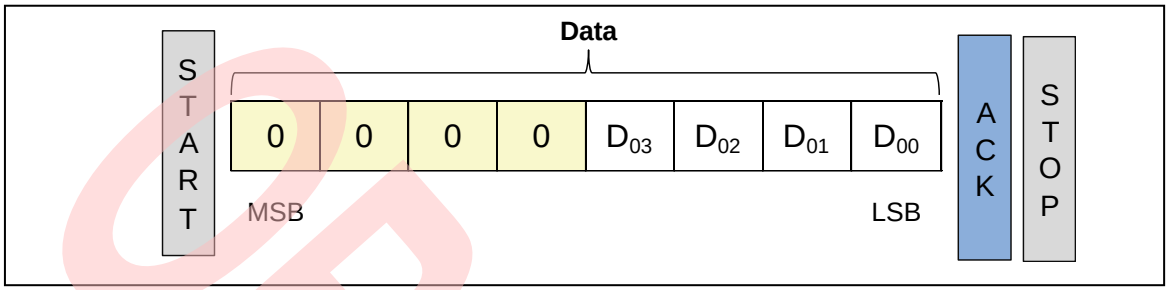

address$20_H$: For DC/DC operation mode setting
$D_{01}$ to $D_{00}$: Set the DC/DC operation mode

| Address | Bit | Description |
|---|---|---|
| $20_H$ | D00 | 0: DD1 Fixed PWM (*1)<br>1: DD1 PFM/PWM |
| $20_H$ | D01 | 0: DD2 Fixed PWM (*1)<br>1: DD2 PFM/PWM |
| $20_H$ | D02 | 0: DD3 Fixed PWM (*1)<br>1: DD3 PFM/PWM |
| $20_H$ | D03 | Out of use |

*1: Preset value

## 21.6 ON/OFF for DC/DC

- Address $30_H$ is allocated as a register for the DC/DC ON/OFF.
- The DC/DC ON/OFF is controlled by writing data to address $30_H$.



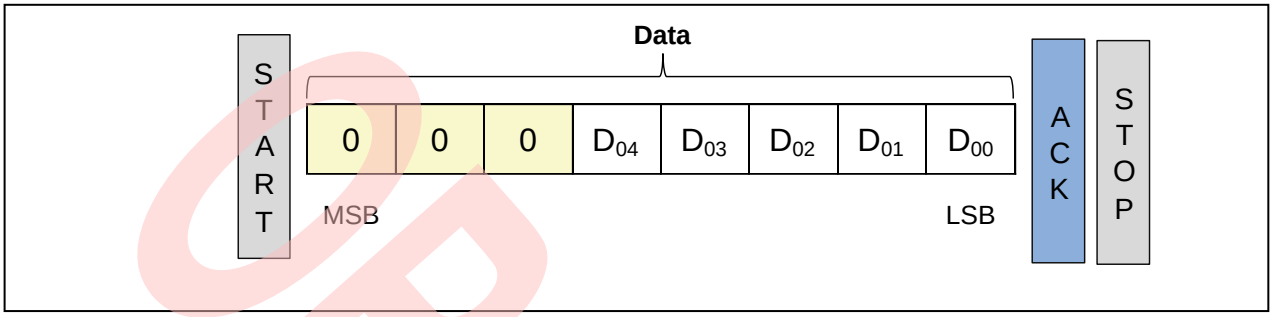

address$30_H$: For DC/DC ON/OFF
$D_{02}$ to $D_{00}$: Set ON/OFF for DC/DC

| Address | Bit | Description |
|---|---|---|
| $30_H$ | D00 | 0: DD1 output OFF (*1)<br>1: DD1 output ON |
| $30_H$ | D01 | 0: DD2 output OFF (*1)<br>1: DD2 output ON |
| $30_H$ | D02 | 0: DD3 output OFF (*1)<br>1: DD3 output ON |
| $30_H$ | D03 | Out of use |

*1: Preset value

## 21.7 About Error Monitor

- Address $40_H$ is allocated as error status monitor of each DC/DC output and thermal shut down.
- Address $40_H$ is read only resistor.



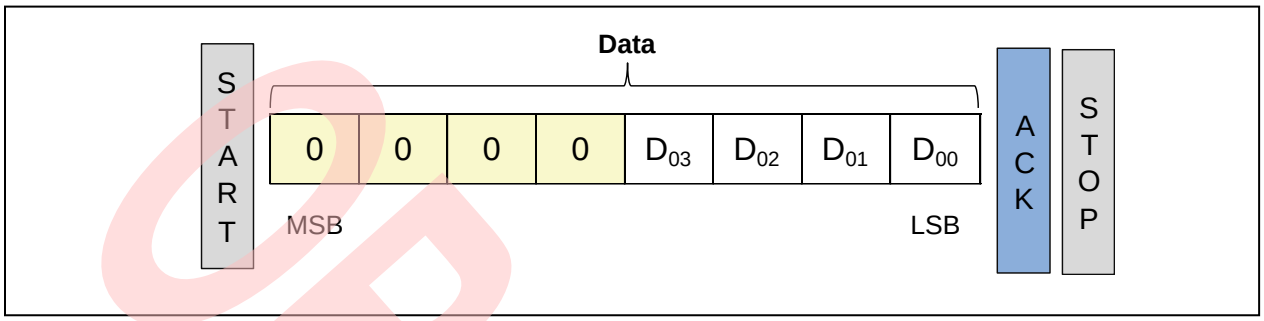

address$40_H$: For error monitor of each DC/DC output and thermal shut down
$D_{04}$ to $D_{00}$: read only resistor. (Not allowed write resistor)

| Address | Bit | Description |
|---|---|---|
| $40_H$ | D00 | 0: DD1 OCP non detection (*1)<br>1: DD1 OCP detection |
| $40_H$ | D01 | 0: DD2 OCP non detection (*1)<br>1: DD2 OCP detection |
| $40_H$ | D02 | 0: DD3 OCP non detection (*1)<br>1: DD3 OCP detection |
| $40_H$ | D03 | Out of use |
| $40_H$ | D04 | 0: TSD non detection (*1)<br>1: TSD detection |

*1:Preset value

## 21.8 About Power Good Monitor

- Address $50_H$ is allocated as output monitor of each DC/DC output.
- Address $50_H$ is read only resistor.

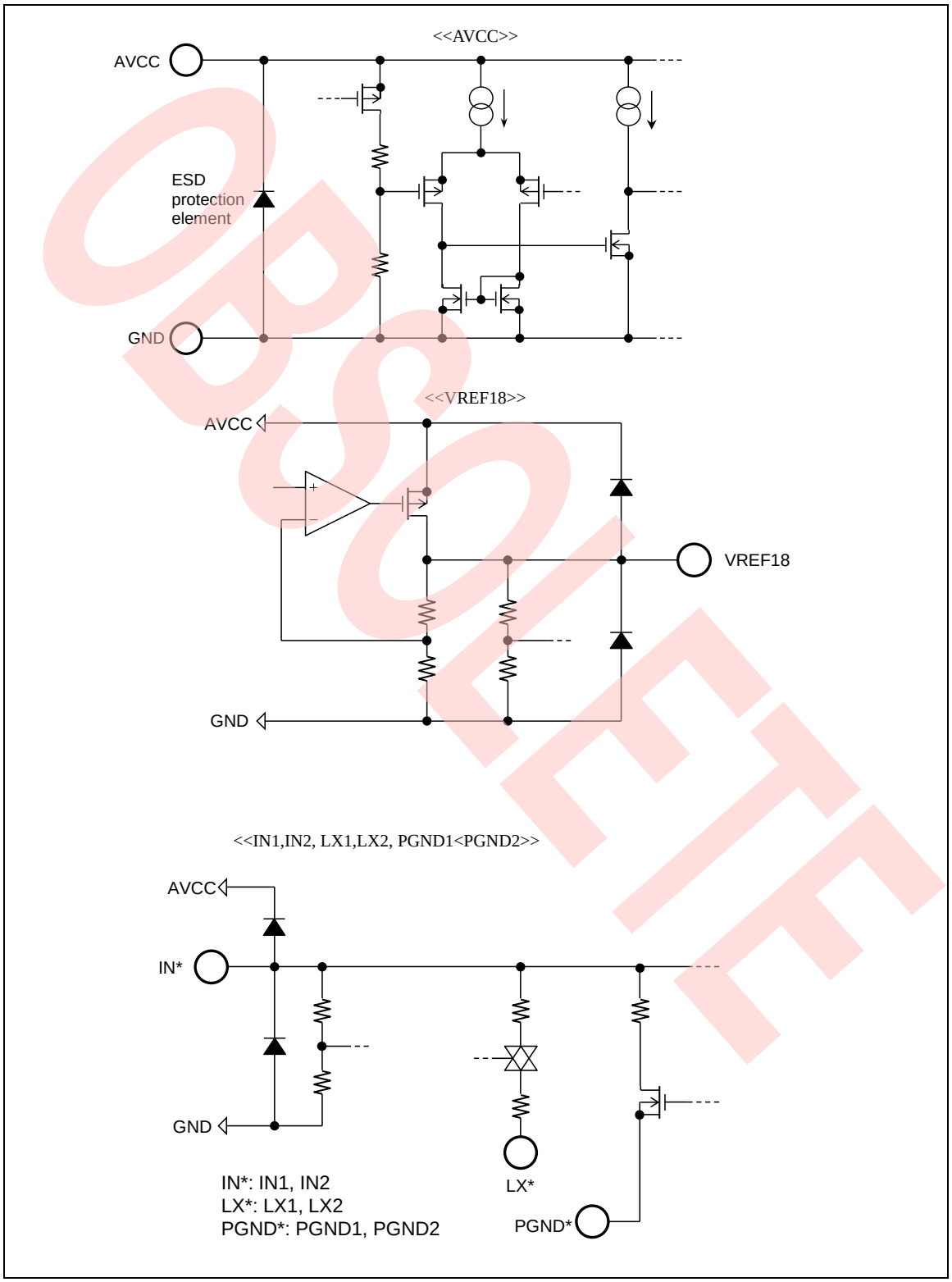


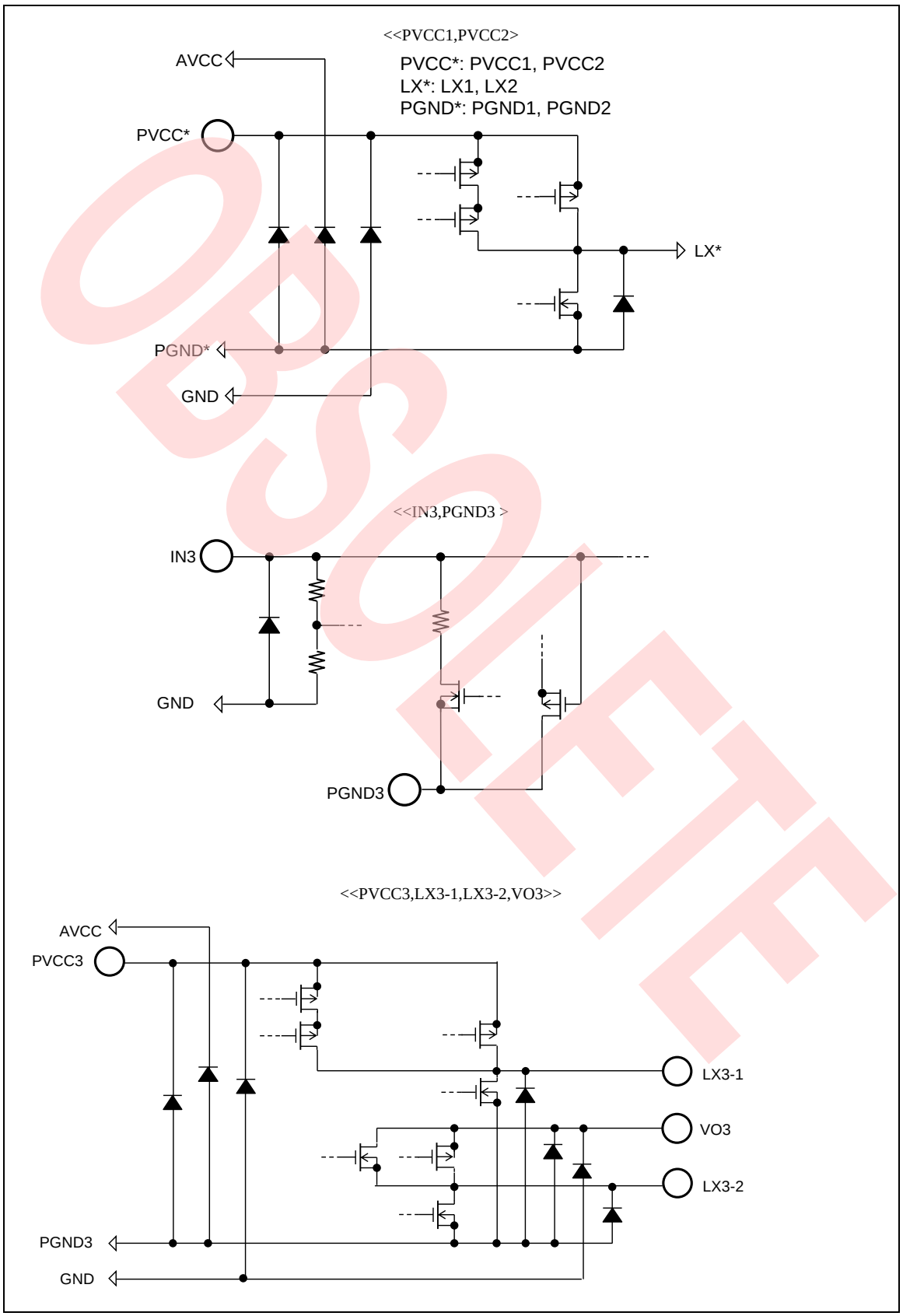

address$50_H$: For output monitor of each DC/DC output.
Detection level is over 93% of DCDC output voltage setting.
$D_{04}$ to $D_{00}$: read only resistor. (Not allowed write resistor)

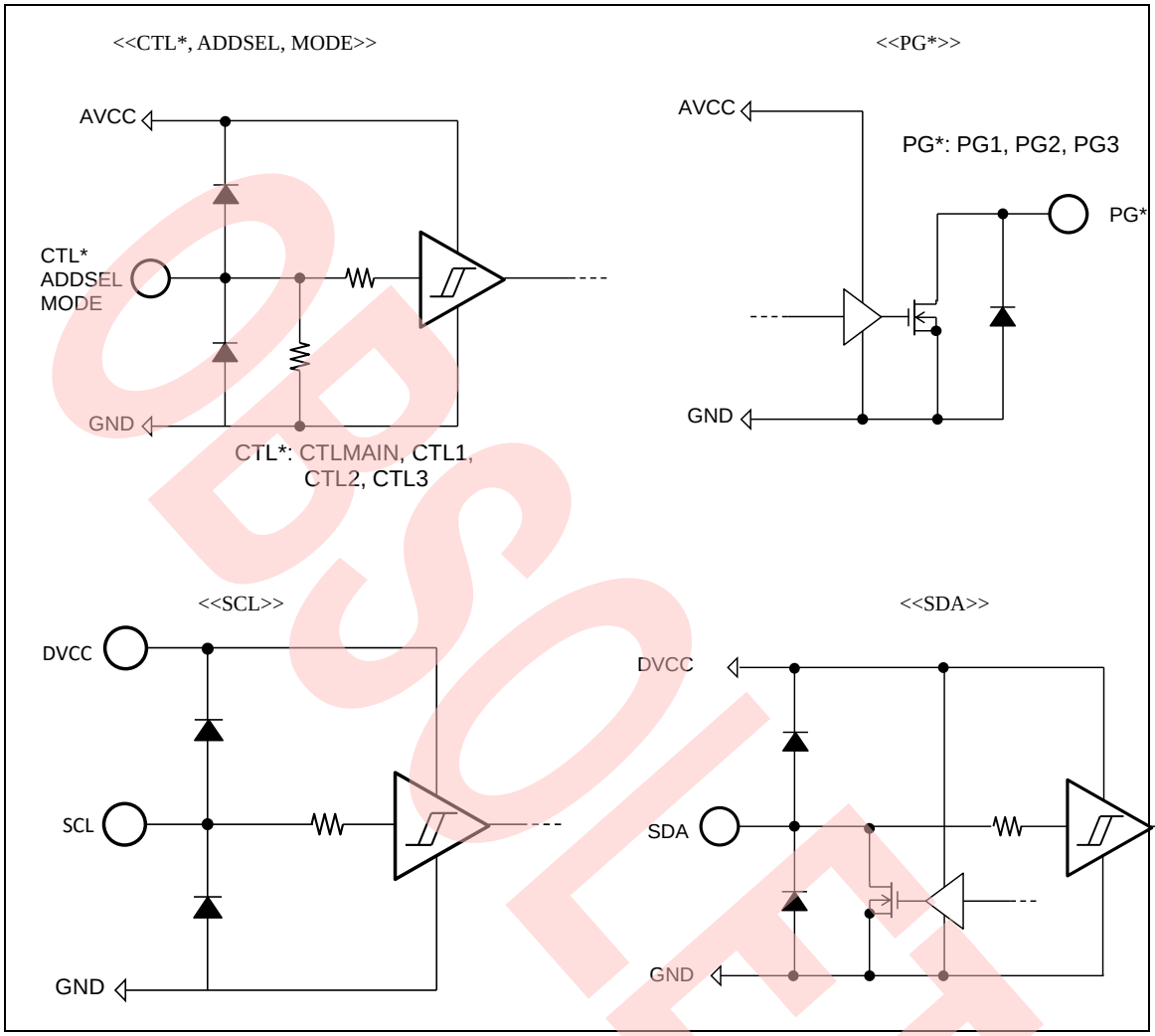
| Address | Bit | Description |
|---|---|---|
| $50_H$ | D00 | 0: DD1 non output (*1)<br>1: DD1 output |
| $50_H$ | D01 | 0: DD2 non output (*1)<br>1: DD2 output |
| $50_H$ | D02 | 0: DD3 non output (*1)<br>1: DD3 output |
| $50_H$ | D03 | Out of use |

*1: Preset value

## 22. I/O Pin Equivalent Circuit Diagram




<<PVCC1,PVCC2>
AVCC
PVCC*: PVCC1, PVCC2
LX*: LX1, LX2
PGND*: PGND1, PGND2
PVCC*
LX*
PGND*
GND
<<IN3,PGND3 >
IN3
GND
PGND3
<<PVCC3,LX3-1,LX3-2,VO3>>
AVCC
PVCC3
LX3-1
VO3
LX3-2
PGND3
GND


<<CTL*, ADDSEL, MODE>>
AVCC
CTL*
ADDSEL
MODE
GND
CTL*: CTLMAIN, CTL1, CTL2, CTL3
<<PG*>>
AVCC
PG*: PG1, PG2, PG3
PG*
GND
<<SCL>>
DVCC
SCL
GND
<<SDA>>
DVCC
SDA
GND

## 23. Measurement Circuit for Characteristics of General Operation

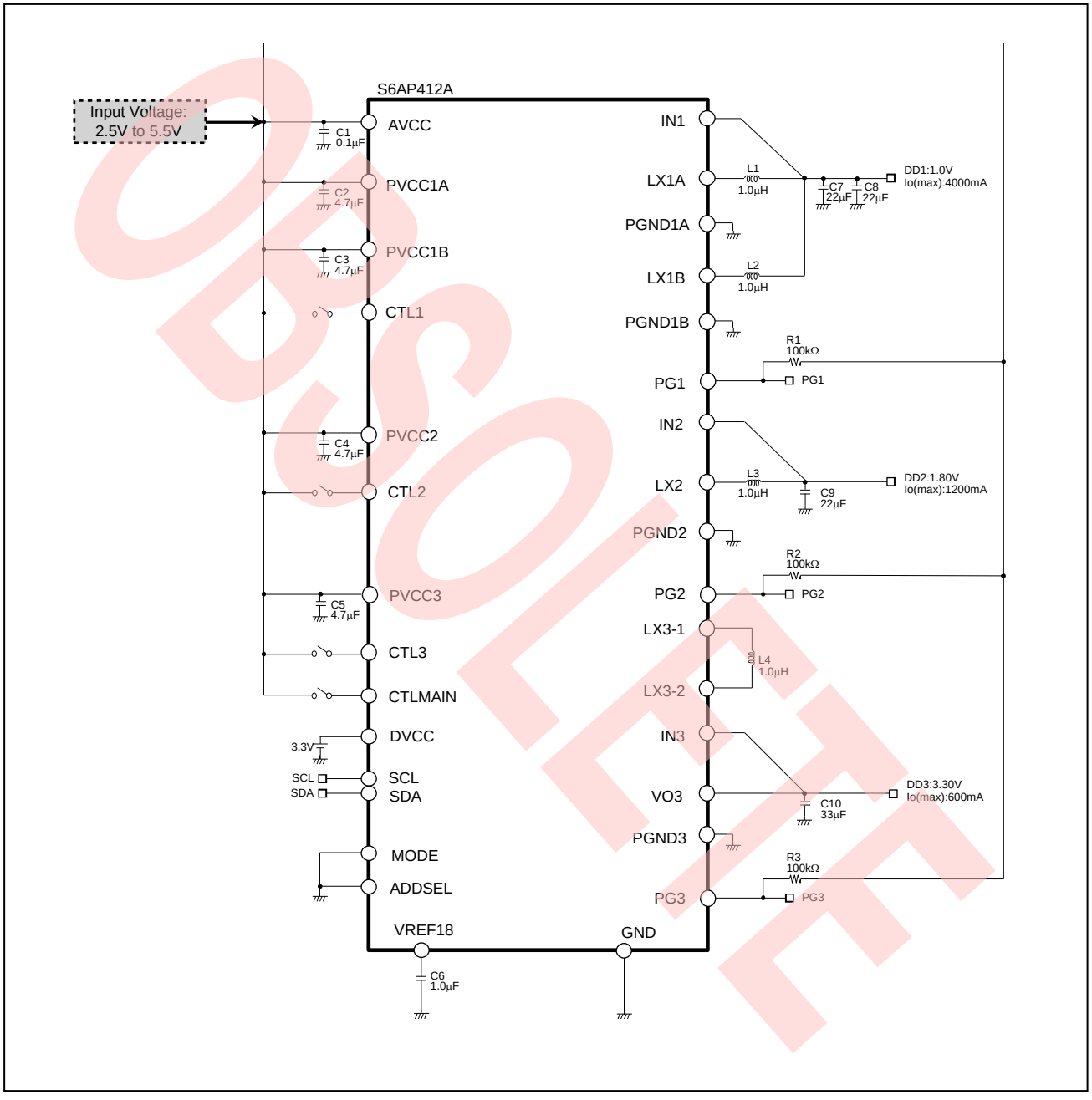


**Table 3. Parts list**

| Symbol | Parts | Part number | Specifications | Vendor |
|---|---|---|---|---|
| L1 | Inductor | 1276AS-H-1R0M | 1.0µH | TOKO |
| L2 | Inductor | 1276AS-H-1R0M | 1.0µH | TOKO |
| L3 | Inductor | 1276AS-H-1R0M | 1.0µH | TOKO |
| L4 | Inductor | 1276AS-H-1R0M | 1.0µH | TOKO |
| C1 | Ceramic Capacitor | C1608X5R1H104K | 0.1µF | TDK |
| C2 | Ceramic Capacitor | C1608X5R1V475K | 4.7µF | TDK |
| C3 | Ceramic Capacitor | C1608X5R1V475K | 4.7µF | TDK |
| C4 | Ceramic Capacitor | C1608X5R1V475K | 4.7µF | TDK |
| C5 | Ceramic Capacitor | C1608X5R1V475K | 4.7µF | TDK |
| C6 | Ceramic Capacitor | C2012X5R1A336M | 1.0µF | TDK |
| C7 | Ceramic Capacitor | C1608X5R1H105K | 22µF | TDK |
| C8 | Ceramic Capacitor | C1608X5R1H105K | 22µF | TDK |
| C9 | Ceramic Capacitor | C1608X5R1H105K | 22µF | TDK |
| C10 | Ceramic Capacitor | C2012X5R1A336M | 33µF | TDK |
| R1 | Resistor | RR0816P-104-D | 100kΩ | SSM |
| R2 | Resistor | RR0816P-104-D | 100kΩ | SSM |
| R3 | Resistor | RR0816P-104-D | 100kΩ | SSM |

TOKO : TOKO, INC.
TDK : TDK Corporation
SSM : SUSUMU CO., LTD.

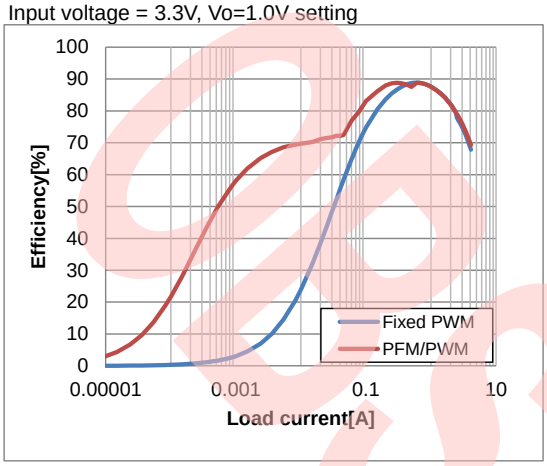
# 24. Reference Data

## DCDC Convertor Efficiency Data

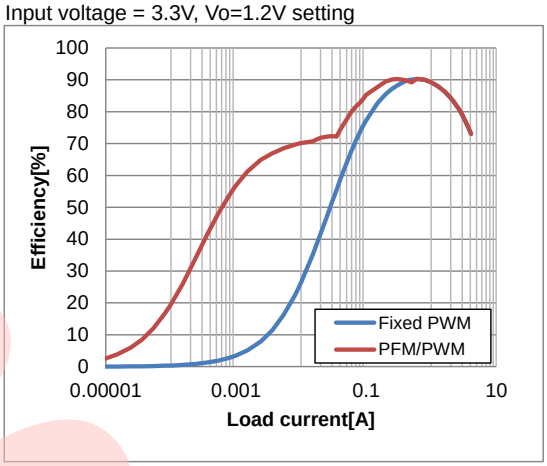
Inductor and capacitor value refer to section 26.

■ **DD1**

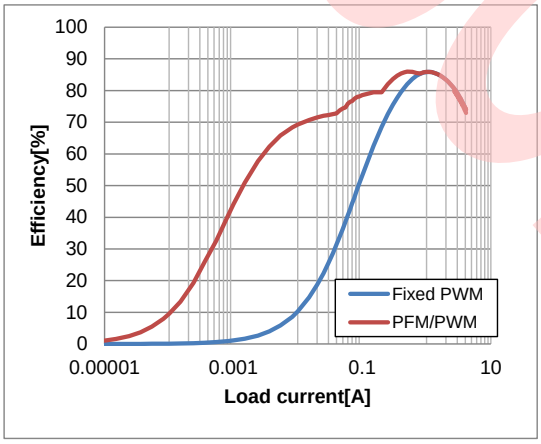
Input voltage = 3.3V, Vo=1.0V setting



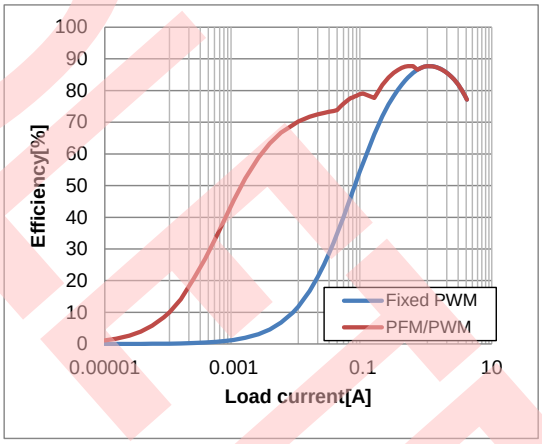

Input voltage = 3.3V, Vo=1.2V setting




Input voltage = 5.5V, Vo = 1.0V setting

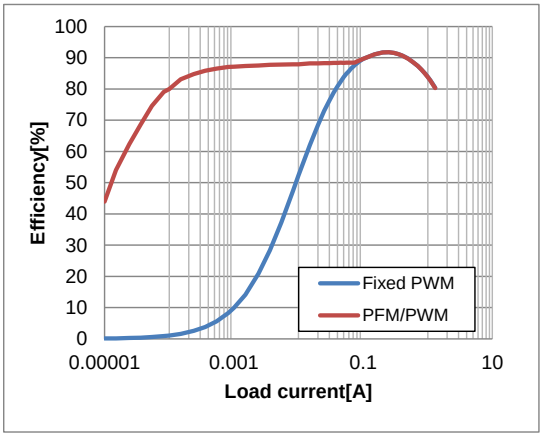



Input voltage = 5.5V, Vo = 1.2V setting

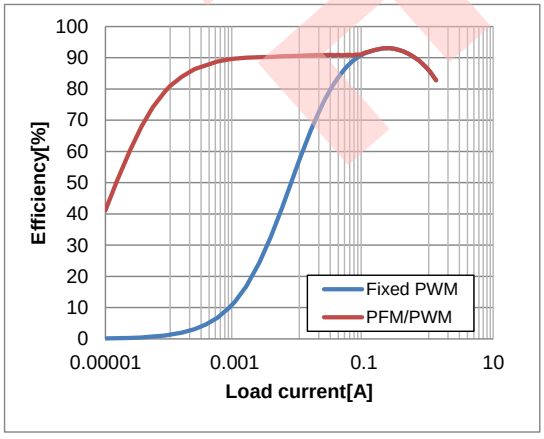



■ **DD2**

Input Voltage = 3.3V, Vo = 1.5V setting

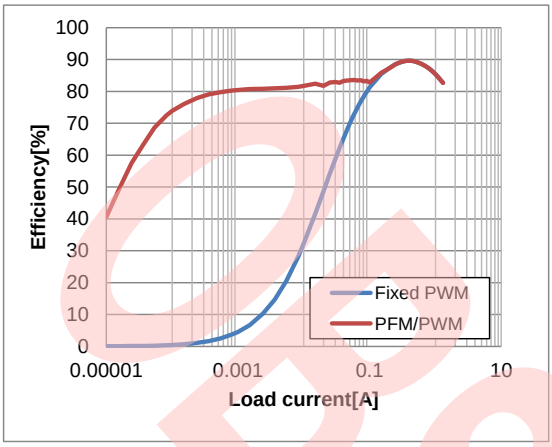



Input voltage = 3.3V, Vo = 1.8V setting

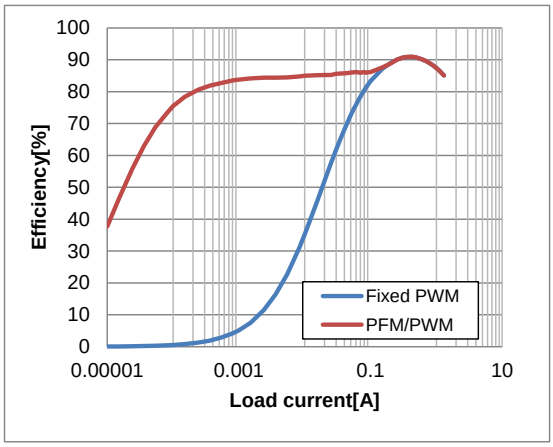


■ **DD2**

Input voltage = 5.5V, Vo = 1.5V setting

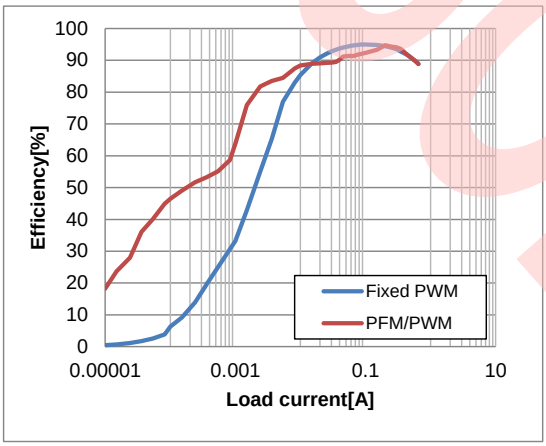



Input Voltage = 5.5V, Vo = 1.8V setting

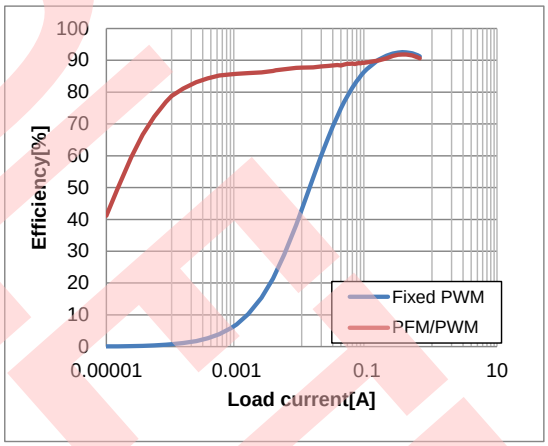



■ **DD3**

Input voltage = 3.3V, Vo = 3.3V setting



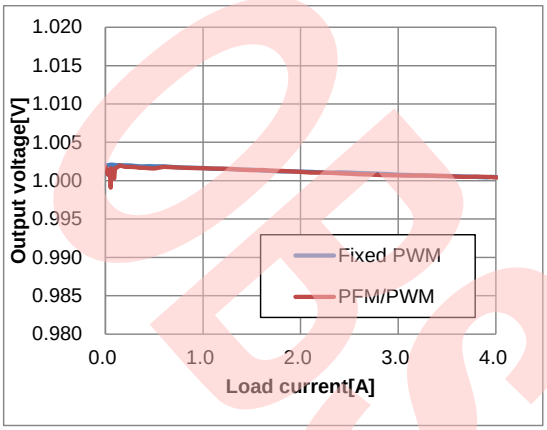

Input Voltage = 5.5V, Vo = 3.3V setting



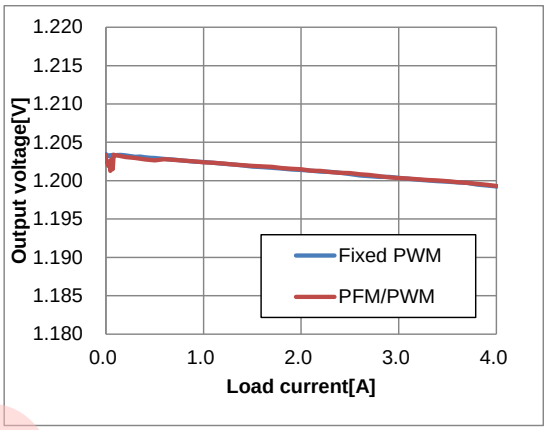
## DCDC Convertor Regulation Data

■ **DD1**

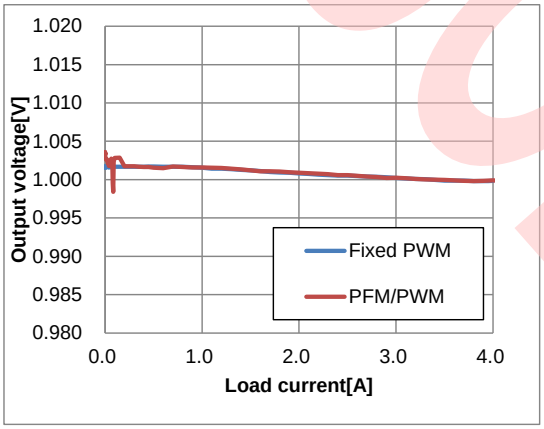
Input voltage = 3.3V, Vo = 1.0V setting



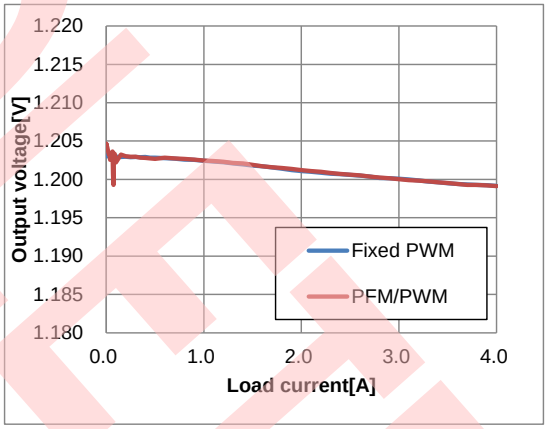

Input voltage = 3.3V, Vo=1.2V setting




Input voltage = 5.5V, Vo = 1.0V setting

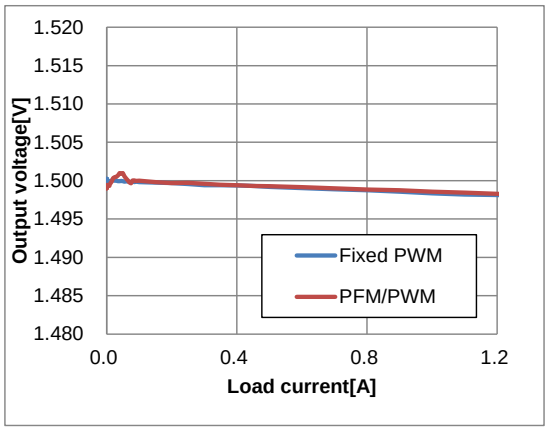



Input voltage = 5.5V, Vo = 1.2V setting

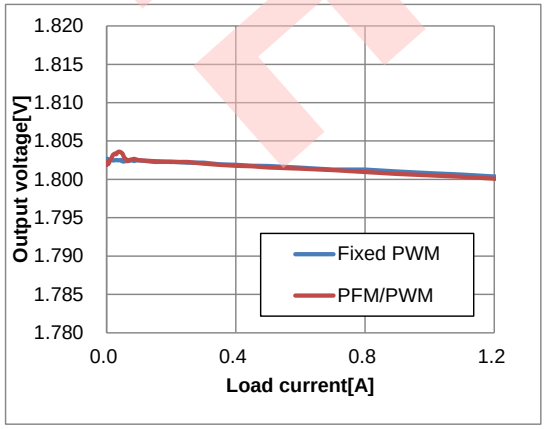



■ **DD2**

Input Voltage = 3.3V, Vo = 1.5V setting

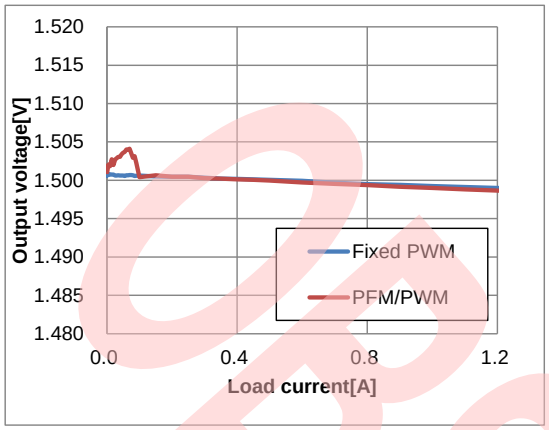



Input voltage = 3.3V, Vo = 1.8V setting

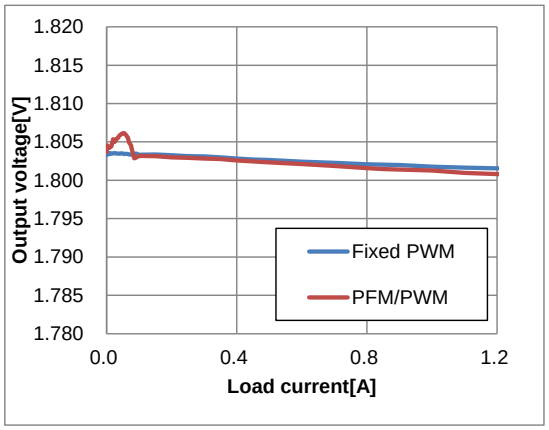


■ **DD2**

Input voltage = 5.5V, Vo = 1.5V setting

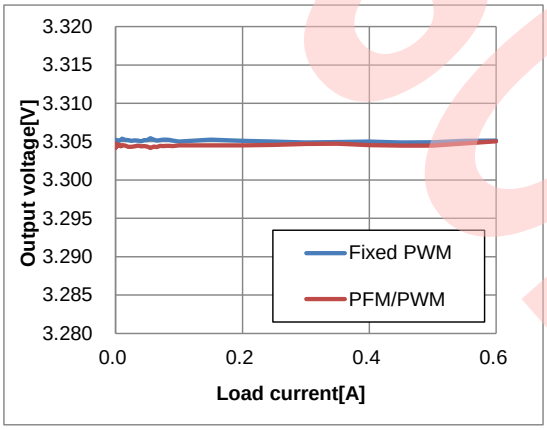



Input Voltage = 5.5V, Vo = 1.8V setting

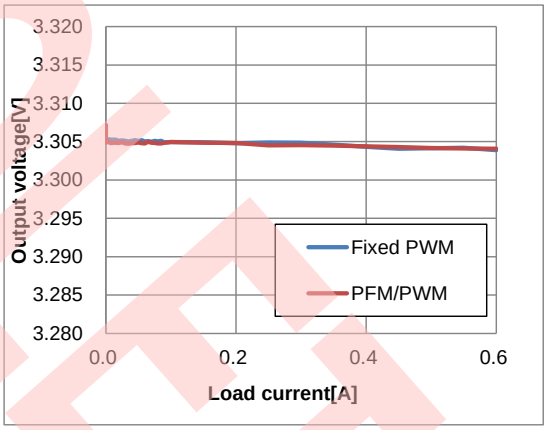



■ **DD3**

Input voltage = 3.3V, Vo = 3.3V setting



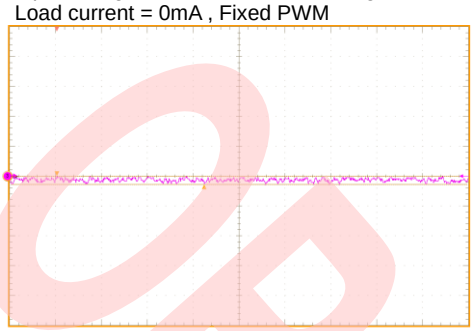

Input Voltage = 5.5V, Vo = 3.3V setting



### DCDC Convertor Output Ripple Voltage

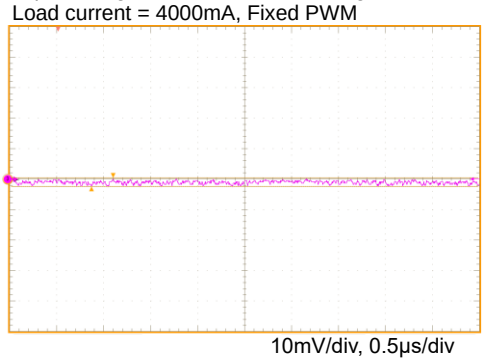
■ **DD1**

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 0mA , Fixed PWM



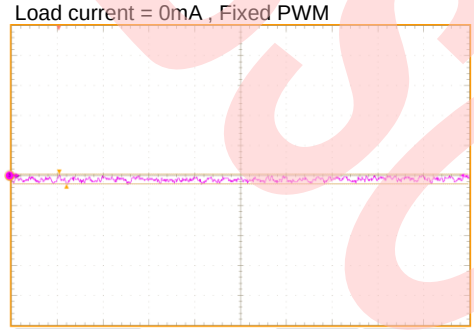
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo=1.0V setting
Load current = 4000mA, Fixed PWM



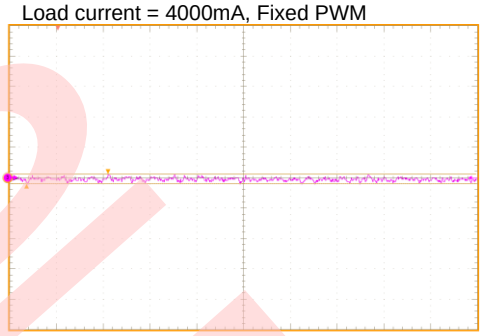
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 0mA , Fixed PWM



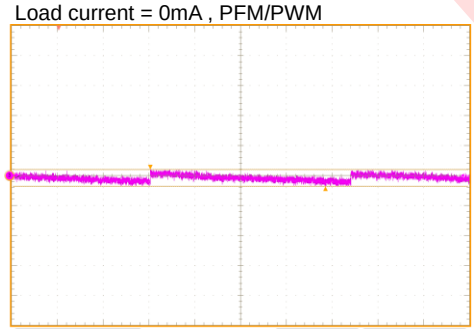
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 4000mA, Fixed PWM



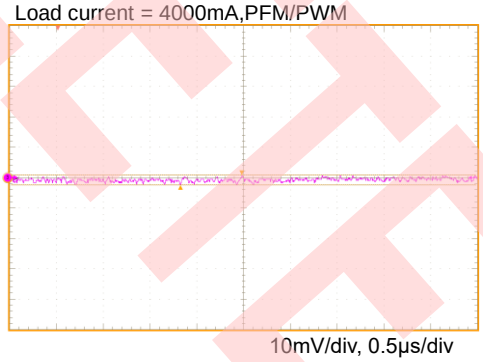
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 0mA , PFM/PWM



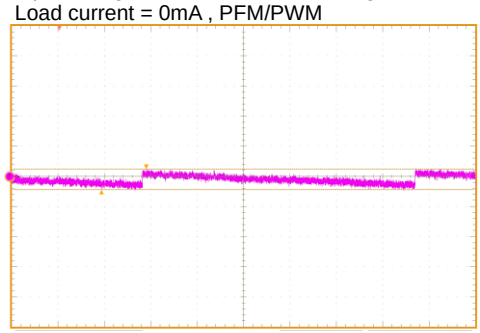
10mV/div, 2ms/div

Input voltage = 3.3V, Vo=1.0V setting
Load current = 4000mA,PFM/PWM



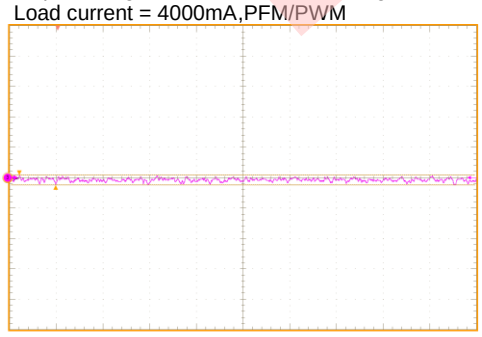
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

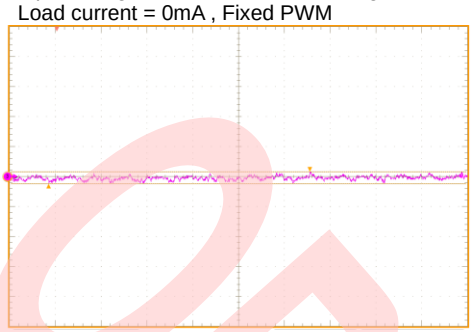
Input voltage = 5.5V, Vo = 1.0V setting
Load current = 4000mA,PFM/PWM



10mV/div, 0.5µs/div

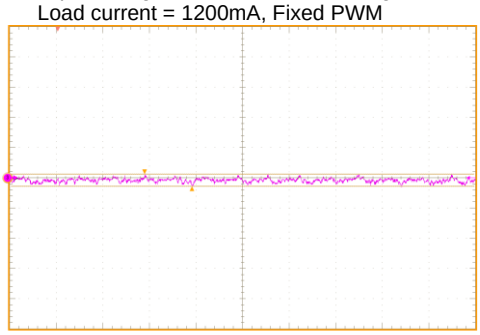
■ **DD2**

Input voltage = 3.3V, Vo = 1.8V setting
Load current = 0mA , Fixed PWM



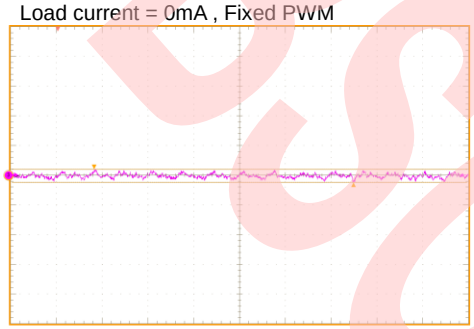
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo=1.8V setting
Load current = 1200mA, Fixed PWM



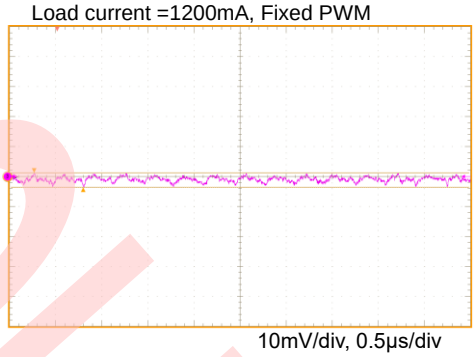
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting
Load current = 0mA , Fixed PWM



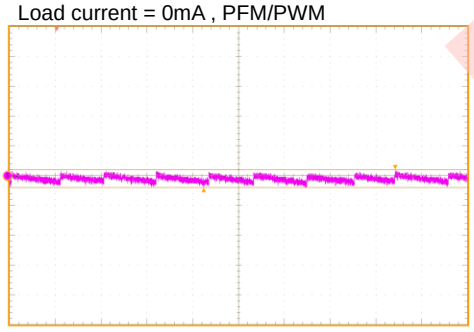
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting
Load current =1200mA, Fixed PWM



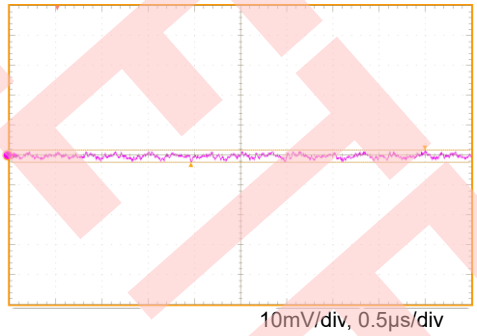
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo = 1.8V setting
Load current = 0mA , PFM/PWM



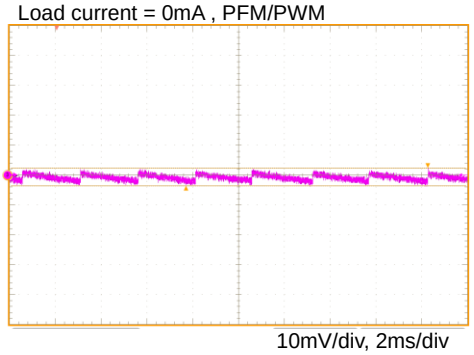
10mV/div, 2ms/div

Input voltage = 3.3V, Vo=1.8V setting
Load current =1200mA,PFM/PWM



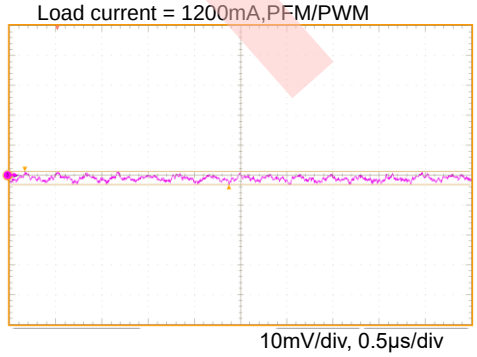
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.8V setting
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

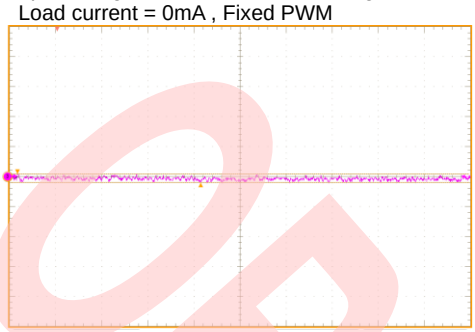
Input voltage = 5.5V, Vo = 1.8V setting
Load current = 1200mA,PFM/PWM



10mV/div, 0.5µs/div

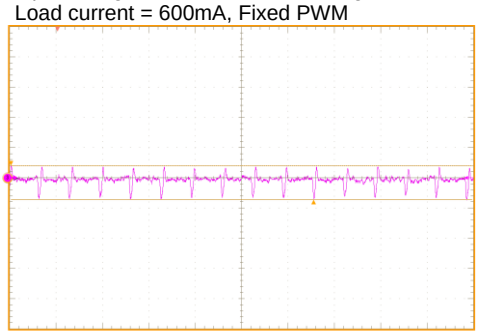
■ DD3

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 0mA , Fixed PWM



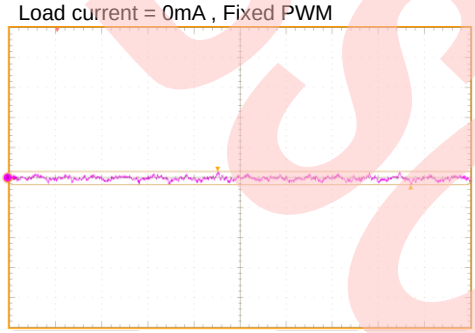
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo=3.3V setting
Load current = 600mA, Fixed PWM



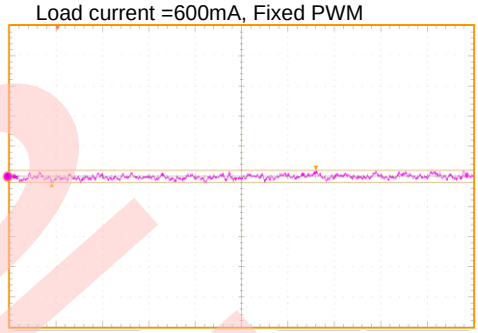
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 3.3V setting
Load current = 0mA , Fixed PWM



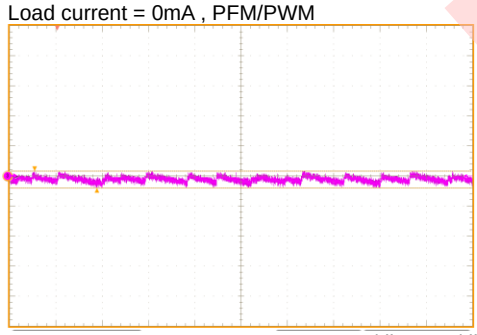
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 3.3V setting
Load current =600mA, Fixed PWM



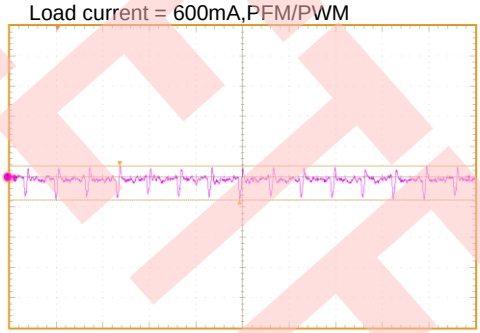
10mV/div, 0.5µs/div

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 0mA , PFM/PWM



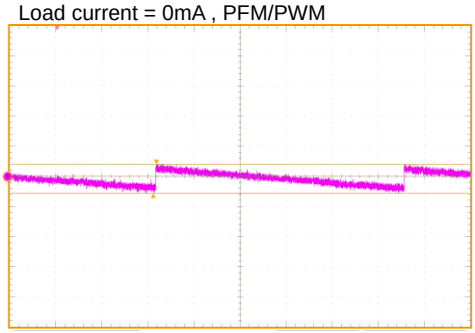
10mV/div, 2ms/div

Input voltage = 3.3V, Vo=3.3V setting
Load current = 600mA,PFM/PWM



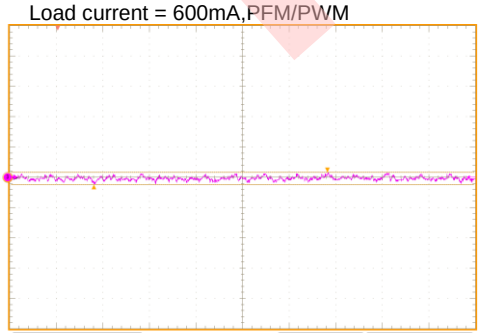
10mV/div, 0.5µs/div

Input voltage = 5.5V, Vo = 1.0V setting
Load current = 0mA , PFM/PWM



10mV/div, 2ms/div

Input voltage = 3.3V, Vo =3.3V setting
Load current = 600mA,PFM/PWM

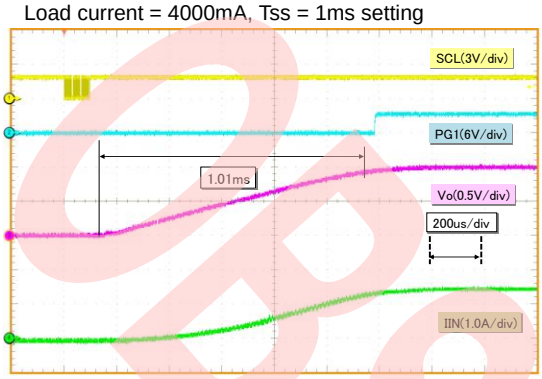


10mV/div, 0.5µs/div

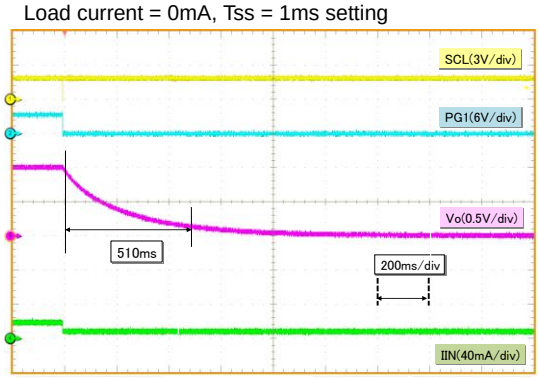
## DCDC Convertor Enable/Disable

### ■ DD1(Fixed PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 4000mA, Tss = 1ms setting

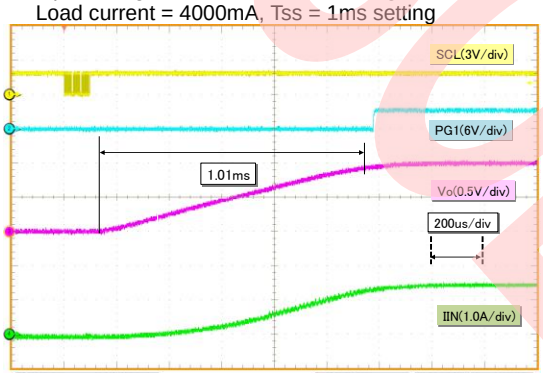



Input voltage = 3.3V, Vo=1.0V setting
Load current = 0mA, Tss = 1ms setting

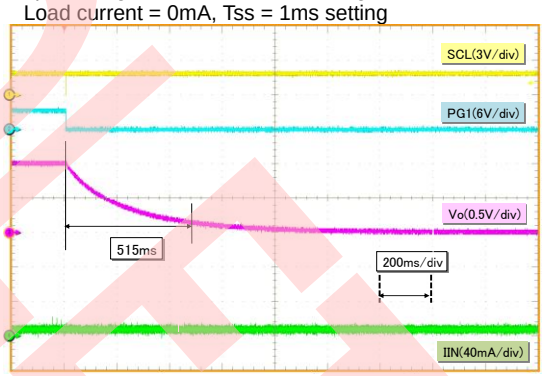



### ■ DD1(PFM/PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = 4000mA, Tss = 1ms setting

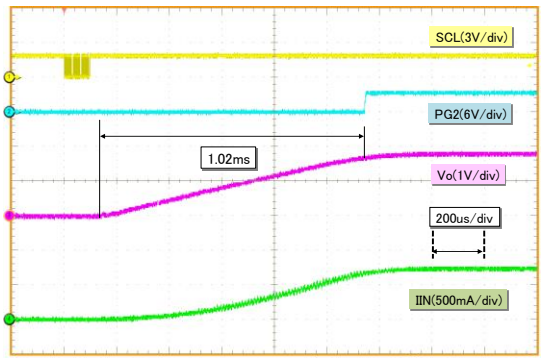



Input voltage = 3.3V, Vo=1.0V setting
Load current = 0mA, Tss = 1ms setting

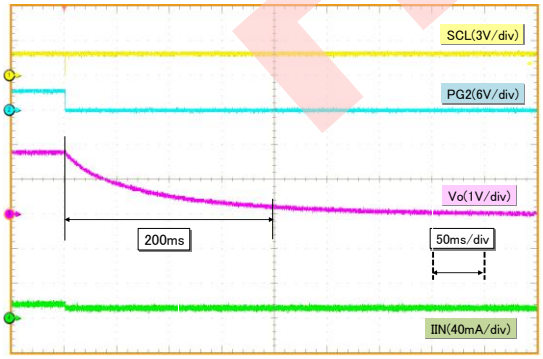



### ■ DD2(Fixed PWM)

Input voltage = 3.3V, Vo = 1.8V setting
Load current = 1200mA, Tss = 1ms setting

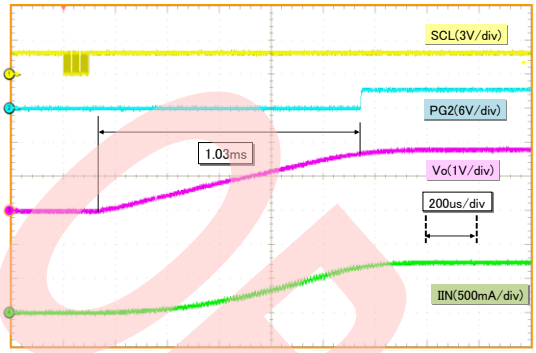



Input voltage = 3.3V, Vo=1.8V setting
Load current = 0mA, Tss = 1ms setting

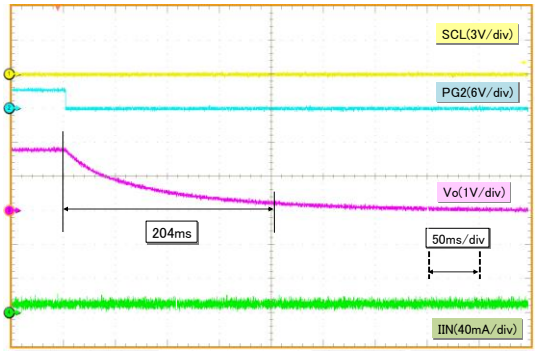


■ **DD2(PFM/ PWM)**

Input voltage = 3.3V, Vo = 1.8V setting
Load current = 1200mA, Tss = 1ms setting

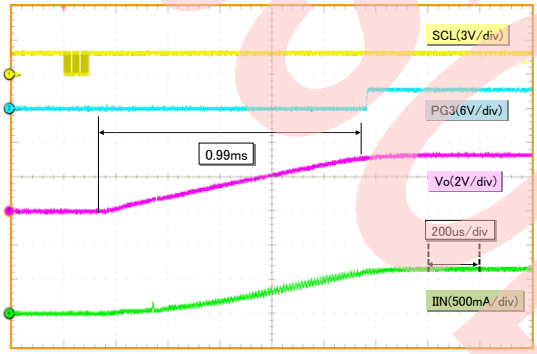



Input voltage = 3.3V, Vo=1.8V setting
Load current = 0mA, Tss = 1ms setting

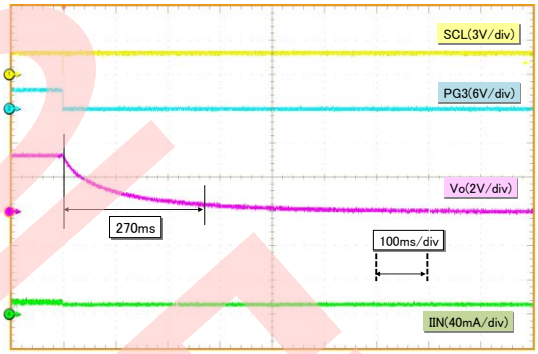



■ **DD3 (Fixed PWM)**

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 600mA, Tss = 1ms setting

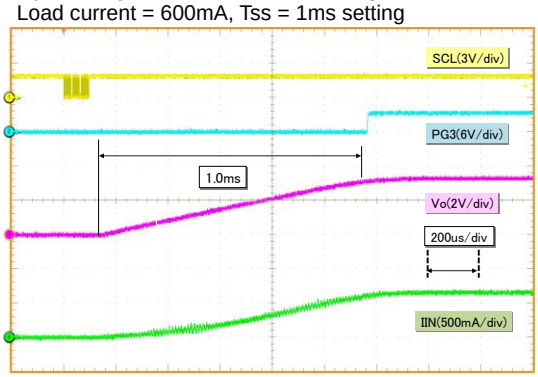



Input voltage = 3.3V, Vo=3.3 V setting
Load current = 0mA, Tss = 1ms setting

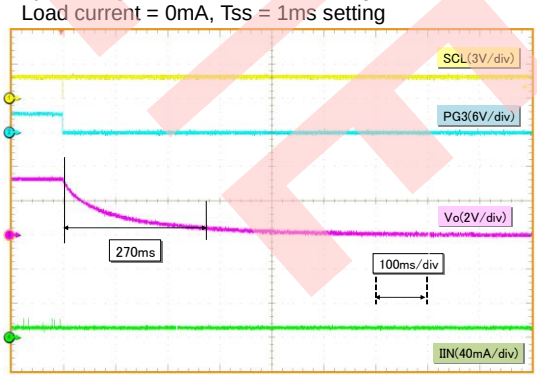



■ **DD3 (Fixed PWM)**

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 600mA, Tss = 1ms setting



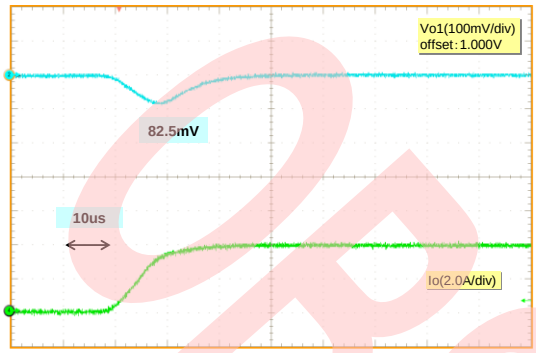

Input voltage = 3.3V, Vo=3.3 V setting
Load current = 0mA, Tss = 1ms setting



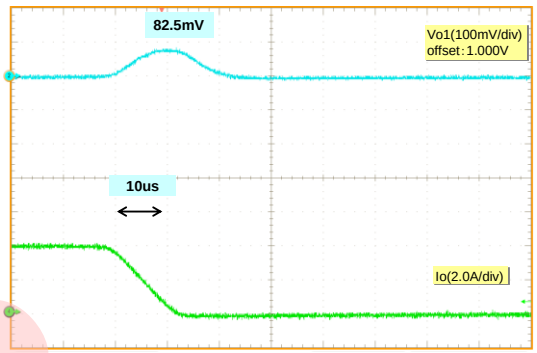
## DCDConvertor Load Transient

### ■ DD1(Fixed PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = from 0mA to 4000mA per 10us

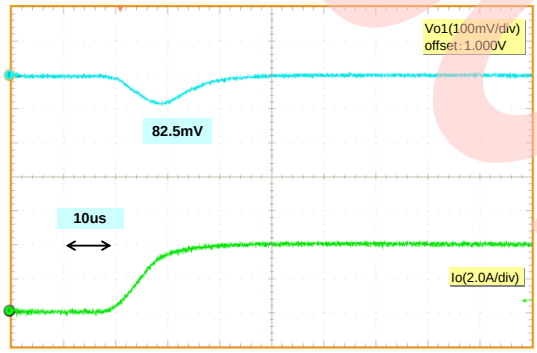



Input voltage = 3.3V, Vo=1.0V setting
Load current = from 4000mA to 0mA per 10us

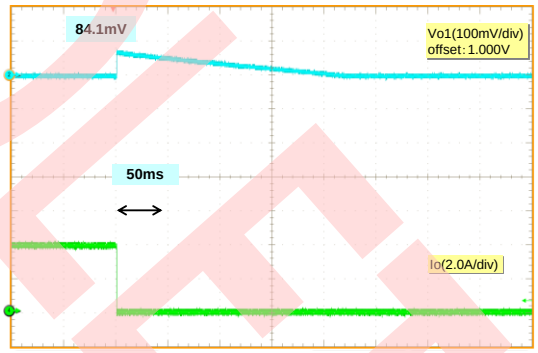



### ■ DD1(PFM/PWM)

Input voltage = 3.3V, Vo = 1.0V setting
Load current = from 0mA to 4000mA per 10us

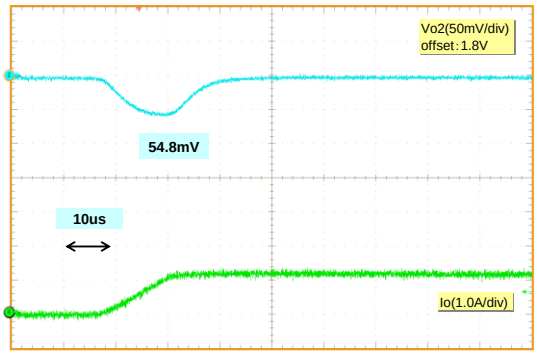



Input voltage = 3.3V, Vo=1.0V setting
Load current = from 4000mA to 0mA per 10us

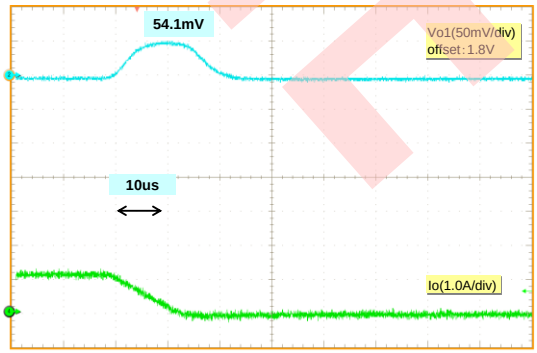



### ■ DD2(Fixed PWM)

Input voltage = 3.3V, Vo = 1.8V setting
Load current = from 0mA to 1200mA per 10us

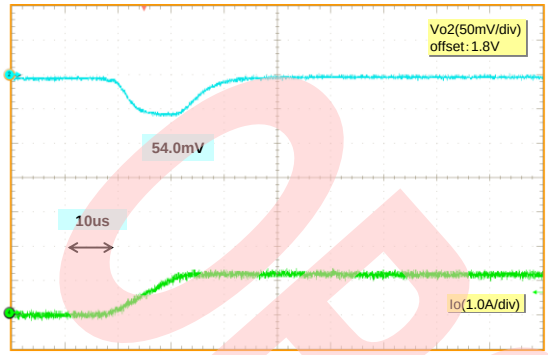



Input voltage = 3.3V, Vo=1.8V setting
Load current = from 1200mA to 0mA per 10us

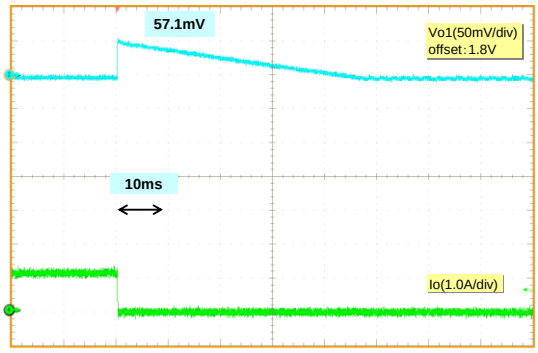


■ **DD2(PFM/ PWM)**

Input voltage = 3.3V, Vo = 1.8V setting
Load current = from 0mA to 1200mA per 10us

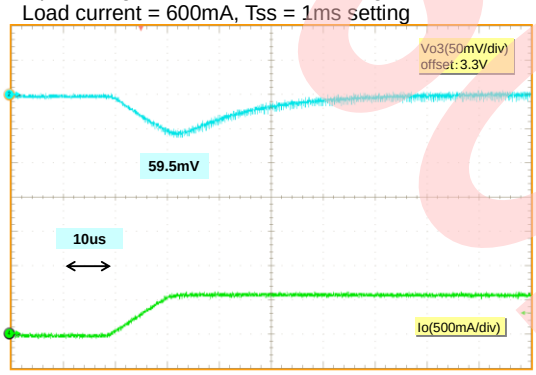



Input voltage = 3.3V, Vo=1.8V setting
Load current = from 1200mA to 0mA per 10us

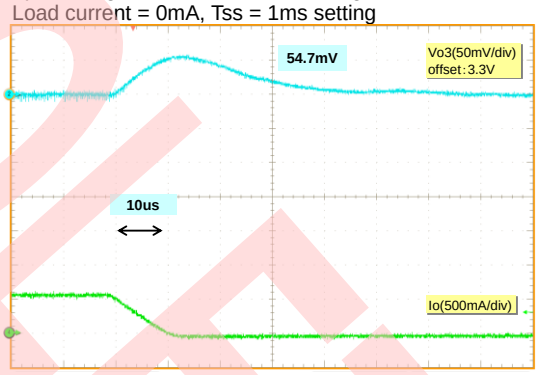



■ **DD3 (Fixed PWM)**

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 600mA, Tss = 1ms setting

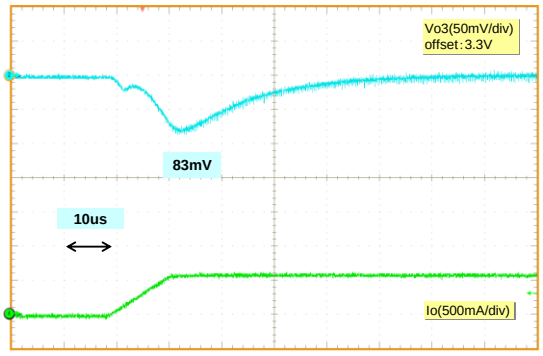



Input voltage = 3.3V, Vo=3.3 V setting
Load current = 0mA, Tss = 1ms setting

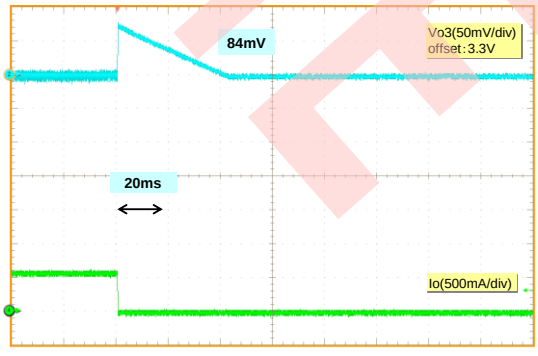



■ **DD3 (Fixed PWM)**

Input voltage = 3.3V, Vo = 3.3V setting
Load current = 600mA, Tss = 1ms setting




Input voltage = 3.3V, Vo=3.3 V setting
Load current = 0mA, Tss = 1ms setting

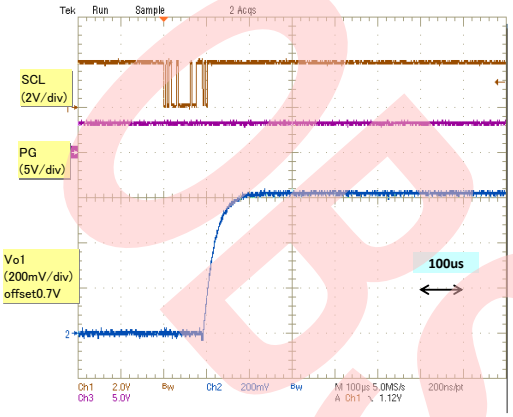


**DCDC Convertor DVFS Function**

■ DD1 (Fixed PWM)

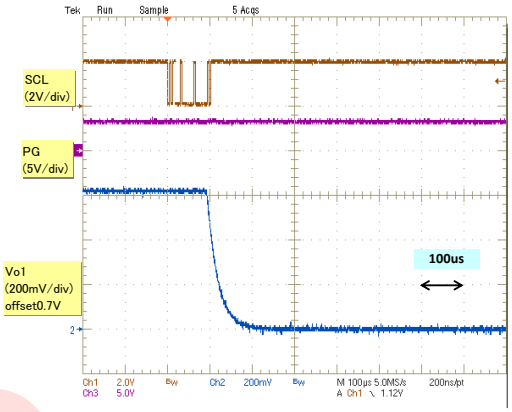
Input voltage = 3.3V,

Vo =from 0.7V to 1.32V setting by I²C




Input voltage = 3.3V

Vo =from 1.32V to 0.7V setting by I²C



## 25. Ordering Information

**Table 4. Ordering Information**

| Part Number | Package | Remarks |
|---|---|---|
| S6AP412A18GN1C000 | 32-pin plastic QFN (WNT032) | |
| S6AP412A28GN1C000 | | |
| S6AP412A38GN1C000 | | |
| S6AP412A58GN1C000 | | |
| S6AP412A68GN1C000 | | |
| S6AP412A78GN1C000 | | |
| S6AP412A98GN1C000 | | |
| S6AP412AA8GN1C000 | | |
| S6AP412AB8GN1C000 | | |
| S6AP412AD8GN1C000 | | |
| S6AP412AE8GN1C000 | | |
| S6AP412AF8GN1C000 | | |

## 26. Preset Code List

| Preset Code | DD1 Output Voltage Preset Code Value | DD2 Output Voltage Preset Code Value | DD3 Output Voltage Preset Code Value |
|---|---|---|---|
| 18 | 0.90V | 1.35V | 3.30V |
| 28 | 0.90V | 1.50V | 3.30V |
| 38 | 0.90V | 1.80V | 3.30V |
| 58 | 1.00V | 1.35V | 3.30V |
| 68 | 1.00V | 1.50V | 3.30V |
| 78 | 1.00V | 1.80V | 3.30V |
| 98 | 1.10V | 1.35V | 3.30V |
| A8 | 1.10V | 1.50V | 3.30V |
| B8 | 1.10V | 1.80V | 3.30V |
| D8 | 1.20V | 1.35V | 3.30V |
| E8 | 1.20V | 1.50V | 3.30V |
| F8 | 1.20V | 1.80V | 3.30V |

## 27. Layout

Consider the points listed below and do the layout design.

- Provide the ground plane as much as possible on the IC mounted face. GND and PGNDx provide the through hole proximal to GND and PGNDx pins of IC, and connect it with GND of internal layer.
- Provide the power plane as much as possible to lower impedance of VCC.
- Play the most attention to the loop composed of input capacitor (CPVCCx) and SWFET. Input capacitor (CPVCCx) connected with PVCCx should be placed close to the pin as much as possible to make the current loop as small as possible. Also connect the GND pin of the input capacitor with PGNDx.
- Output capacitor (CVO3) connected with VO3 should be placed close to the pin as much as possible. Also connect the GND pin of the output capacitor with PGND3.
- GND pins of the switching system parts provide the through hole at the proximal place, and connect it with GND of internal layer.
- By-pass capacitor (CVREF, CAVCC) connected with VREF and AVCC should be placed close to the pin as much as possible. Also connect the GND pin of the by-pass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the INx pin of the IC separately from near the output capacitor pin, whenever possible. Consider the line connected with INx pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
- There is leaked magnetic flux around the inductor or backside of place equipped with inductor.

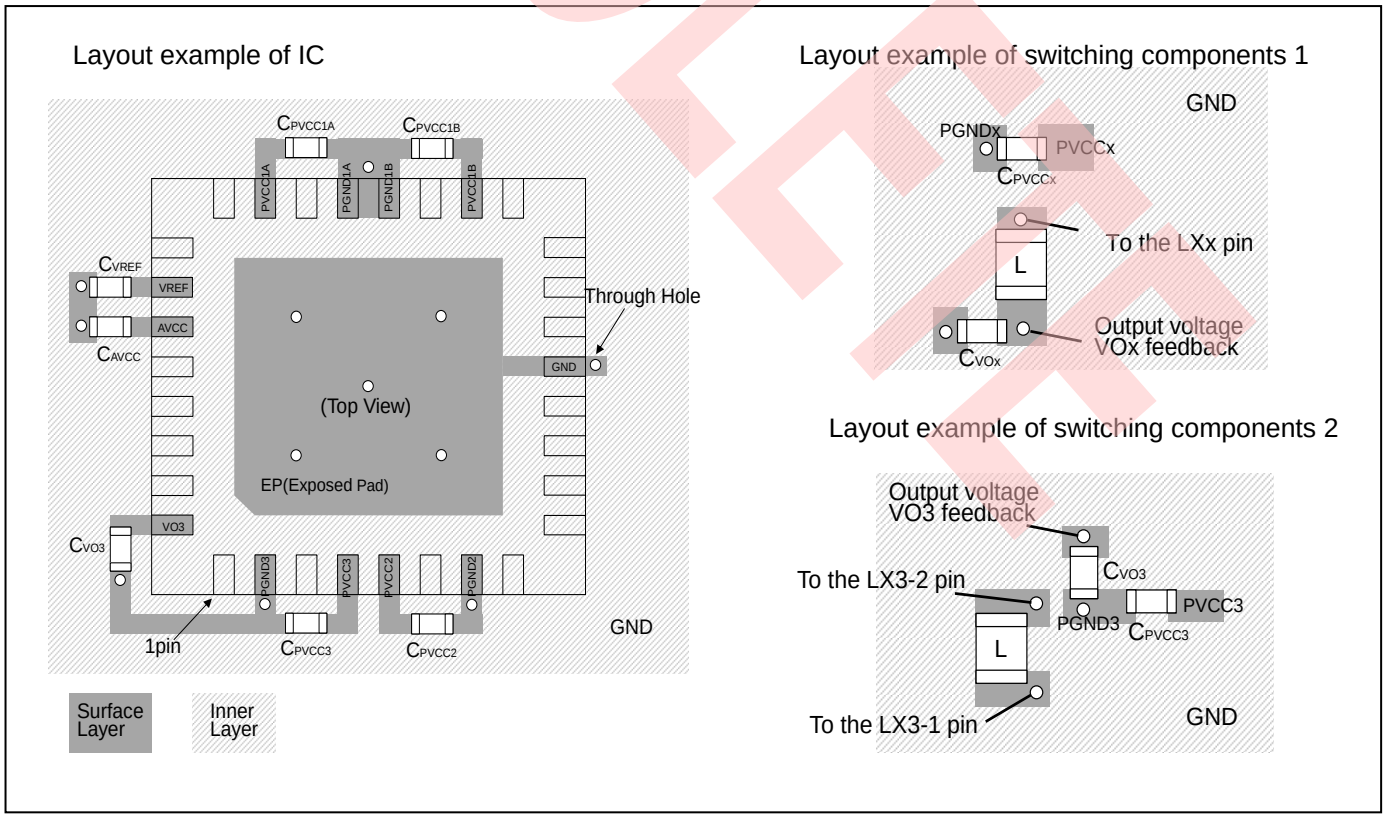
Line and parts sensitive to noise should be considered to be placed away from the inductor (or backside of place equipped with inductor).

Switching system parts: Input capacitor(CPVCCx), Inductor(L), Output capacitor(CVOx)

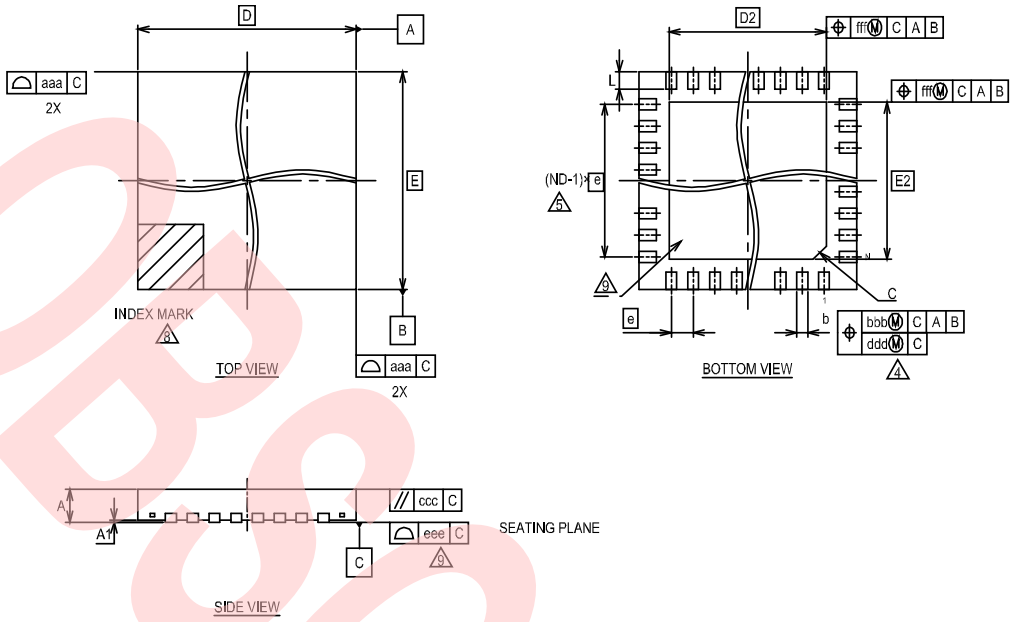
**Note:**

- x: Each channel number

Figure 6. Layout Example



## 28. Package Dimensions




| SYMBOL | MILLIMETER | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | — | — | 0.75 | PROFILE |
| $A_1$ | 0.00 | — | 0.05 | TERMINAL HEIGHT |
| D | | 5.00 BSC. | | BODY SIZE |
| E | | 5.00 BSC. | | BODY SIZE |
| b | 0.20 | 0.25 | 0.30 | TERMINAL WIDTH |
| $D_2$ | | 3.60 BSC. | | EXPOSED PAD SIZE |
| $E_2$ | | 3.60 BSC. | | EXPOSED PAD SIZE |
| e | | 0.50 BSC. | | TERMINAL PITCH |
| n | | 32 | | TERMINAL COUNT |
| L | 0.33 | 0.40 | 0.47 | TERMINAL LENGTH |
| C | | C0.30 | | EXPOSED PAD CHAMFER |
| aaa | | 0.07 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| ddd | | 0.05 | | |
| eee | | 0.05 | | |
| fff | | 0.10 | | |

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

## 29. Major Changes

**Spansion Publication Number: S6AP412A_DS405-00018**

| Page | Section | Change Results |
|---|---|---|
| Revision 0.1 | | |
| - | - | Initial release |
| Revision 1.0 | | |
| - | - | Preliminary → Full production |
| 50 | 26. Measurement Circuit for Characteristics of General Operation | Revised the Parts number of Component list<br>1278AS-H-1R0M → 1276AS-H-1R0M |
| 63 | 28. Ordering Information | Revised the Part number of Ordering Information |

**NOTE: Please see "Document History" about later revised information.**

## Document History

**Document Title: S6AP412A 3ch DC/DC Converter with I²C Interface and Internal SW FETs**
**Document Number: 002-08447**

| Revision | ECN | Submission Date | Description of Change |
|---|---|---|---|
| ** | – | 12/26/2014 | Migrated to Cypress and assigned document number 002-08447.<br>No change to document contents or format. |
| *A | 5157734 | 03/28/2016 | Updated to Cypress template |
| *B | 6767186 | 01/06/2020 | Updated to template and completing Sunset review. |
| *C | 6895534 | 06/09/2020 | This Spec to be Obsolete.<br>Reason: All the MPNs in the datasheet are Obsolete/Prune. |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Arm® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

### PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

### Cypress Developer Community

Community | Code Examples | Projects | Videos | Blogs | Training | Components

### Technical Support

cypress.com/support



ARM and Cortex are the registered trademarks of ARM Limited in the EU and other countries.