FAIRCHILD SEMICONDUCTOR®

May 2007

74VHC221A
Dual Non-Retriggerable Monostable Multivibrator

Features

- High Speed: t_{PD} = 8.1ns (Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4µA (Max.) at T_A = 25°C
- Active State: I_{CC} = 600µA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC221A

General Description

The VHC221A is an advanced high speed CMOS Monostable Multivibrator fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken LOW resets the one-shot. The VHC221A can be triggered on the positive transition of the clear while A is held LOW and B is held HIGH. The VHC221A is non-retriggerable, and therefore cannot be retriggered until the output pulse times out. The output pulse width is determined by the equation:

PW = (Rx)(Cx)

where,

PW is in seconds, R is in ohms, and C is in farads.

Limits for R_x and C_x are:

External capacitor, C_x: No limit

External resistors, R_x: V_{CC} = 2.0V, 5kΩ Min.
V_{CC} > 3.0V, 1 kΩ Min

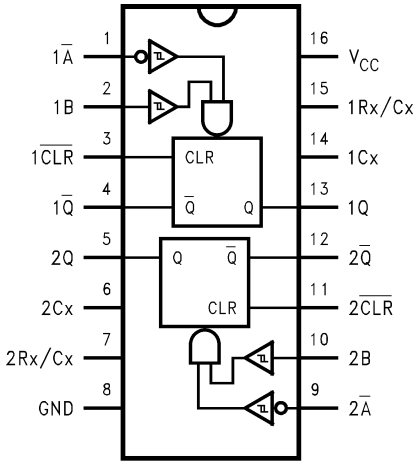
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

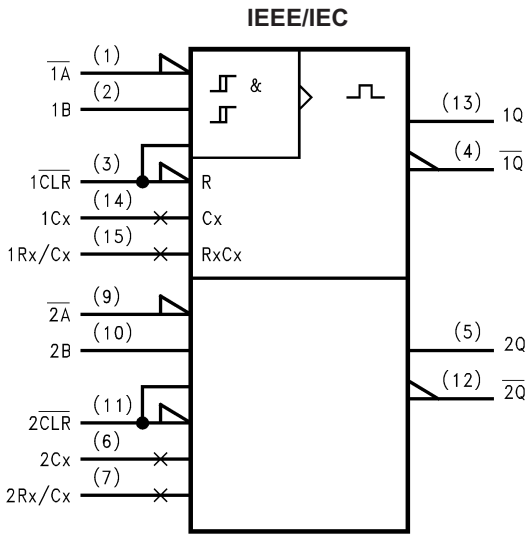
Order Number	Package Number	Package Description
74VHC221AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC221ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC221AMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Logic Symbol



Truth Table

Inputs			Outputs		Function
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↘	H	H	⎍	⎌	Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L	↗	H	⎍	⎌	Output Enable
L	H	↗	⎍	⎌	Output Enable
X	X	L	L	H	Reset

H = HIGH Voltage Level

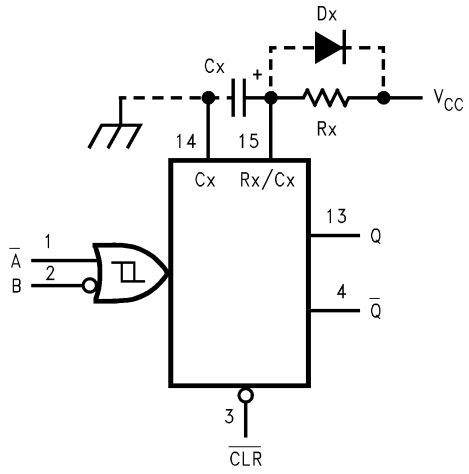
L = LOW Voltage Level

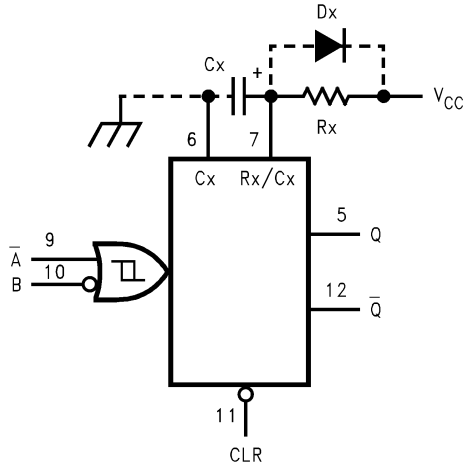
↘ = HIGH-to-LOW Transition

↗ = LOW-to-HIGH Transition

X = Don't Care

Block Diagrams





Note A: Cx, Rx, Dx are external Capacitor, Resistor, and Diode, respectively.

Note B: External clamping diode, Dx;

External capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, Cx discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

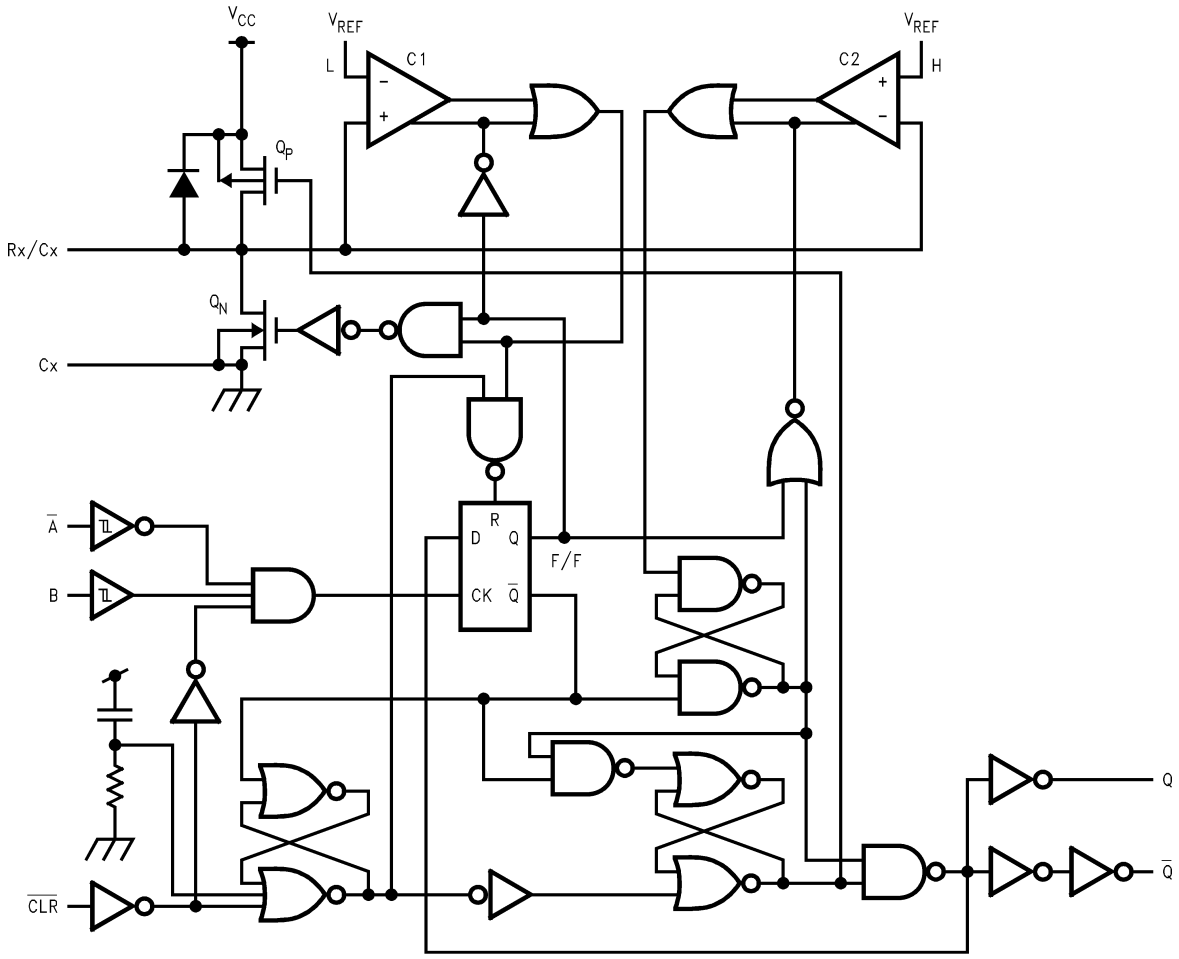
The maximum value of forward current through the parasitic diode is ±20 mA. In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$t_f \geq (V_{CC} - 0.7)\ Cx / 20mA$

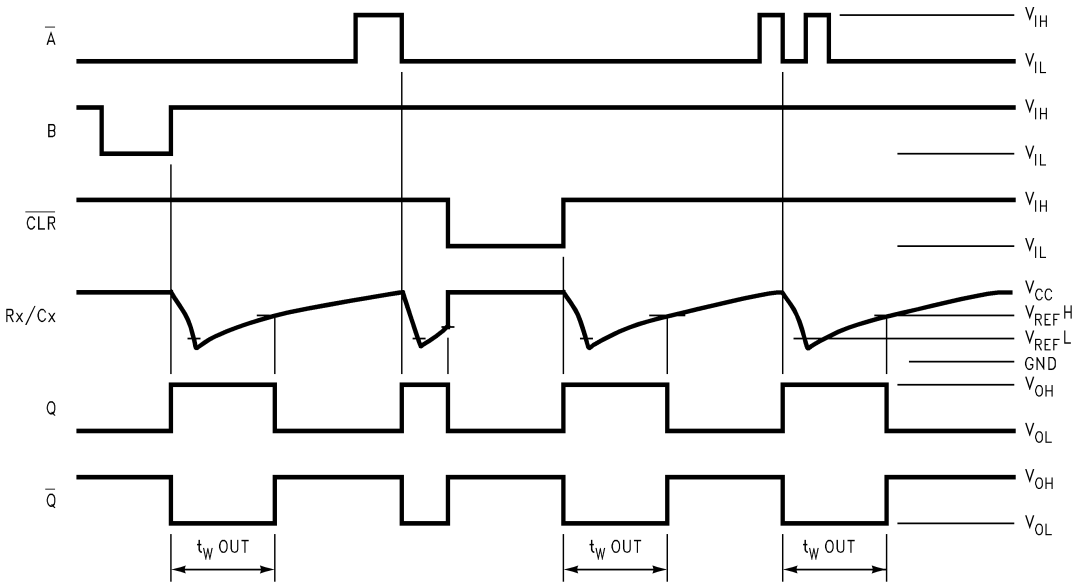
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC})

In the event a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

System Diagram



Timing Chart



Functional Description

1. Stand-by State

   The external capacitor (Cx) is fully charged to V_{CC} in the Stand-by State. That means, before triggering, the Q_P and Q_N transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

2. Trigger Operation

   Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is LOW, and B input has a rising signal; second, where the B input is HIGH, and the A input has a falling signal; and third, where the $\overline{A}$ input is LOW and the B input is HIGH, and the $\overline{CLR}$ input has a rising signal.

   After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage $V_{ref}L$, the output of C1 becomes LOW. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

   After Q_N turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

   Upon triggering, output Q becomes HIGH, following some delay time of the internal F/F and gates. It stays HIGH even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage $V_{ref}H$, the output of C2 becomes LOW, the output Q goes LOW and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx node reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

   With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_W (OUT), is as follows:

   t_W (OUT) = 1.0 Cx Rx

3. Reset Operation

   In normal operation, the $\overline{CLR}$ input is held HIGH. If $\overline{CLR}$ is LOW, a trigger has no affect because the Q output is held LOW and the trigger control F/F is reset. Also, Q_p turns on and Cx is charged rapidly to V_{CC}.

   This means if $\overline{CLR}$ is set LOW, the IC goes into a wait state.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time (CLR only) V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	 0ns/V ~ 100ns/V 0ns/V ~ 20ns/V
	External Capacitor, Cx	No Limitation(2) F
	External Resistor, Rx	>5kΩ(2) (V_{CC} = 2.0V) >1kΩ(2) (V_{CC} > 3.0V)

Notes:

1. Unused inputs must be held HIGH or LOW. They may not float.
2. The maximum allowable values of Cx and Rx are a function of the leakage of capacitor Cx, the leakage of the device, and leakage due to board layout and surface resistance.

   Susceptibility to externally induced noise signals may occur for Rx > 1 MΩ.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40° to 85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50µA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = –4mA	2.58			2.48		
		4.5		I_{OH} = –8mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50µA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4mA			0.36		0.44	
		4.5		I_{OL} = 8mA			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5V or GND				±0.1		±1.0	µA
I_{IN}	Rx/Cx Terminal Off-State Current	5.5	V_{IN} = V_{CC} or GND				±0.25		±2.50	µA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				4.0		40.0	µA
I_{CC}	Active—State[3] Supply Current	3.0	V_{IN} = V_{CC} or GND, Rx/Cx = 0.5 V_{CC}			160	250		280	µA
		4.5				380	500		650	
		5.5				560	750		975	

Note:

3. Per circuit.

AC Electrical Characteristics[4]

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time (A, B–Q, $\overline{Q}$)	3.3 ± 0.3	C_L = 15pF		13.4	20.6	1.0	24.0	ns
			C_L = 50pF		15.9	24.1	1.0	27.5	
		5.0 ± 0.5	C_L = 15pF		8.1	12.0	1.0	14.0	ns
			C_L = 50pF		9.6	14.0	1.0	16.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (CLR Trigger—Q, $\overline{Q}$)	3.3 ± 0.3	C_L = 15pF		14.5	22.4	1.0	26.0	ns
			C_L = 50pF		17.0	25.9	1.0	29.5	
		5.0 ± 0.5	C_L = 15pF		8.7	12.9	1.0	15.0	ns
			C_L = 50pF		10.2	14.9	1.0	17.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (CLR—Q, $\overline{Q}$)	3.3 ± 0.3	C_L = 15pF		10.3	15.8	1.0	18.5	ns
			C_L = 50pF		12.8	19.3	1.0	22.0	
		5.0 ± 0.5	C_L = 15pF		6.3	9.4	1.0	11.0	ns
			C_L = 50pF		7.8	11.4	1.0	13.0	
t_{WOUT}	Output Pulse Width	2.0	C_X = 28pF, C_L = 50pF, R_X = 6kΩ		415				
		3.3 ± 0.3			345				ns
		5.0 ± 0.5			312				
		3.3 ± 0.3	C_L = 50pF, Cx = 28pF, Rx = 2kΩ		160	240		300	ns
		5.0 ± 0.5			133	200		240	
		3.3 ± 0.3	C_L = 50pF, Cx = 0.01μF, Rx = 10kΩ	90	100	110	90	110	μs
		5.0 ± 0.5		90	100	110	90	110	
		3.3 ± 0.3	C_L = 50pF, Cx = 0.1μF, Rx = 10kΩ	0.9	1.0	1.1	0.9	1.1	ms
		5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1	
Δt_{wOUT}	Output Pulse Width Error Between Circuits (In same Package)				±1				%
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		(5)		73				pF

Notes:

4. Refer to 74VHC221A Timing Chart.

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

   I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + $I_{CC}{}^1$ • Duty / 100 + I_{CC} / 2 (per Circuit)

   $I_{CC}{}^1$: Active Supply Current

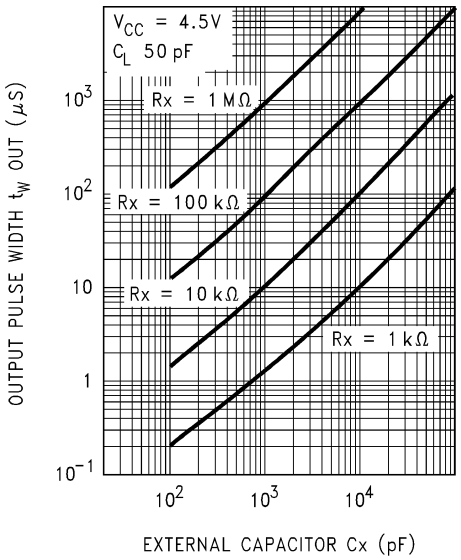
   Duty: %

AC Operating Requirement

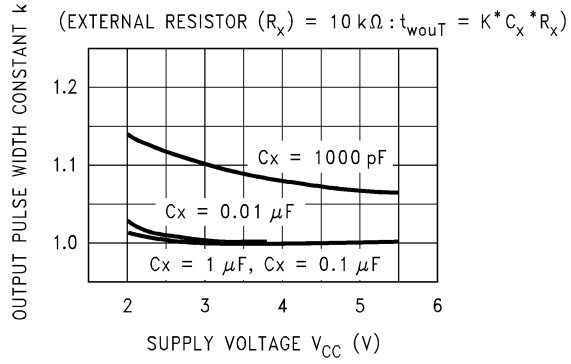
Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = –40°C to +85°C		Units
			Min.	Typ.	Max.	Min.	Max.	
t_W(L)	Minimum Trigger	3.3	5.0			5.0		ns
t_W(H)	Pulse Width	5.0	5.0			5.0		
t_W(L)	Minimum Clear Pulse Width	3.3	5.0			5.0		ns
		5.0	5.0			5.0		

Device Characteristics

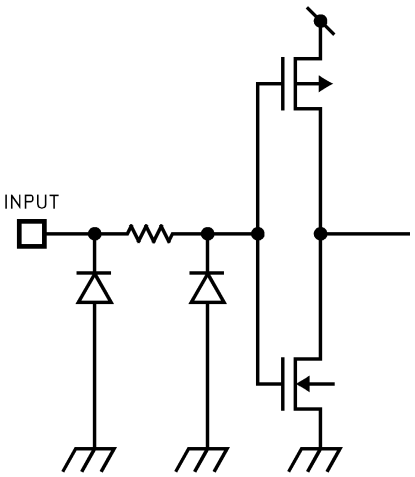
t_{wout}*C_x Characteristics (Typ.)



Output Pulse Width Constant K-Supply Voltage (Typical)



Input Equivalent Circuit



Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

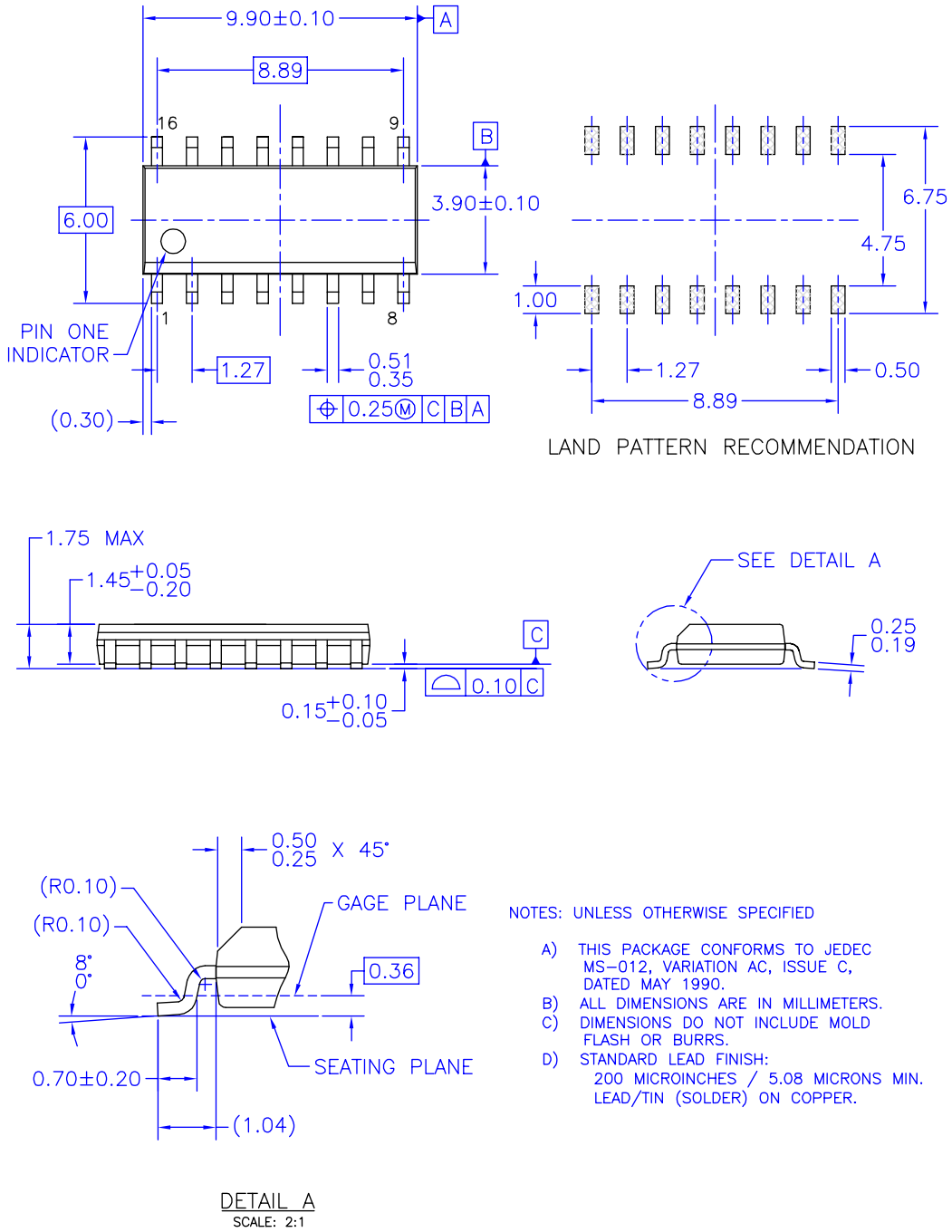
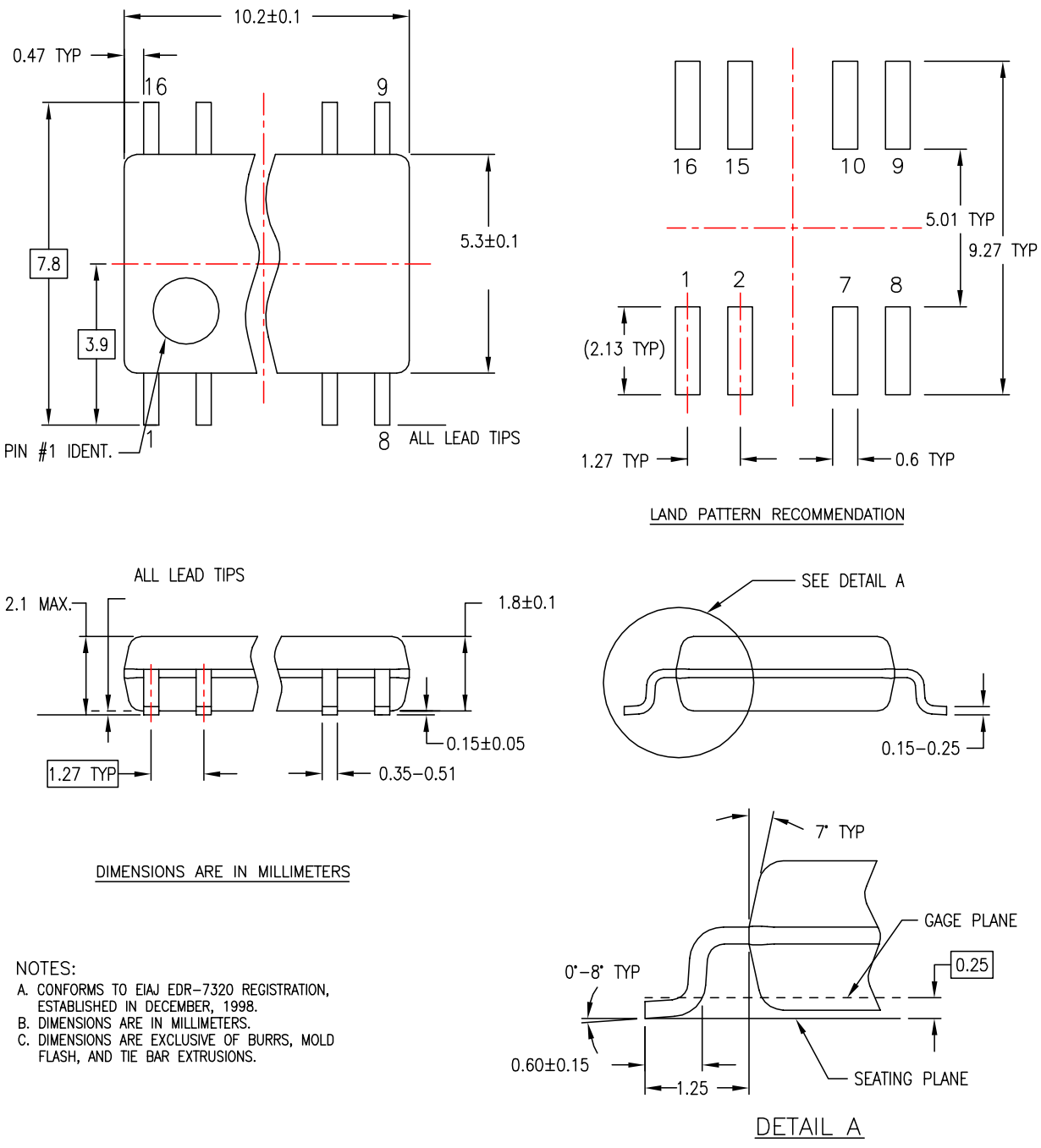


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

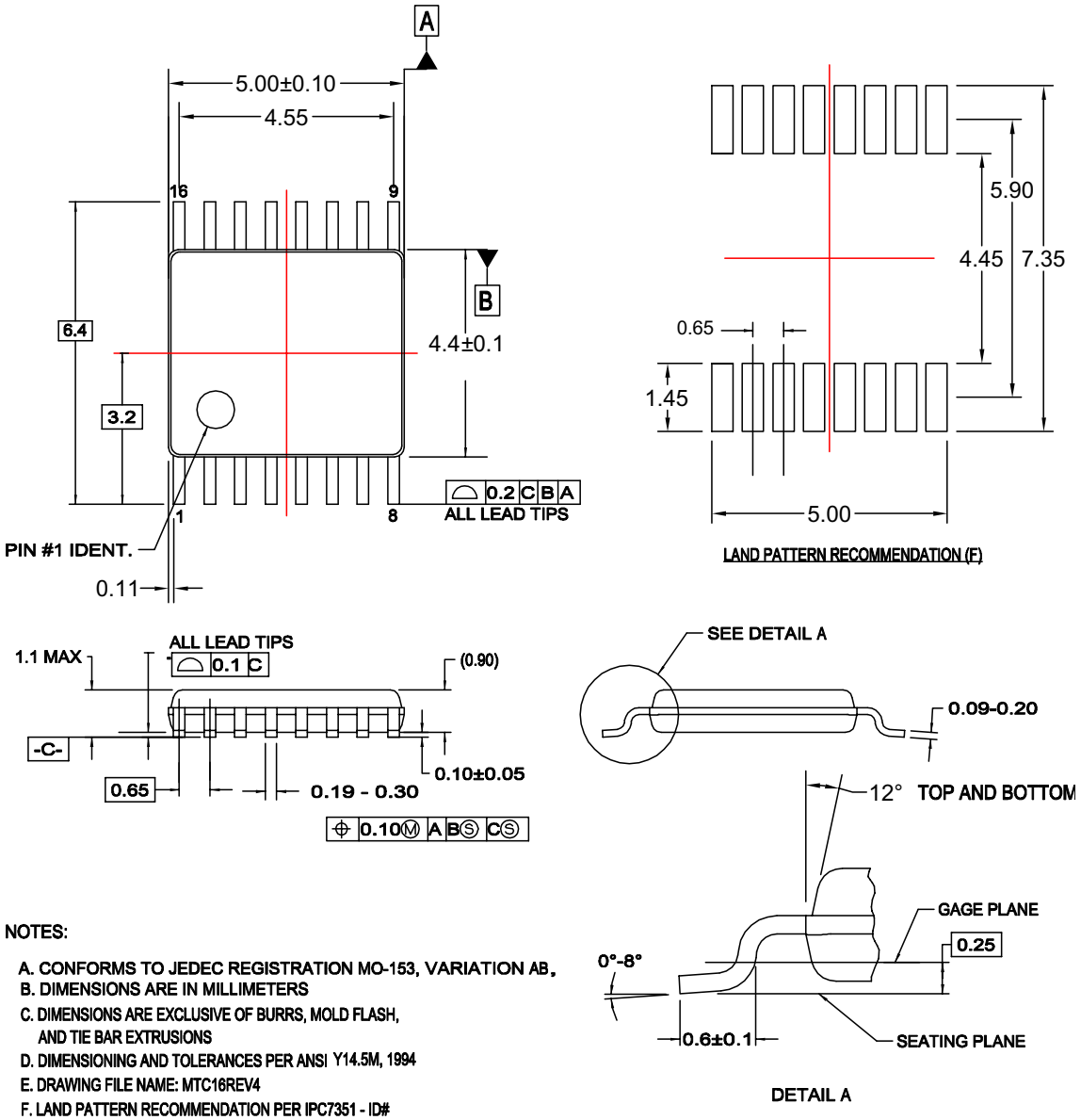
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB.
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

FAIRCHILD
SEMICONDUCTOR®

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Across the board. Around the world.™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
CTL™
Current Transfer Logic™
DOME™
E²CMOS™
EcoSPARK®
EnSigna™
FACT Quiet Series™
FACT®
FAST®
FASTr™
FPS™
FRFET®
GlobalOptoisolator™
GTO™
HiSeC™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
MICROCOUPLER™
MicroPak™
MICROWIRE™
Motion-SPM™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR®
PACMAN™
PDP-SPM™
POP™
Power220®
Power247®
PowerEdge™
PowerSaver™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
The Power Franchise®
™
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyWire™
TruTranslation™
µSerDes™
UHC®
UniFET™
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I26