

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

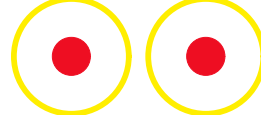
U_PWR2
PWR2.SchDoc

Serial
Serial
Serialnumber 6,3 x 6.3mm

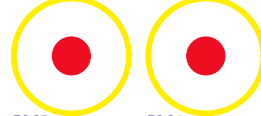
FIDU-DOT - small FIDU-DOT - small



PM1 PM2
FIDU-DOT - small FIDU-DOT - small

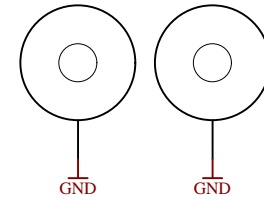


PM3 PM4
FIDU-DOT - small FIDU-DOT - small

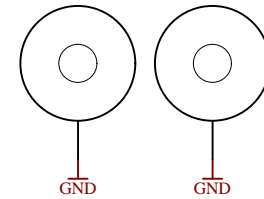


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




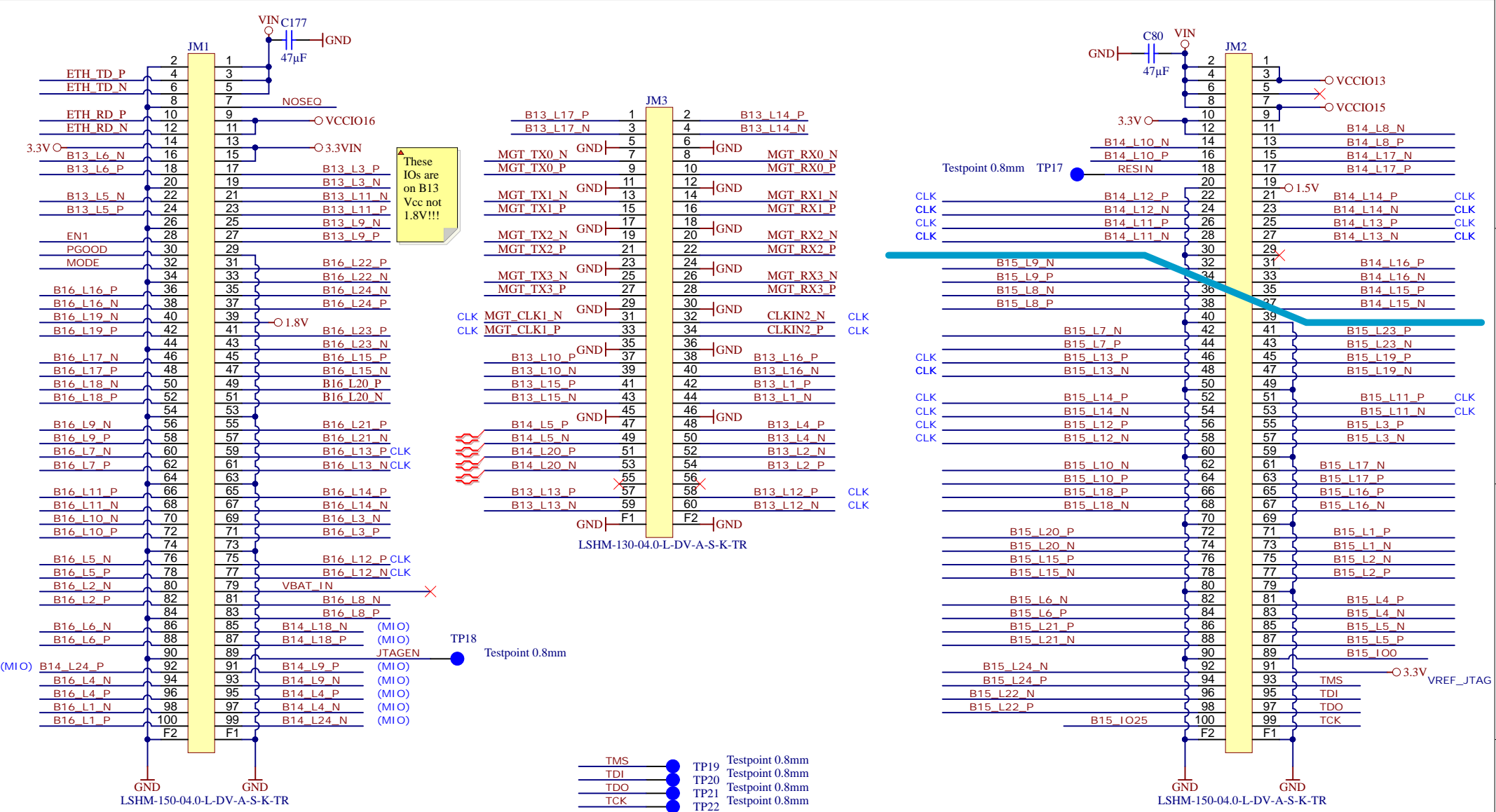
Mount.Hole 3.2mm Mount.Hole 3.2mm



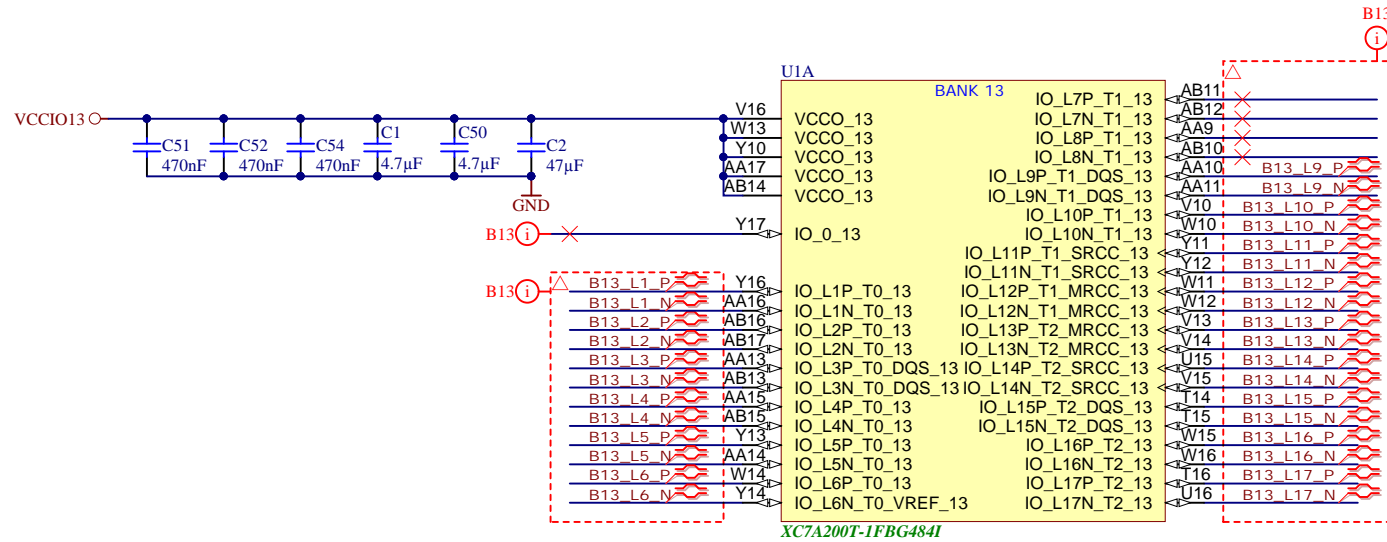
Top of Board



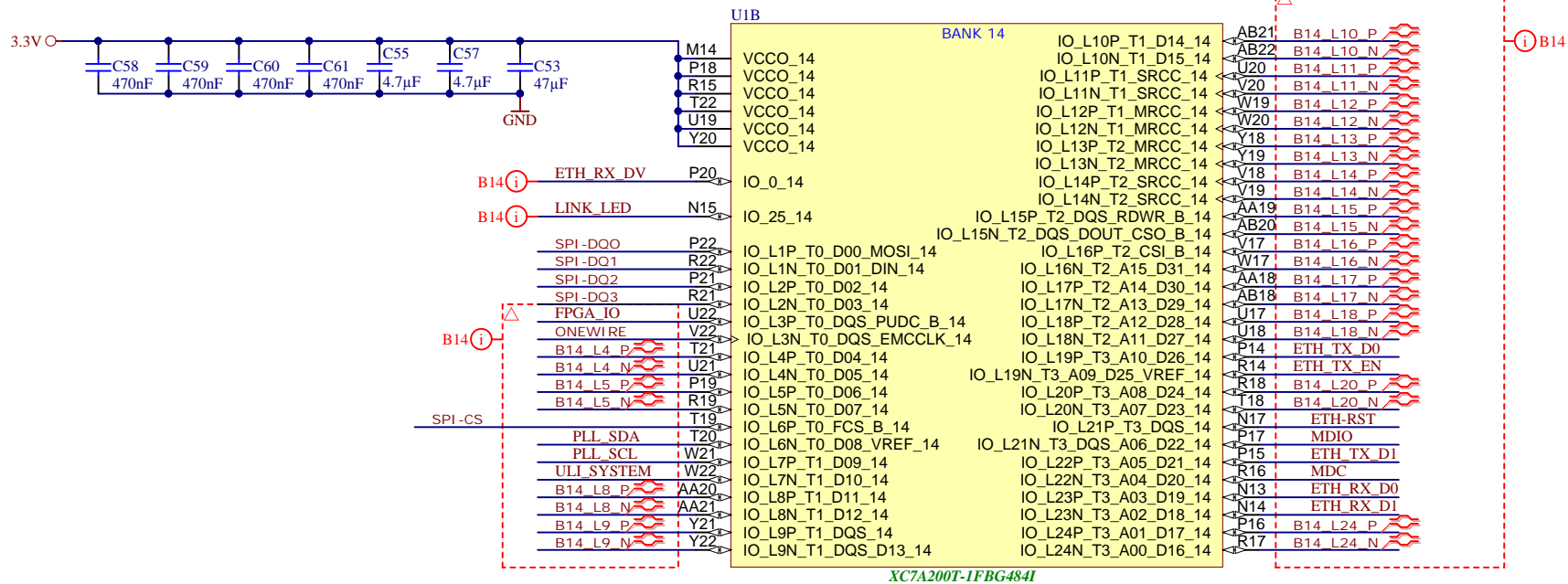
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		A4	Number: TE0712 200_11
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
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Filename: TE0712.SchDoc			



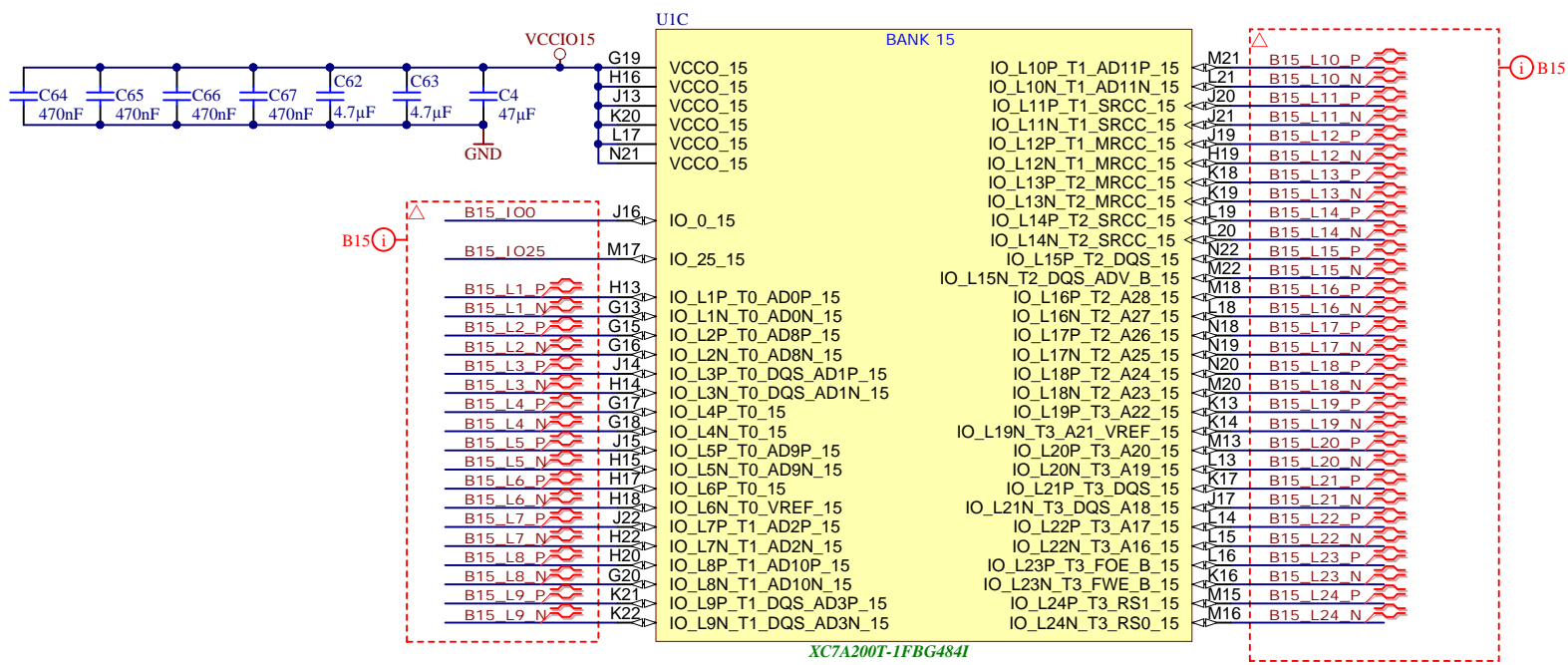
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A4	Number: TE0712 200_11	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page2 of 16
Filename: B2B-Connectors.SchDoc		



	Title: B13	
	A4	Number: TE0712 200_11
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Filename: B13.SchDoc		



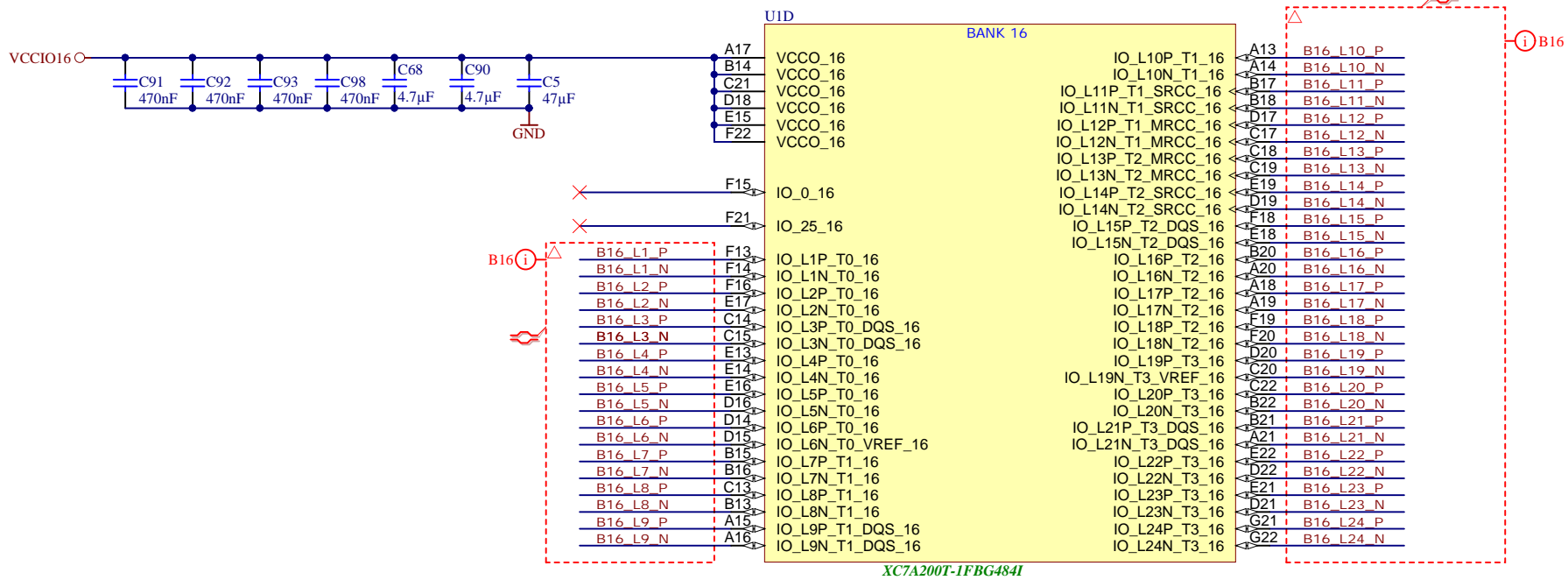
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Filename: B14.SchDoc		Page 4 of 16



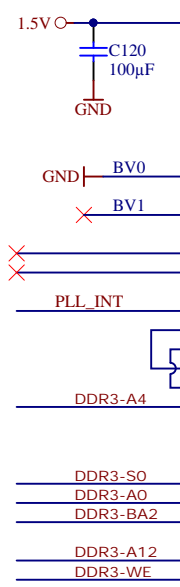
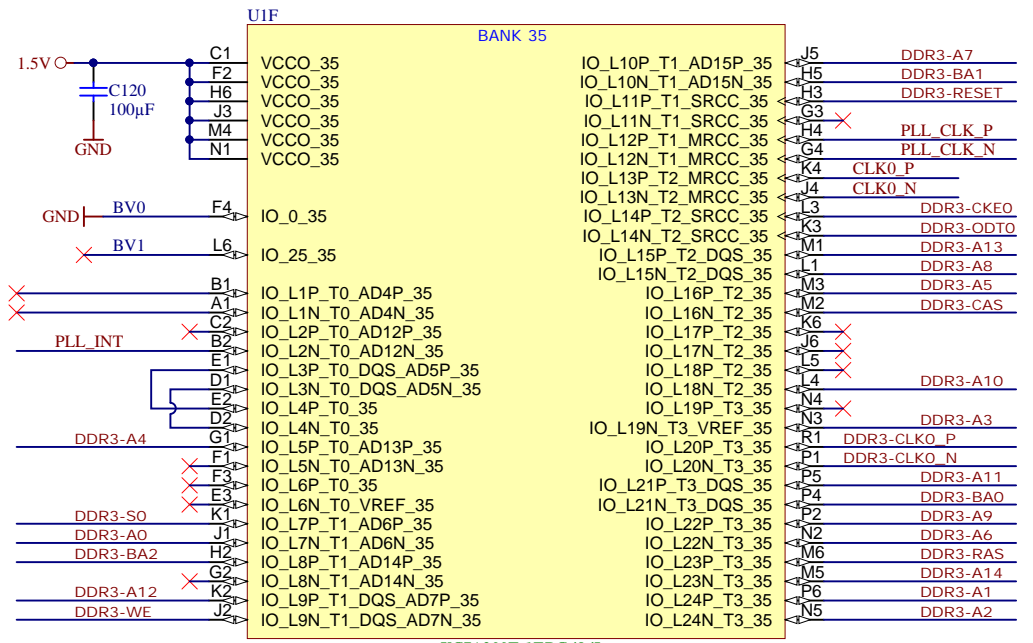
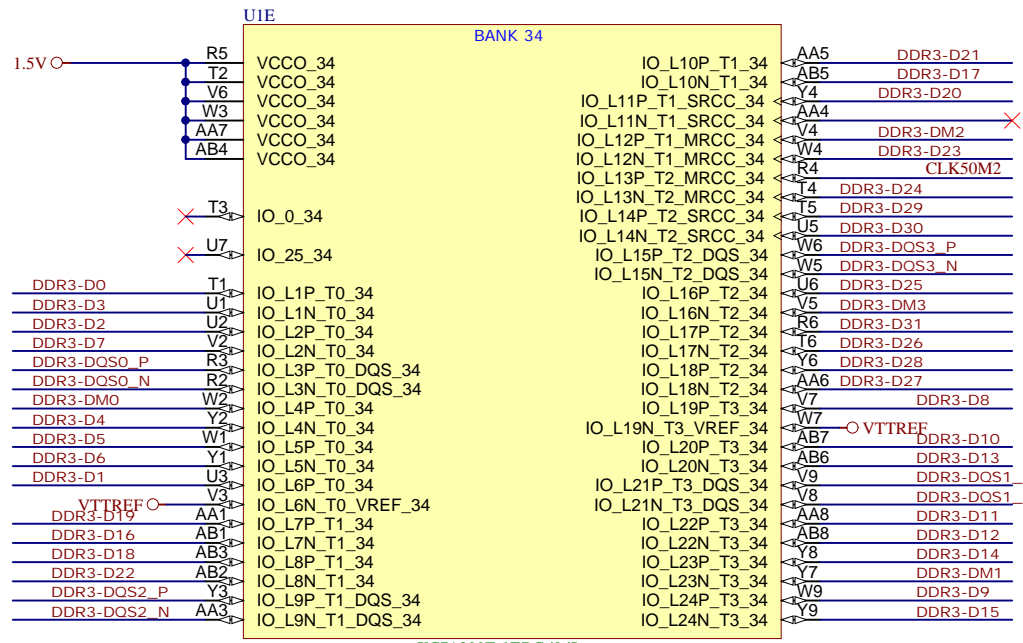
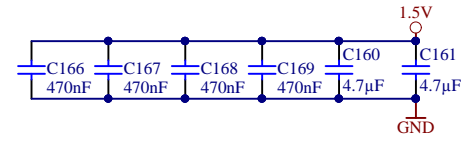
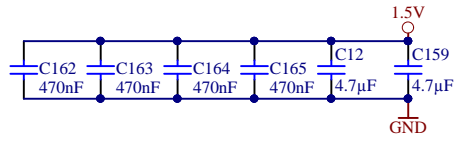
XC7A200T-1FBG484I



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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
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Filename: B15.SchDoc		

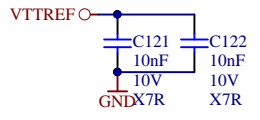
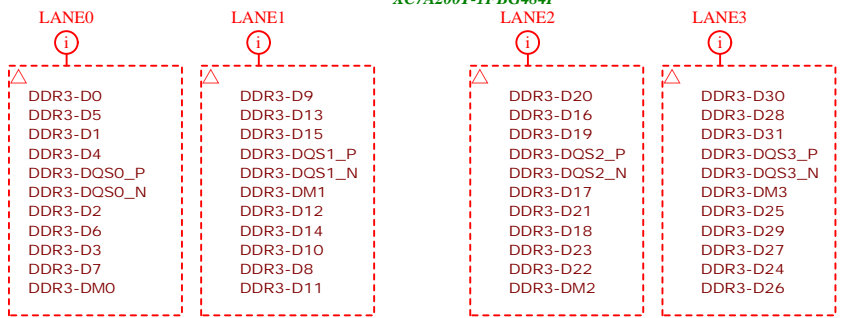


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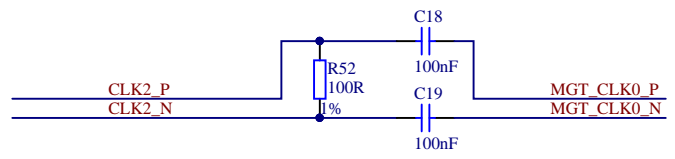
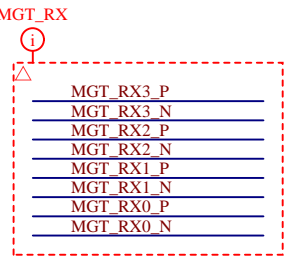
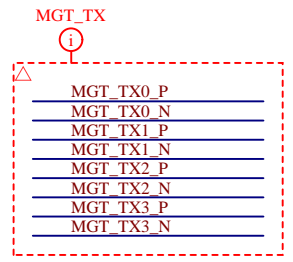
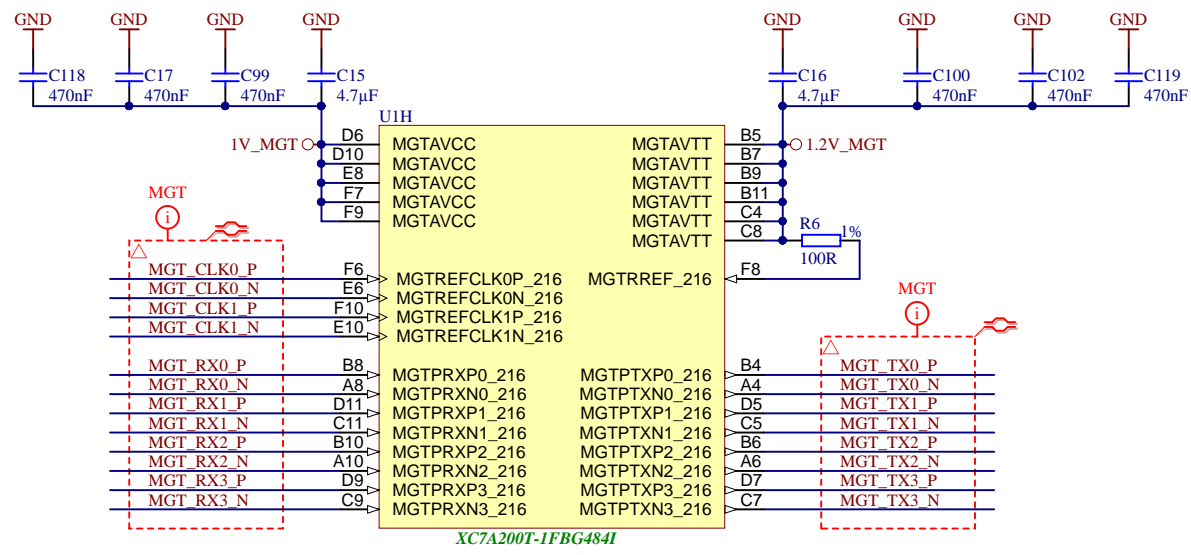


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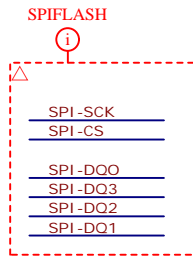
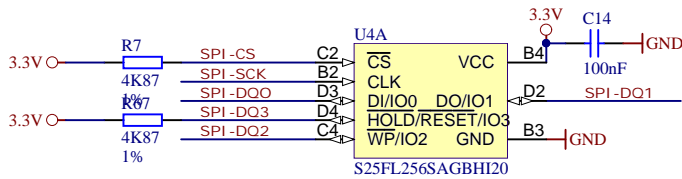
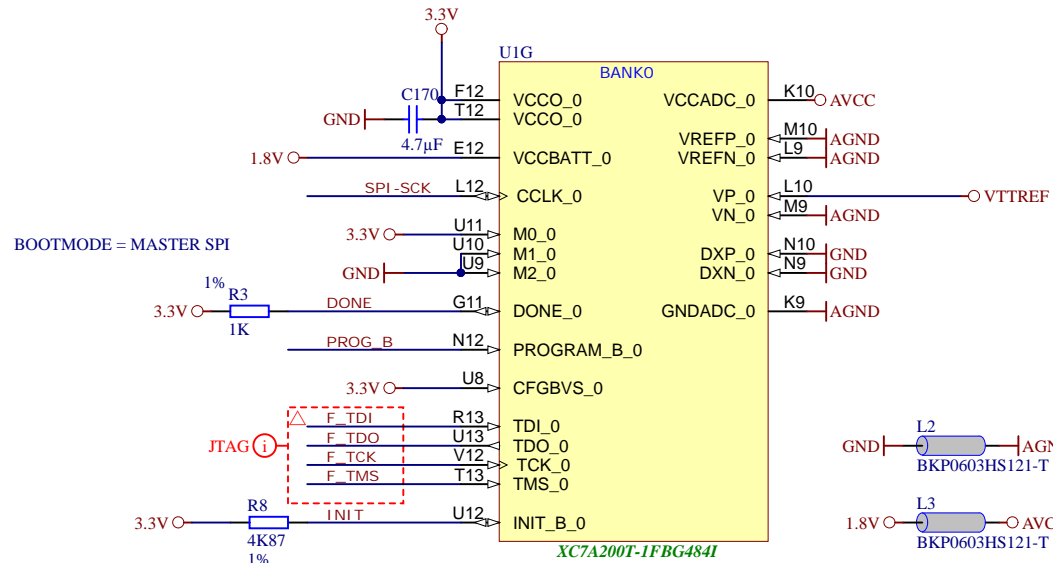
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	Title: MGT		
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Filename: FPGA-MGT.SchDoc			



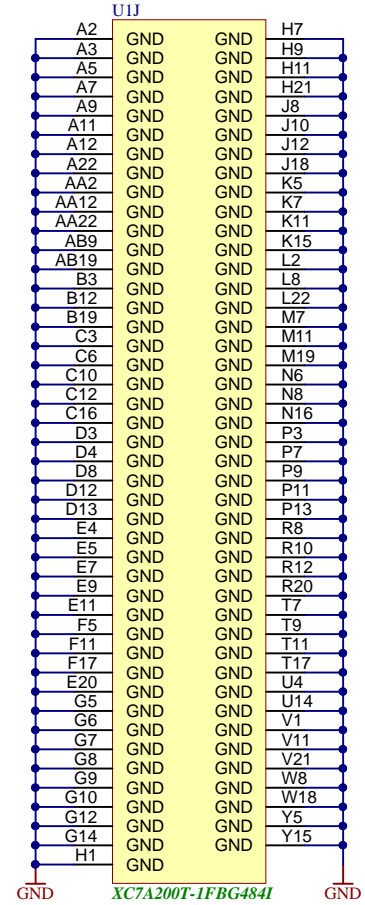
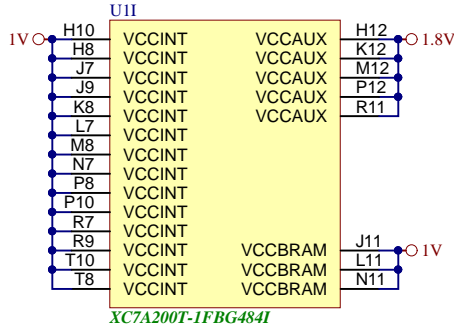
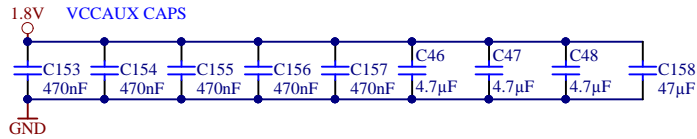
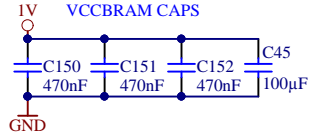
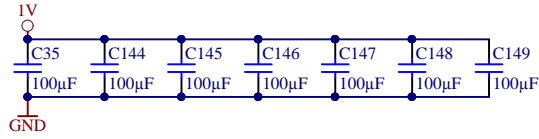
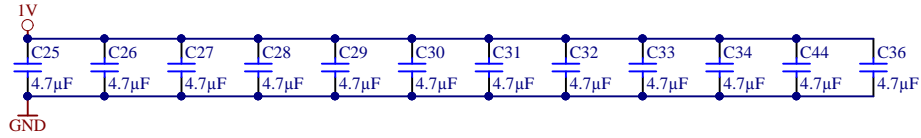
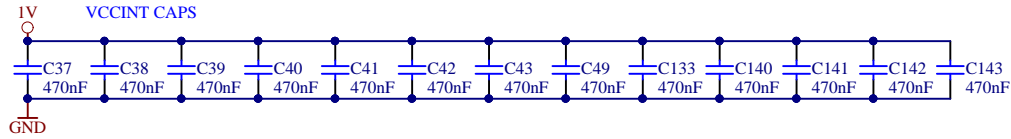

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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 9 of 16
Filename: FPGA-CFG.SchDoc		

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2

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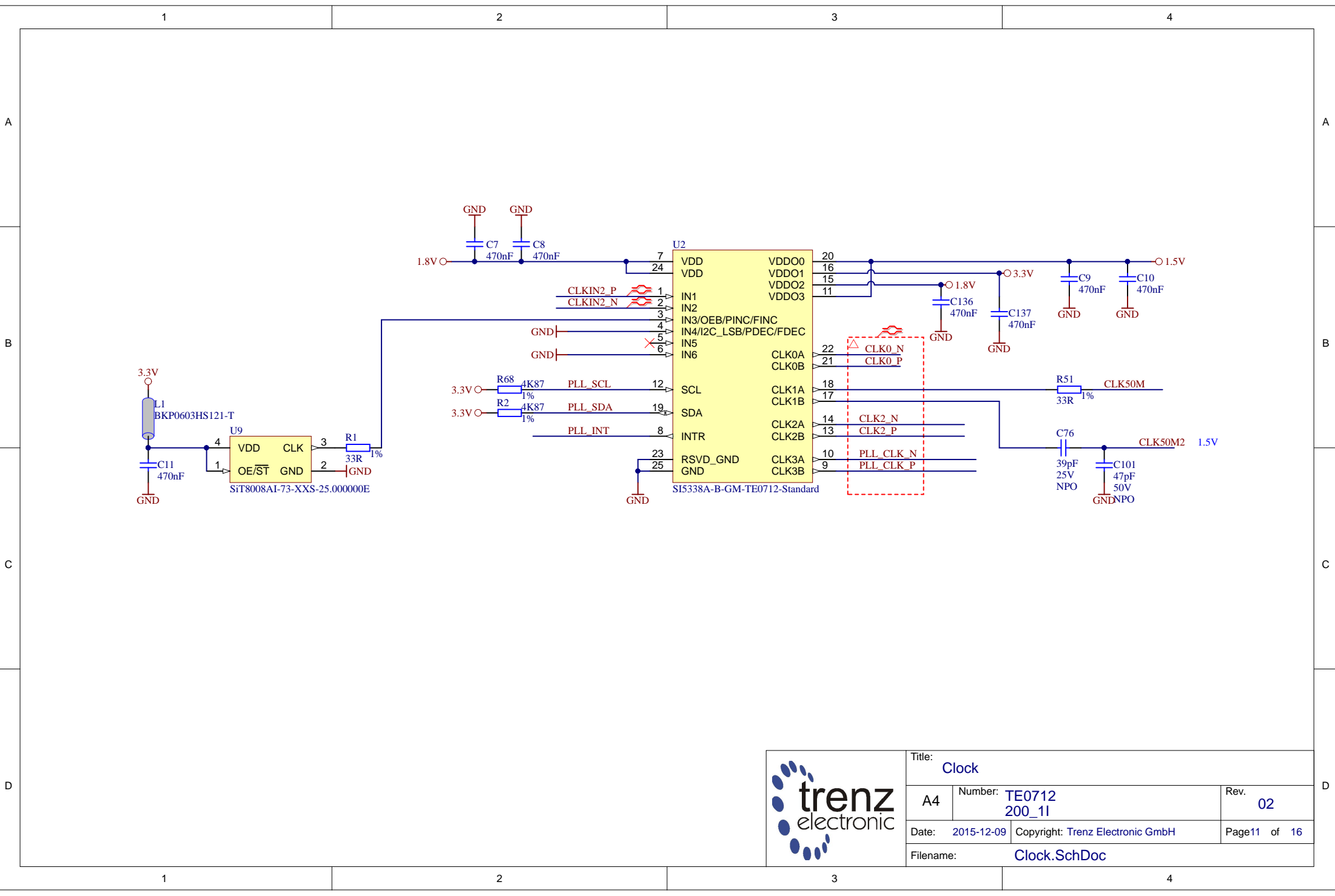
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 10 of 16
Filename: FPGA-PWR.SchDoc		


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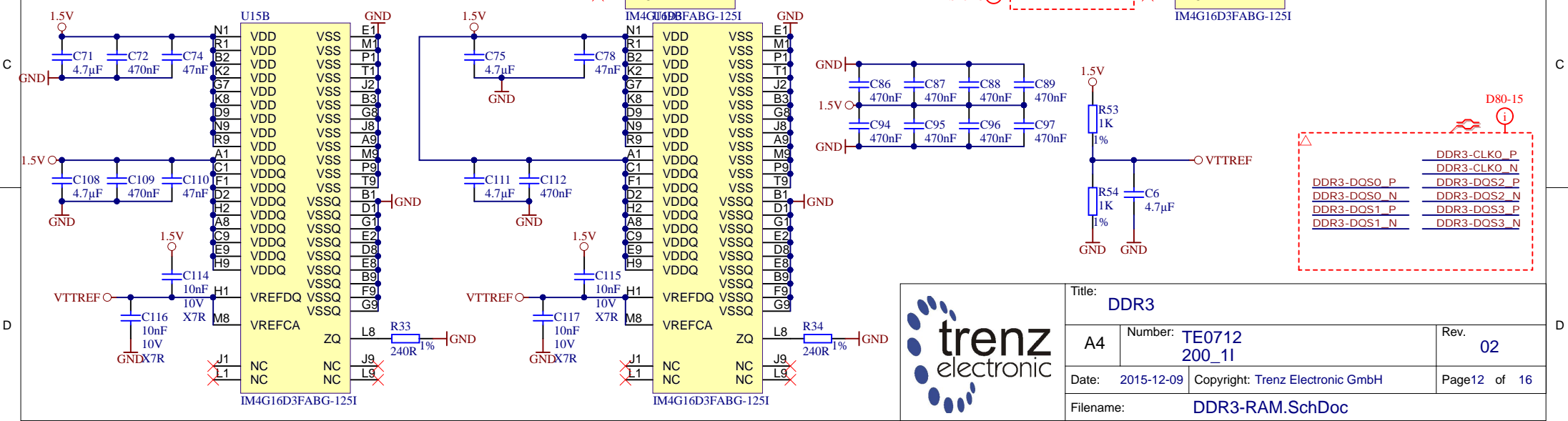
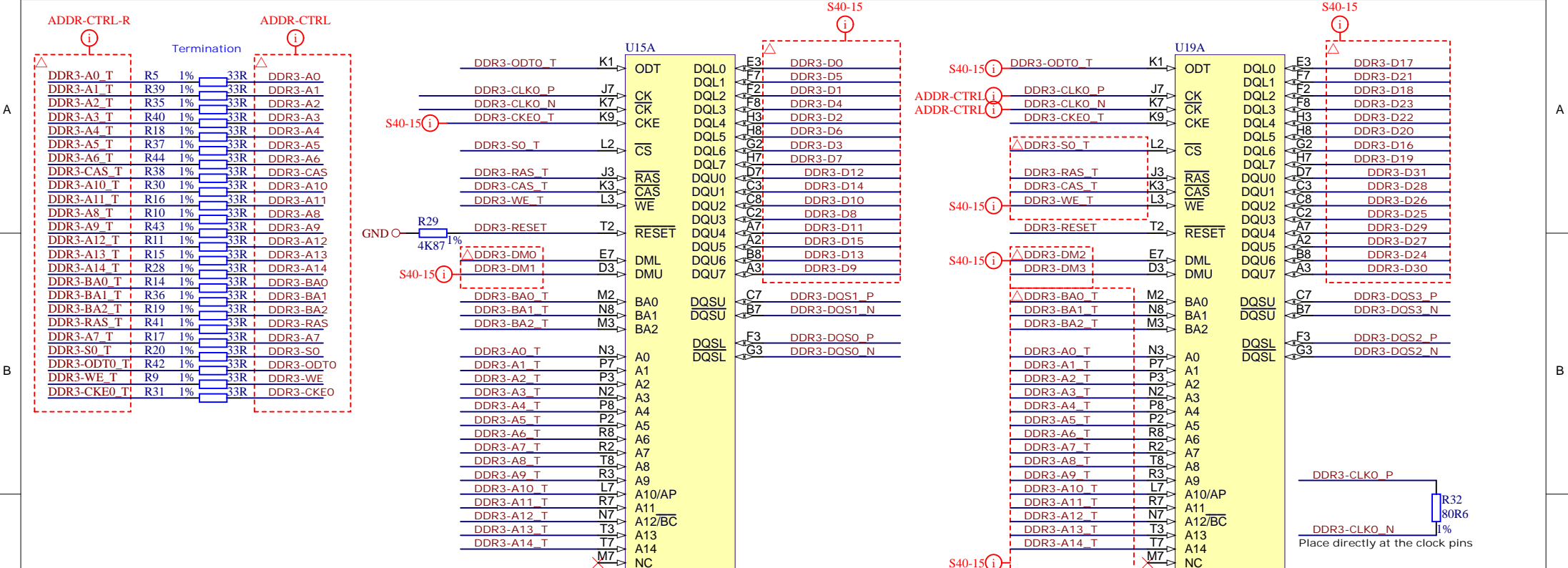
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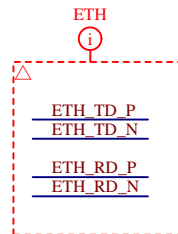
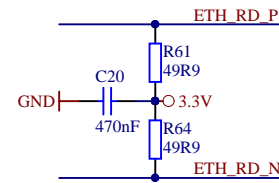
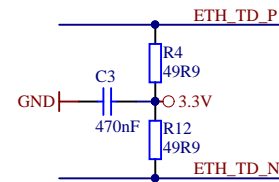
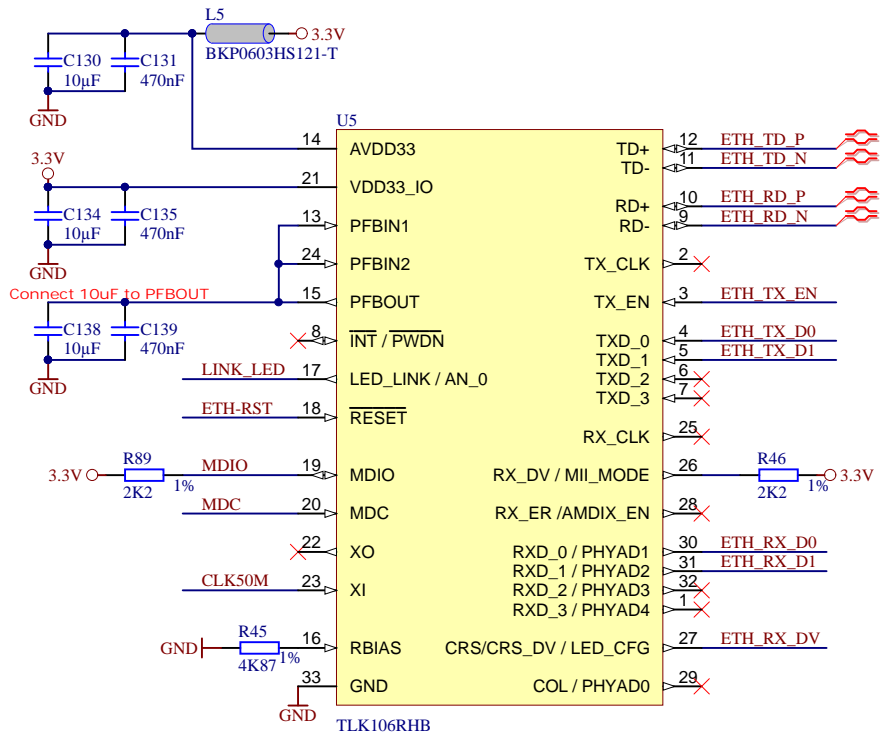
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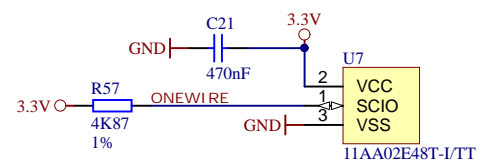
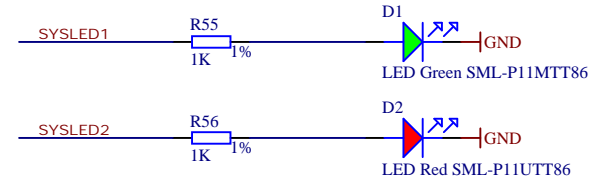
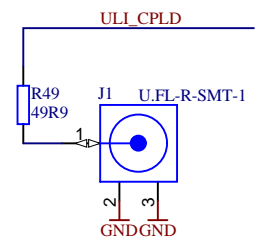
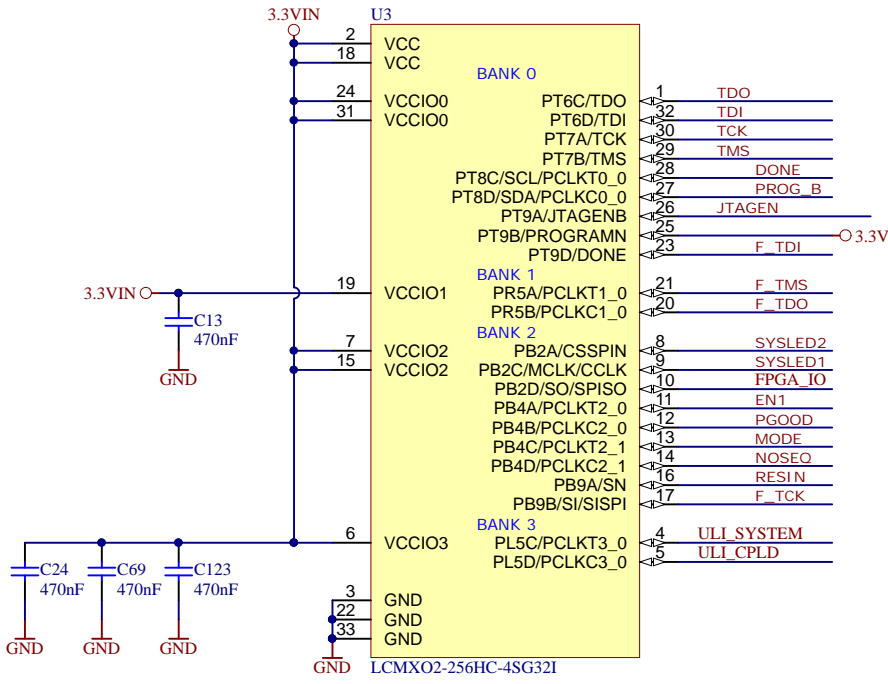
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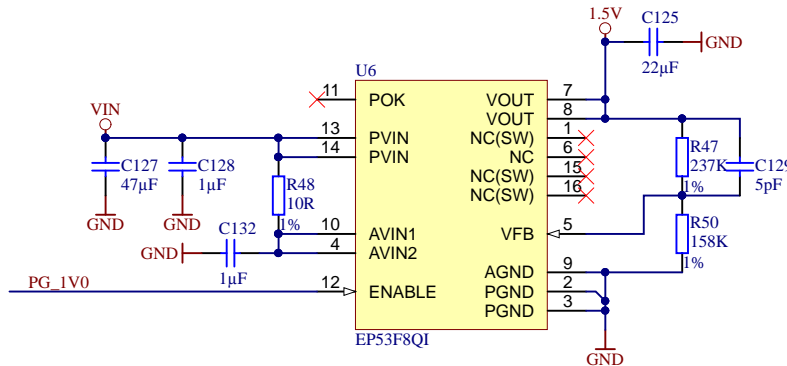
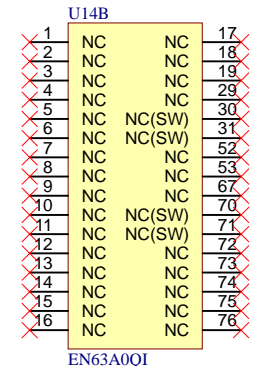
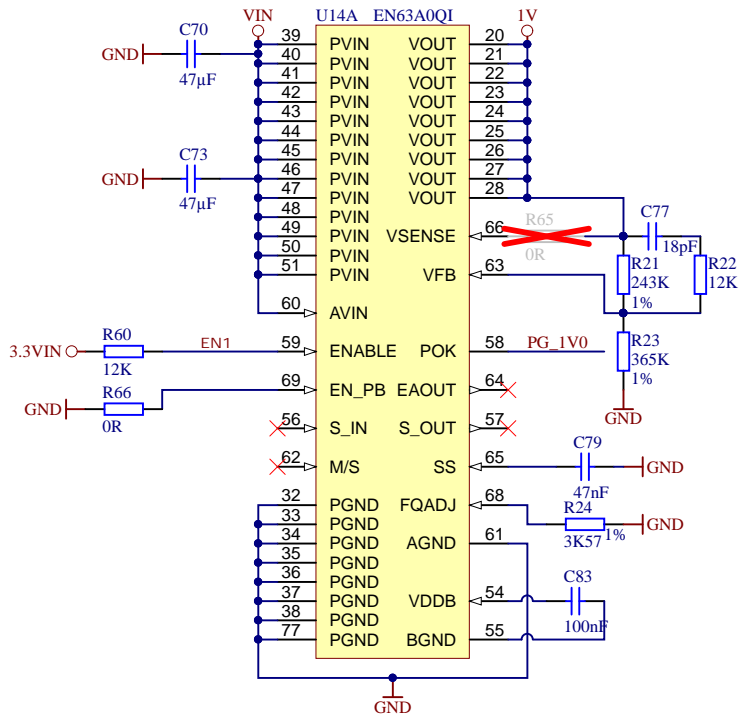
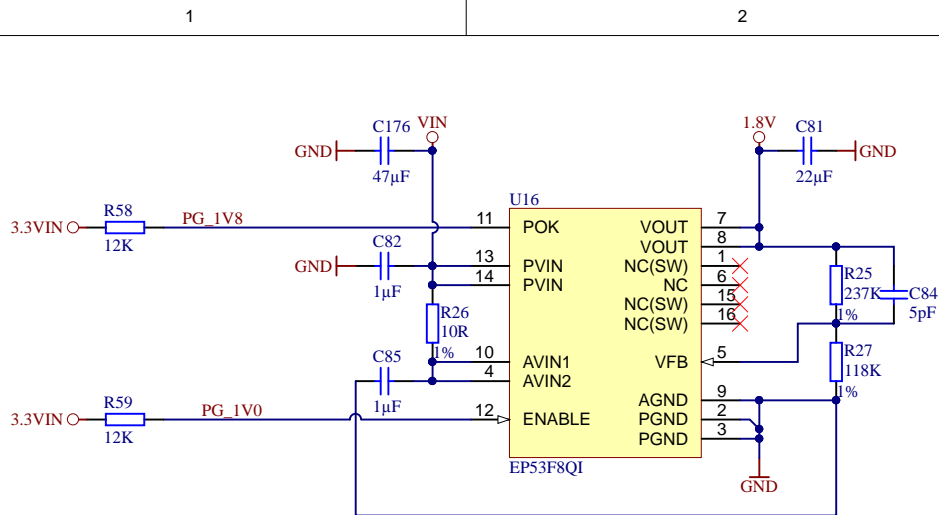
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 12 of 16
Filename: DDR3-RAM.SchDoc		



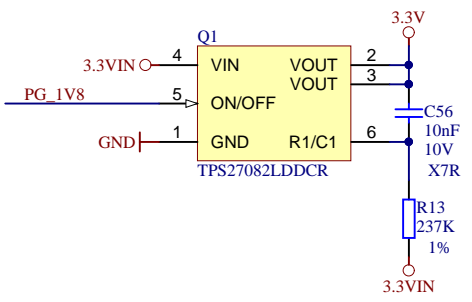
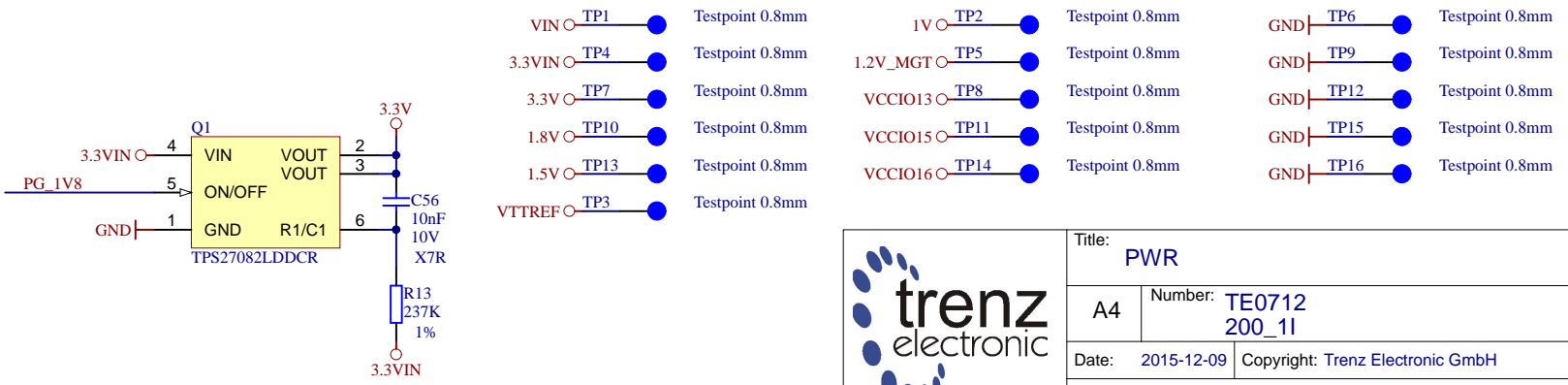
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	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
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Filename: ETHERNET.SchDoc			



Title: CPLD		
A4	Number: TE0712 200_11	Rev. 02
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R65	R66	MODE	EN63A0QI
OK	X		enable pre-bias start-up
X	OK		disable pre-bias start-up



Title: PWR		
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A

A

B

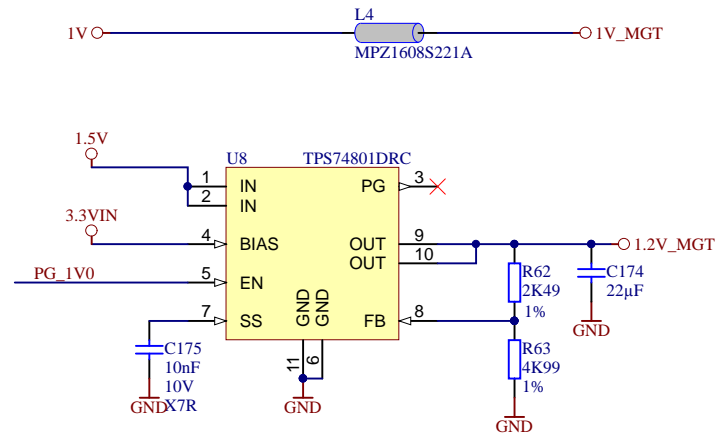
B


C

C

D

D



			Title: PWR	
			A4	Number: TE0712 200_11
Date: 2015-12-09		Copyright: Trenz Electronic GmbH		Page 16 of 16
Filename: PWR2.SchDoc				

1

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4