THCV226 4LANE Evaluation board

V-by-One HS receiver evaluation board

Parts Number: THEVA226-4LANE

1. Description

THEVA226-4LANE is designed to support video data transmission between the host and display. This board can receive 32bit video data and 3bit control data via four differential pairs of V-by-One HS lanes. This chip supports the video data transmission up to 1080p/10b/120Hz. The maximum serial data rate is 3.4Gbps/lane. The supply voltage range is "5V to 12V".

2. Connection Diagram

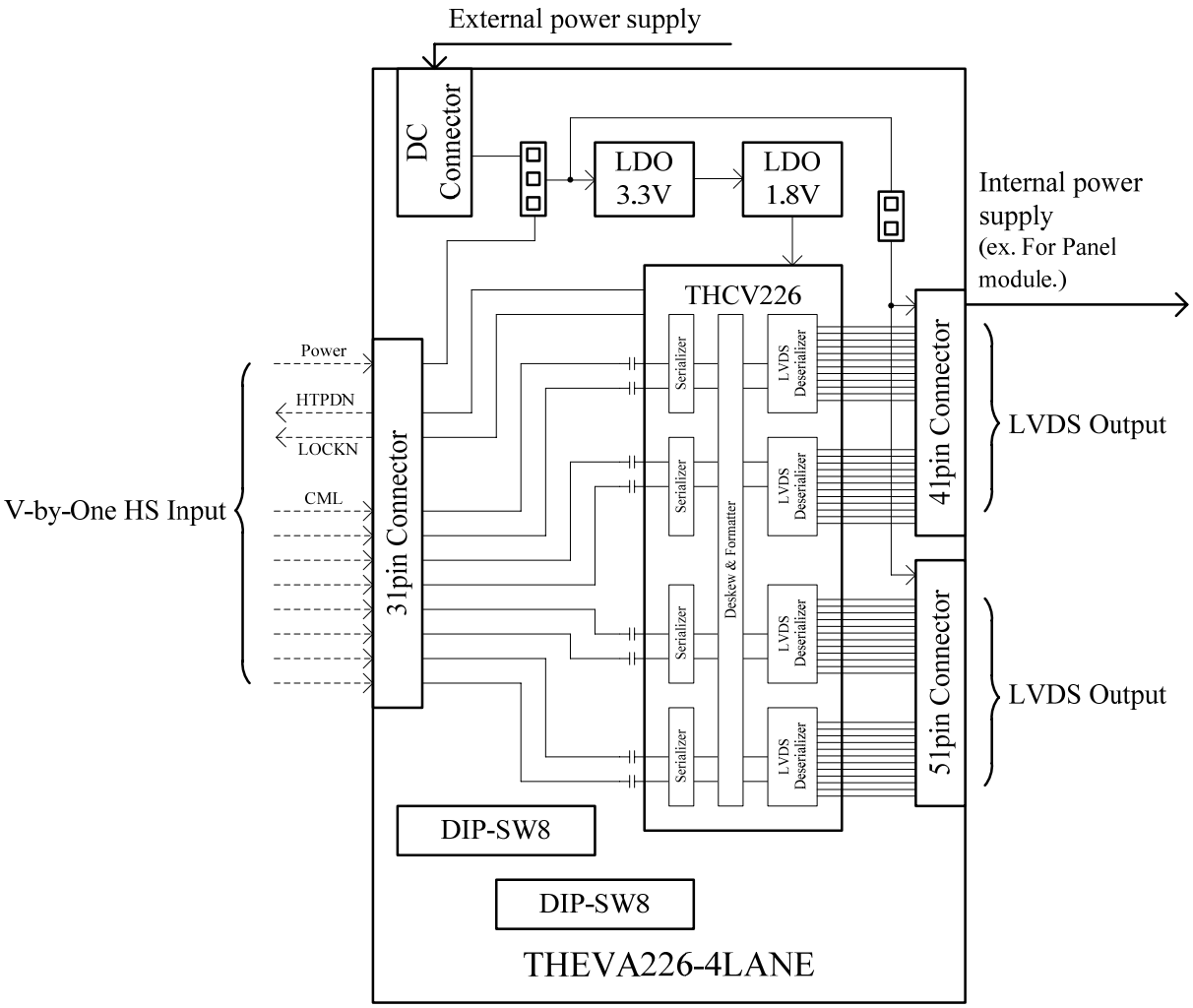


Figure2 Connection diagram

3. Example of Evaluation

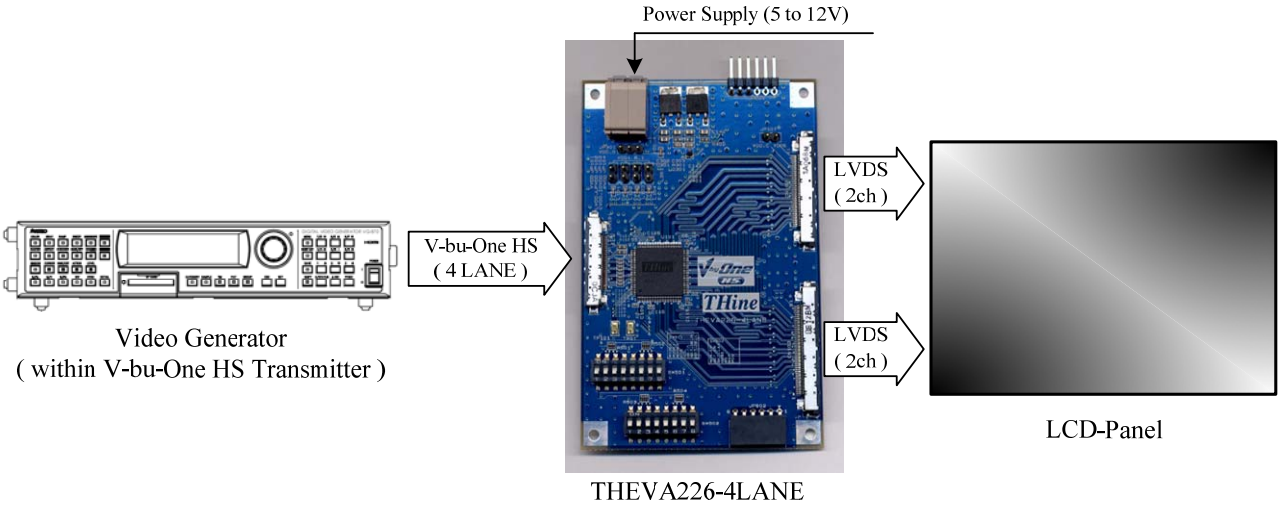


Figure3.1 Example of evaluation 1

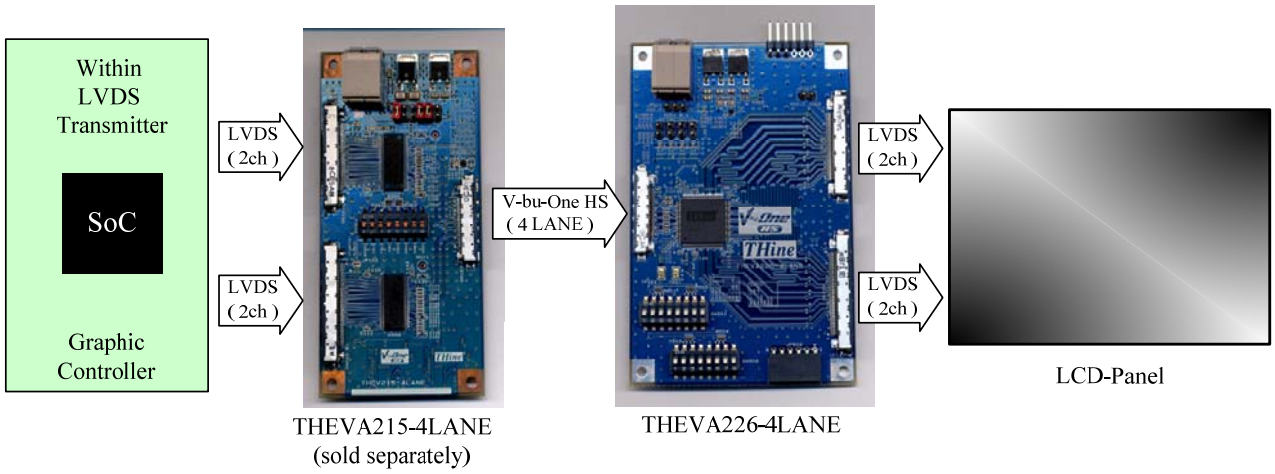


Figure3.2 Example of evaluation 2

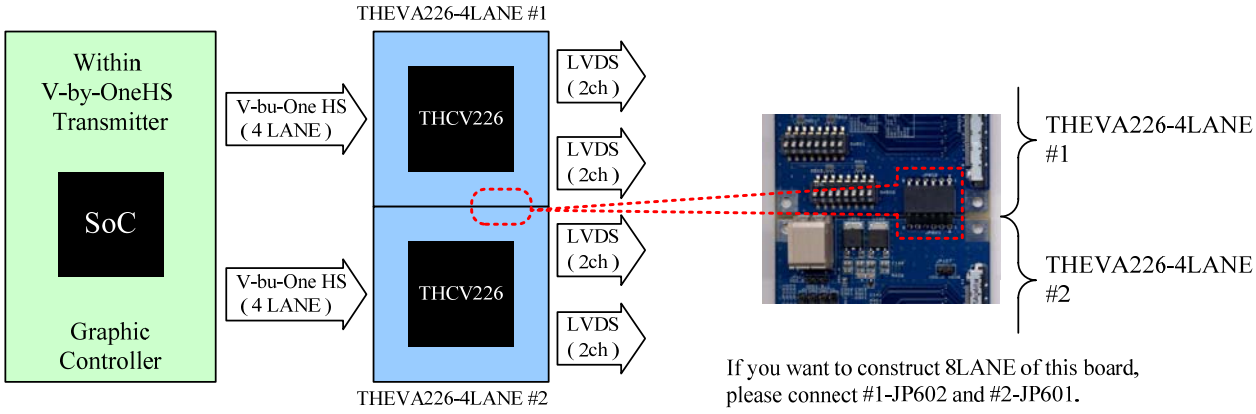


Figure3.3 Example of evaluation 3

4. Connectors

This chapter shows the connector.

Table4.1 CN101 Pin assignments

Pin No.	Symbol	Descriptions
1	Vcc	Supply voltage from Before Board to THEVA226-4LANE
2		
3		
4		
5		
6		
7		
8	GND	Ground
9		
10		
11		
12	HTPDN	Hot plug detect
13	LOCKN	Lock detect
14	GND	Ground
15	Rx0n	V-by-One® HS Channel 0 (CML)
16	Rx0p	
17	GND	Ground
18	GND	
19	Rx1n	V-by-One® HS Channel 1 (CML)
20	Rx1p	
21	GND	Ground
22	GND	
23	Rx2n	V-by-One® HS Channel 2 (CML)
24	Rx2p	
25	GND	Ground
26	GND	
27	Rx3n	V-by-One® HS Channel 3 (CML)
28	Rx3p	
29	GND	Ground
30	NC	Non Connected
31		

Table4.2 CN102 Pin assignments

Pin No.	Symbol	Descriptions
41	Vcc	Supply voltage from video processing unit, And for Panel module (Internal Supply)
40		
39		
38		
37		
36	NC	Non Connected
35	GND	Ground
34		
33		
32	RLA0-	LVDS data input/output
31	RLA0+	
30	RLB0-	
29	RLB0+	
28	RLC0-	
27	RLC0+	
26	GND	Ground
25	RLCLK0-	LVDS clock input/output
24	RLCLK0+	
23	GND	Ground
22	RLD0-	LVDS data input/output
21	RLD0+	
20	RLE0-	
19	RLE0+	
18	GND	Ground
17	RLA1-	LVDS data input/output
16	RLA1+	
15	RLB1-	
14	RLB1+	
13	RLC1-	
12	RLC1+	
11	GND	Ground
10	RLCLK1-	LVDS clock input/output
9	RLCLK1+	
8	GND	Ground
7	RLD1-	LVDS data input/output
6	RLD1+	
5	RLE1-	
4	RLE1+	
3	GND	Ground
2	NC	Non Connected
1		

Table4.3 CN103 Pin assignments

Pin No.	Symbol	Descriptions
51	Vcc	Supply voltage from video processing unit, And for Panel module (Internal Supply)
50		
49		
48		
47		
46	NC	Non Connected
45	GND	Ground
44		
43		
42	RLA2-	LVDS data input/output
41	RLA2+	
40	RLB2-	
39	RLB2+	
38	RLC2-	
37	RLC2+	
36	GND	Ground
35	RLCLK2-	LVDS clock input/output
34	RLCLK2+	
33	GND	Ground
32	RLD2-	LVDS data input/output
31	RLD2+	
30	RLE2-	
29	RLE2+	
28	GND	Ground
27	RLA3-	LVDS data input/output
26	RLA3+	
25	RLB3-	
24	RLB3+	
23	RLC3-	
22	RLC3+	
21	GND	Ground
20	RLCLK3-	LVDS clock input/output
19	RLCLK3+	
18	GND	Ground
17	RLD3-	LVDS data input/output
16	RLD3+	
15	RLE3-	
14	RLE3+	
13	GND	Ground
12	NC	Non Connected
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		

5. Power supplies and Transfer mode set up

This chapter shows the power supply and transfer mode setting with the jumper.

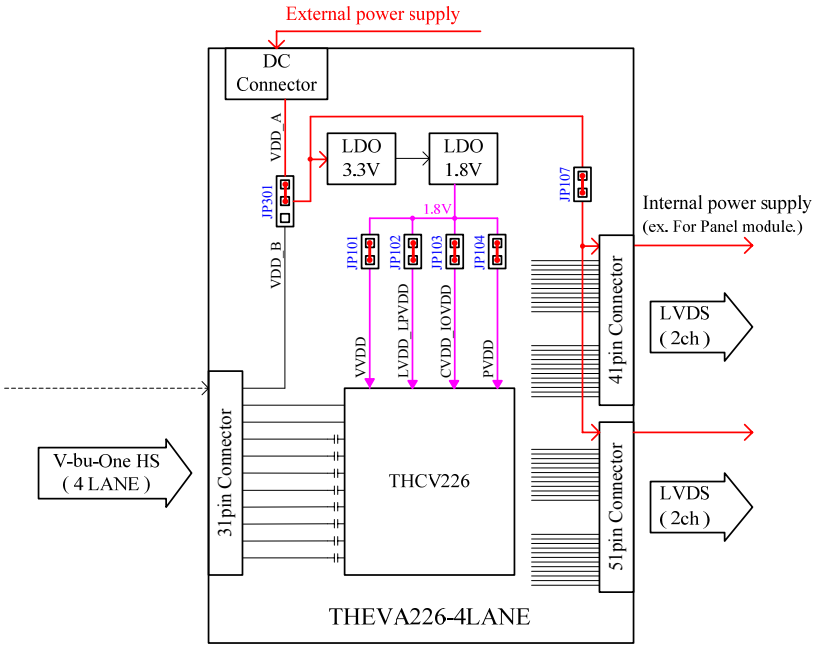


Figure5.1 From external power supply to after board

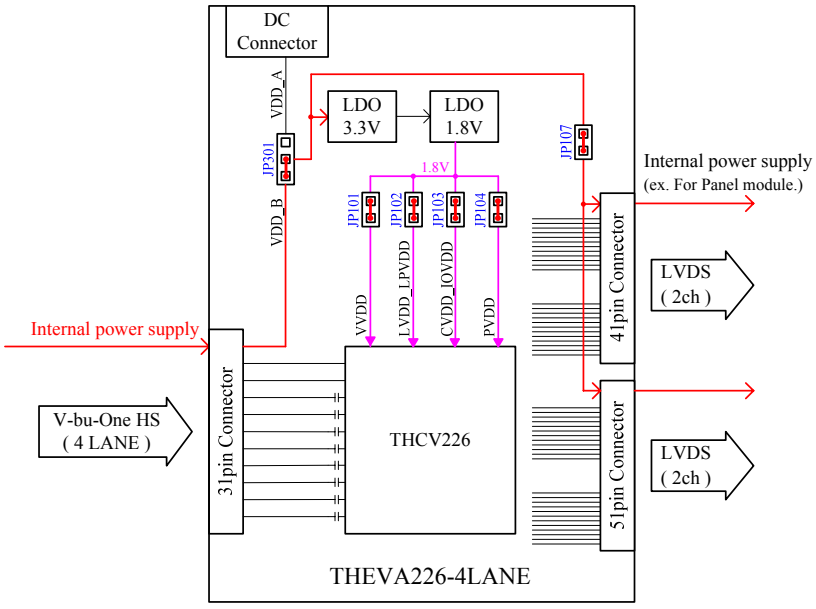


Figure5.2 From internal power supply to after board

6. Other functional descriptions

This chapter shows other function.

6.1 LED on THEA226-4LANE
D301: Power ON indicator.
D401: LOCKN indicator.

7. DIP-SW setting

This chapter shows the DIP switches of control settings.

Table7.1 SW501 Setting

<table>
<tr><th>SW#</th><th>Symbol</th><th>Default Setting</th><th>Function</th></tr>
<tr><td>1</td><td>MODE2</td><td>Low</td><td rowspan="3">Input / Output mode select
<table>
<tr><th>MODE2</th><th>MODE1</th><th>MODE0</th><th>COL</th><th>V-by-One HS</th><th>LVDS</th><th>Operation Mode</th></tr>
<tr><td rowspan="2">High</td><td rowspan="2">High</td><td rowspan="2">High</td><td>High</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td><td rowspan="2">HSLVDS / Distribution mode2</td></tr>
<tr><td>Low</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td></tr>
<tr><td rowspan="2">High</td><td rowspan="2">High</td><td rowspan="2">Low</td><td>High</td><td>40 – 85MHz</td><td>40 – 85MHz</td><td rowspan="2">Normal LVDS / Distribution mode2</td></tr>
<tr><td>Low</td><td>40 – 90MHz</td><td>40 – 90MHz</td></tr>
<tr><td rowspan="2">High</td><td rowspan="2">Low</td><td rowspan="2">High</td><td>High</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td><td rowspan="2">HSLVDS / Distribution mode1</td></tr>
<tr><td>Low</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td></tr>
<tr><td rowspan="2">High</td><td rowspan="2">Low</td><td rowspan="2">Low</td><td>High</td><td>40 – 85MHz</td><td>40 – 85MHz</td><td rowspan="2">Normal LVDS / Distribution mode1</td></tr>
<tr><td>Low</td><td>40 – 90MHz</td><td>40 – 90MHz</td></tr>
<tr><td rowspan="2">Low</td><td rowspan="2">High</td><td rowspan="2">High</td><td>High</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td><td rowspan="2">HSLVDS / Crossing Mode</td></tr>
<tr><td>Low</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td></tr>
<tr><td rowspan="2">Low</td><td rowspan="2">High</td><td rowspan="2">Low</td><td>High</td><td>40 – 85MHz</td><td>40 – 85MHz</td><td rowspan="2">Normal LVDS / Crossing mode</td></tr>
<tr><td>Low</td><td>40 – 90MHz</td><td>40 – 90MHz</td></tr>
<tr><td rowspan="2">Low</td><td rowspan="2">Low</td><td rowspan="2">High</td><td>High</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td><td rowspan="2">HSLVDS mode</td></tr>
<tr><td>Low</td><td>40 – 78.5MHz</td><td>80 – 157MHz</td></tr>
<tr><td rowspan="2">Low</td><td rowspan="2">Low</td><td rowspan="2">Low</td><td>High</td><td>40 – 85MHz</td><td>40 – 85MHz</td><td rowspan="2">Normal LVDS mode</td></tr>
<tr><td>Low</td><td>40 – 90MHz</td><td>40 – 90MHz</td></tr>
</table></td></tr>
<tr><td>4</td><td>OPF</td><td>Low</td><td>Output Pattern at CDR Fail Condition (LOCKN=1)
High: LVDS output Low data
Low: LVDS output Hi-Z data</td></tr>
<tr><td>5</td><td>COL</td><td>High</td><td>Color depth select
High: 10 bit mode
Low: 8 bit mode</td></tr>
<tr><td>6</td><td>OE</td><td>High</td><td>LVDS Output Enable
High: Normal Operation
Low: Output Disable</td></tr>
<tr><td>7</td><td>BET_SEL0</td><td>Low</td><td rowspan="2">Monitoring pin select</td></tr>
<tr><td>8</td><td>BET_SEL1</td><td>Low</td></tr>
</table>

* Please see the datasheet for details. (THCV226_Rev.x.xx_E.pdf)

Table7.2 SW502 Setting

SW#	Symbol	Default Setting	Function
1	MON_EN	Low	Monitoring mode enable High: Monitoring enable Low: Monitoring disable
2	BET_EN	Low	Field-BET enable High: Enable Low: Normal operation
3	BET_LAT	Low	Latch select input under Field BET operation High: Latched result output Low: Reset latched result
4	PRBS	Low	Must be tied to GND
5	RS	High	LVDS swing level select High: Normal swing (350mV) Low: Reduced swing (200mV)
6	MAP	High	LVDS output format select High: JEIDA format Low: VESA format
7	PDN1	High	Power down High: Normal operation Low: Power down operation
8	NC	Low	Must be tied to GND

* Please see the datasheet for details. (THCV226_Rev.x.xx_E.pdf)

8. Schematic

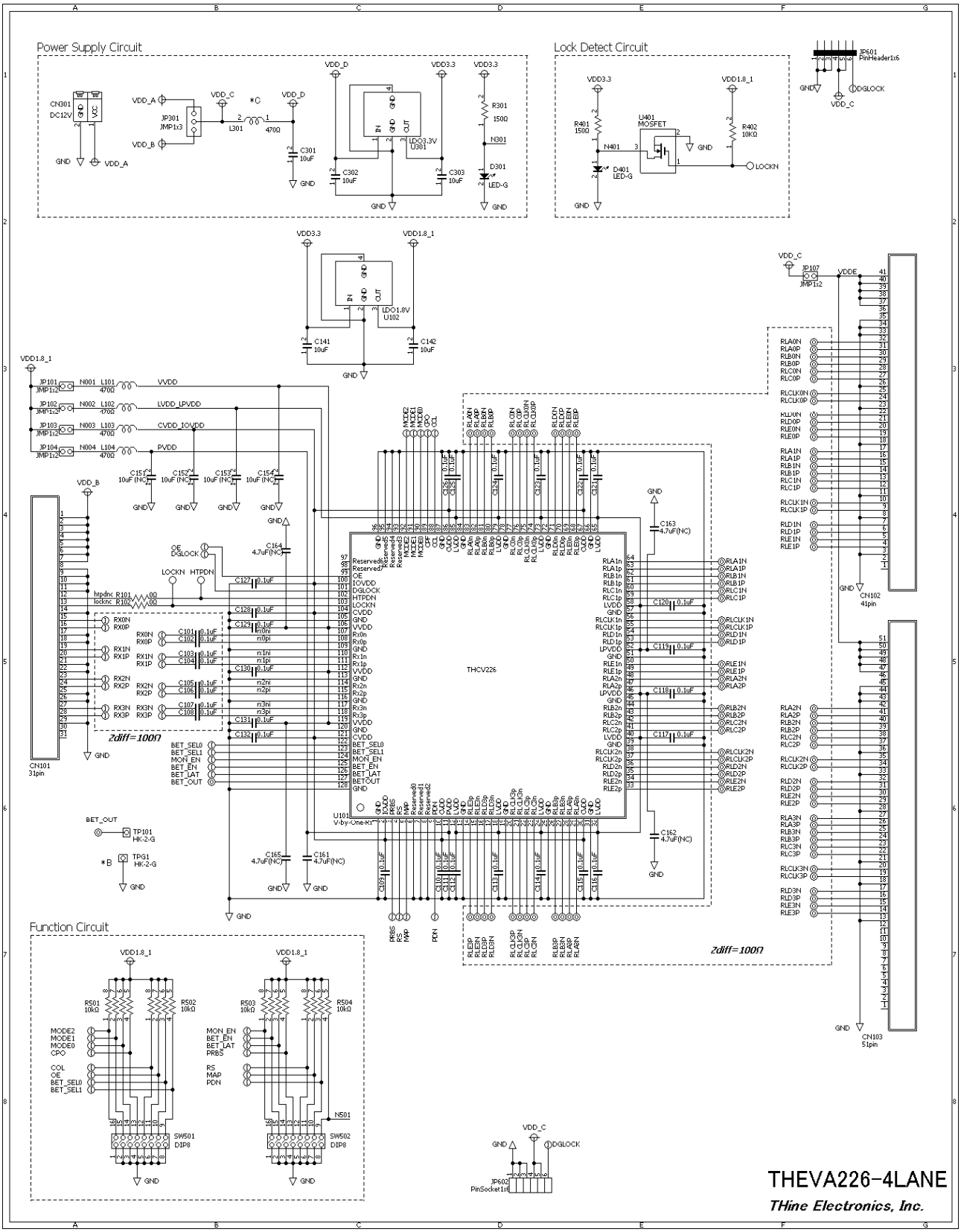


Figure8 Board schematic

9. Bills of Materials

Table9 Bills of Materials (BOM)

Designnator	Description	Size	PartNumber	Manufacter	Designnator	Description	Size	PartNumber	Manufacter
C101	0.1uF	1005	GRM155B31C104KA87	Murata	D301	LED-G	1608	SML-310MT	ROHM
C102	0.1uF	1005	GRM155B31C104KA87	Murata	D401	LED-G	1608	SML-310MT	ROHM
C103	0.1uF	1005	GRM155B31C104KA87	Murata	JP101	JMP1x2	2.54mm	1*2-PinHeaders	-
C104	0.1uF	1005	GRM155B31C104KA87	Murata	JP102	JMP1x2	2.54mm	1*2-PinHeaders	-
C105	0.1uF	1005	GRM155B31C104KA87	Murata	JP103	JMP1x2	2.54mm	1*2-PinHeaders	-
C106	0.1uF	1005	GRM155B31C104KA87	Murata	JP104	JMP1x2	2.54mm	1*2-PinHeaders	-
C107	0.1uF	1005	GRM155B31C104KA87	Murata	JP107	JMP1x2	2.54mm	1*2-PinHeaders	-
C108	0.1uF	1005	GRM155B31C104KA87	Murata	JP301	JMP1x3	2.54mm	1*3-PinHeaders	-
C109	0.1uF	1005	GRM155B31C104KA87	Murata	JP601	PinHeader1x6	2.54mm	C-05336	Akizuki
C110	0.1uF	1005	GRM155B31C104KA87	Murata	JP602	PinSocket1x6	2.54mm	C-03795	Akizuki
C111	0.1uF	1005	GRM155B31C104KA87	Murata	L101	470Ω	1608	MPZ1608B471ATA00	TDK
C112	0.1uF	1005	GRM155B31C104KA87	Murata	L102	470Ω	1608	MPZ1608B471ATA00	TDK
C113	0.1uF	1005	GRM155B31C104KA87	Murata	L103	470Ω	1608	MPZ1608B471ATA00	TDK
C114	0.1uF	1005	GRM155B31C104KA87	Murata	L104	470Ω	1608	MPZ1608B471ATA00	TDK
C115	0.1uF	1005	GRM155B31C104KA87	Murata	L301	470Ω	1608	MPZ1608B471ATA00	TDK
C116	0.1uF	1005	GRM155B31C104KA87	Murata	R101	0Ω	1608	RK73Z1JTBK	KOA
C117	0.1uF	1005	GRM155B31C104KA87	Murata	R102	0Ω	1608	RK73Z1JTBK	KOA
C118	0.1uF	1005	GRM155B31C104KA87	Murata	R301	150Ω	1608	RK73B1JBK151J	KOA
C119	0.1uF	1005	GRM155B31C104KA87	Murata	R401	150Ω	1608	RK73B1JBK151J	KOA
C120	0.1uF	1005	GRM155B31C104KA87	Murata	R402	10KΩ	1608	RK73B1JBK103J	KOA
C121	0.1uF	1005	GRM155B31C104KA87	Murata	R501	10kΩ	2010	EXB-28V103JX	KOA
C122	0.1uF	1005	GRM155B31C104KA87	Murata	R502	10kΩ	2010	EXB-28V103JX	KOA
C123	0.1uF	1005	GRM155B31C104KA87	Murata	R503	10kΩ	2010	EXB-28V103JX	KOA
C124	0.1uF	1005	GRM155B31C104KA87	Murata	R504	10kΩ	2010	EXB-28V103JX	KOA
C125	0.1uF	1005	GRM155B31C104KA87	Murata	R911	0Ω(NC)	3216	CNZ1J4	KOA
C126	0.1uF	1005	GRM155B31C104KA87	Murata	R912	0Ω(NC)	3216	CNZ1J4	KOA
C127	0.1uF	1005	GRM155B31C104KA87	Murata	R913	0Ω(NC)	3216	CNZ1J4	KOA
C128	0.1uF	1005	GRM155B31C104KA87	Murata	R914	0Ω(NC)	3216	CNZ1J4	KOA
C129	0.1uF	1005	GRM155B31C104KA87	Murata	R915	0Ω(NC)	3216	CNZ1J4	KOA
C130	0.1uF	1005	GRM155B31C104KA87	Murata	R916	0Ω(NC)	3216	CNZ1J4	KOA
C131	0.1uF	1005	GRM155B31C104KA87	Murata	R921	0Ω(NC)	3216	CNZ1J4	KOA
C132	0.1uF	1005	GRM155B31C104KA87	Murata	R922	0Ω(NC)	3216	CNZ1J4	KOA
C141	10uF	2012	GRM21BB31C106KE15	Murata	R923	0Ω(NC)	3216	CNZ1J4	KOA
C142	10uF	2012	GRM21BB31C106KE15	Murata	R924	0Ω(NC)	3216	CNZ1J4	KOA
C151	10uF (NC)	2012	GRM21BB31C106KE15	Murata	R925	0Ω(NC)	3216	CNZ1J4	KOA
C152	10uF (NC)	2012	GRM21BB31C106KE15	Murata	R926	0Ω(NC)	3216	CNZ1J4	KOA
C153	10uF (NC)	2012	GRM21BB31C106KE15	Murata	SW501	DIP8	2206	A6S-8104-H	Omuron
C154	10uF (NC)	2012	GRM21BB31C106KE15	Murata	SW502	DIP8	2206	A6S-8104-H	Omuron
C161	4.7uF(NC)	1608	GRM185B31C475KE43	Murata	TP101	HK-2-G	3216	HK-2-G	Mac8
C162	4.7uF(NC)	1608	GRM185B31C475KE43	Murata	TPG1	HK-2-G	3216	HK-2-G	Mac8
C163	4.7uF(NC)	1608	GRM185B31C475KE43	Murata	U101	V-by-One-Rx	TQFP128	THCV226	THine
C164	4.7uF(NC)	1608	GRM185B31C475KE43	Murata	U102	LDO1.8V	SC-63	uPC2918BT-AZ	NEC
C165	4.7uF(NC)	1608	GRM185B31C475KE43	Murata	U301	LDO3.3V	SC-63	uPC2933BT-AZ	NEC
C301	10uF	2012	GRM21BB31C106KE15	Murata	U401	MOSFET	1616	SSM3K16FS	Toshiba
C302	10uF	2012	GRM21BB31C106KE15	Murata					
C303	10uF	2012	GRM21BB31C106KE15	Murata					
CN101	31pin	2804	FX16-31S-0.5SH	HRS					
CN102	41pin	3404	FX15SC-41S-0.5SH	HRS					
CN103	51pin	3804	FX15SC-51S-0.5SH	HRS					
CN301	DC12V	1105	ML-800-S1H-2P	Sato-parts					
CN901	FI-X30SSLB-HF(NC)	-	FI-X30SSLB-HF	JAE					
CN902	FI-X30SSLB-HF(NC)	-	FI-X30SSLB-HF	JAE					

10. Layout

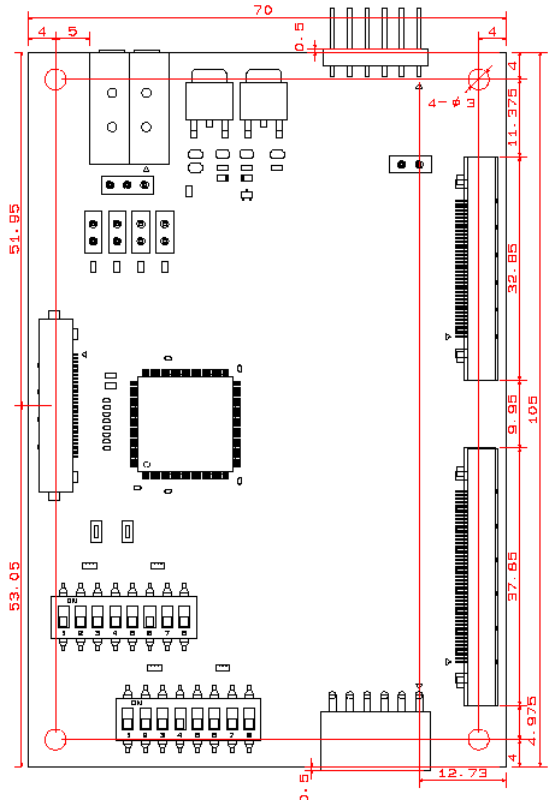


Figure10.1 Board Size (Unit: mm)

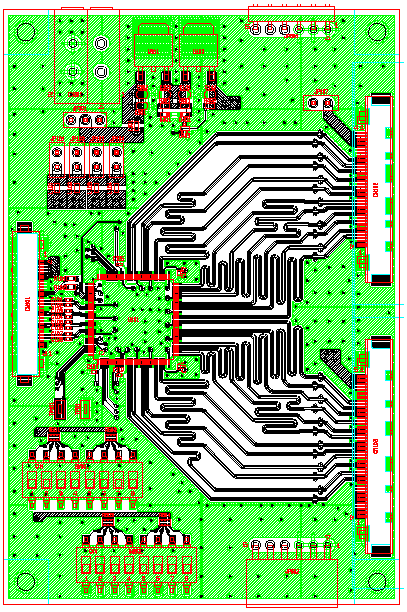


Figure10.2 COMPONENT SIDE – LAYER 1

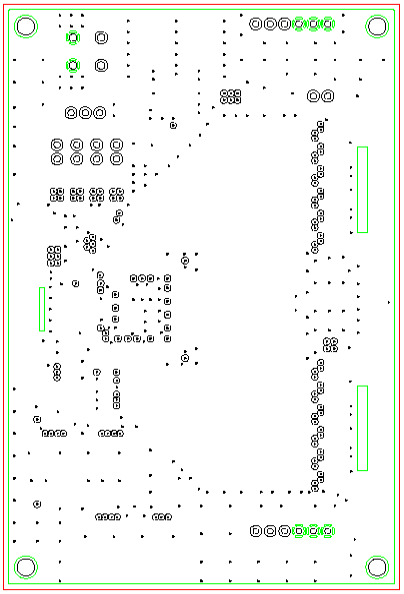


Figure10.2 GROUND PLANE – LAYER 2

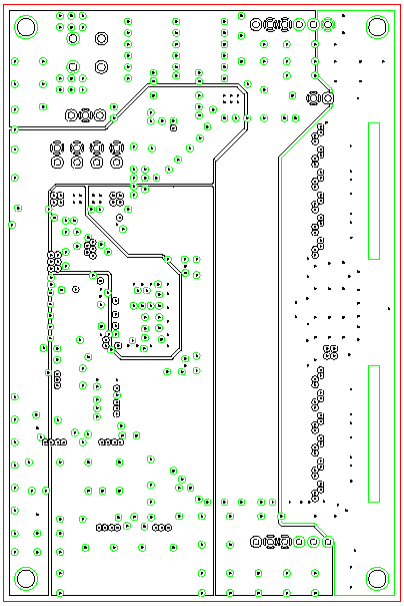


Figure10.3 POWER PLANE – LAYER 3

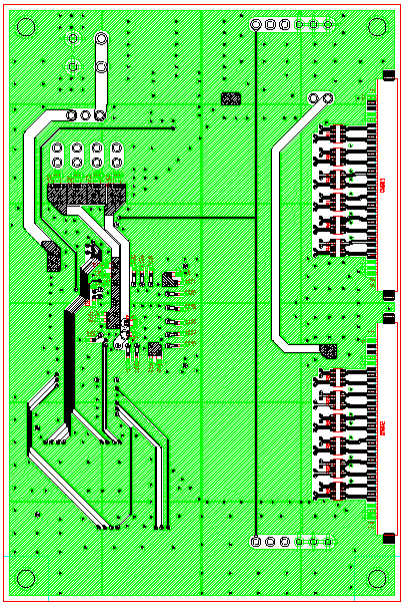
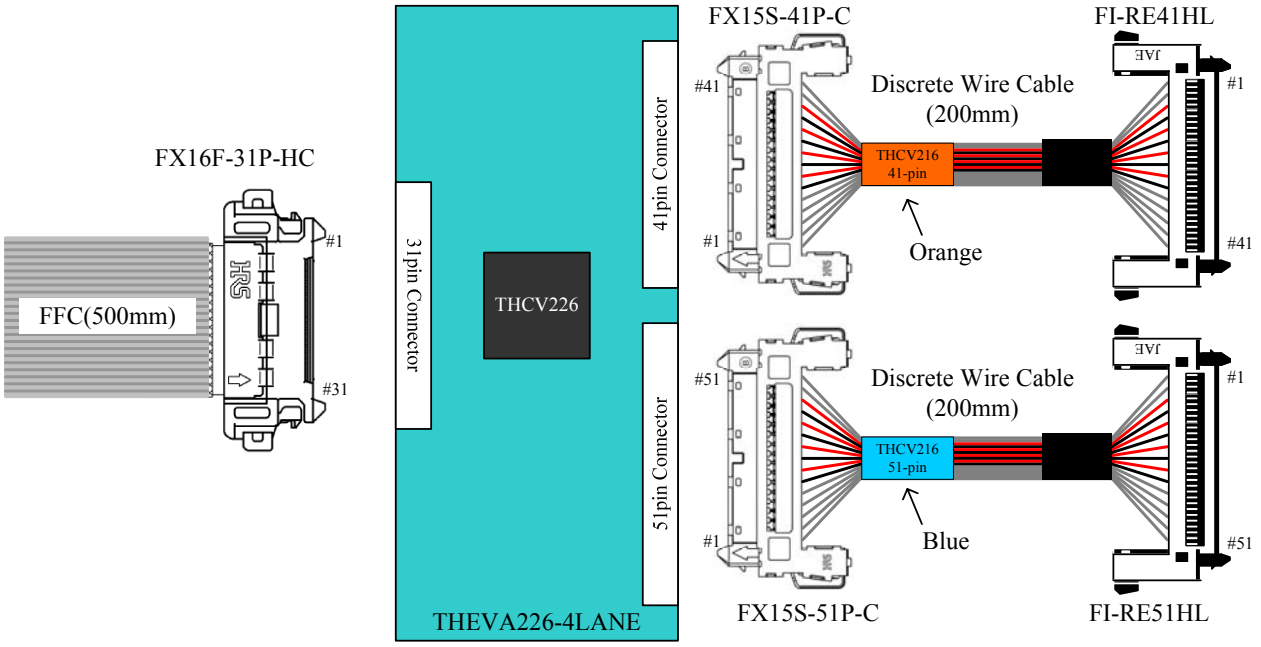


Figure10.4 SOLDER SIDE – LAYER 4

11. Set items



12. Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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