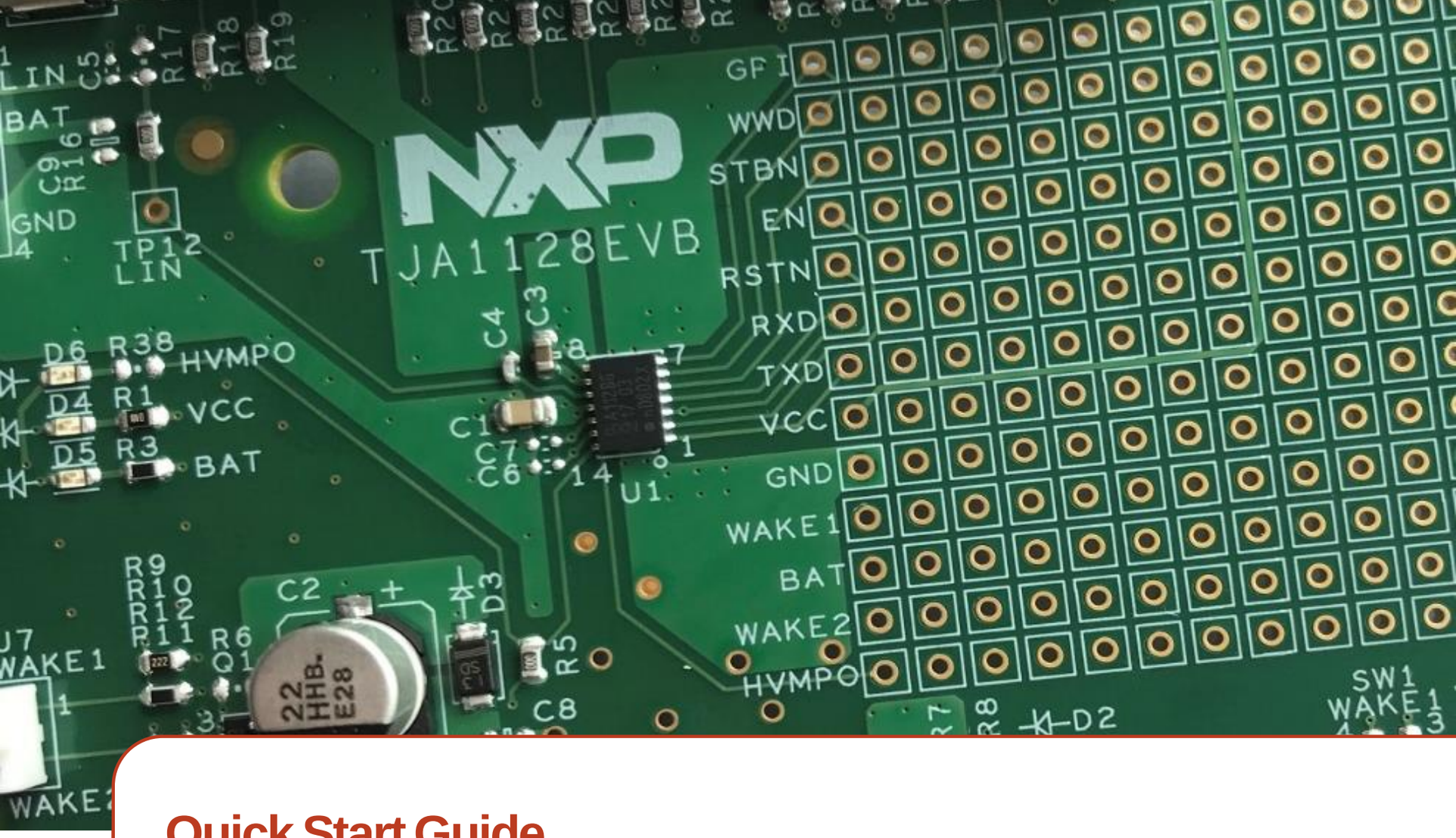


Quick Start Guide

TJA1128EVB

Evaluation Board for TJA1128 LIN Mini System Basis Chip

Arduino™ UNO footprint-compatible LIN Communication Shield

GET TO KNOW THE TJA1128 EVALUATION BOARD

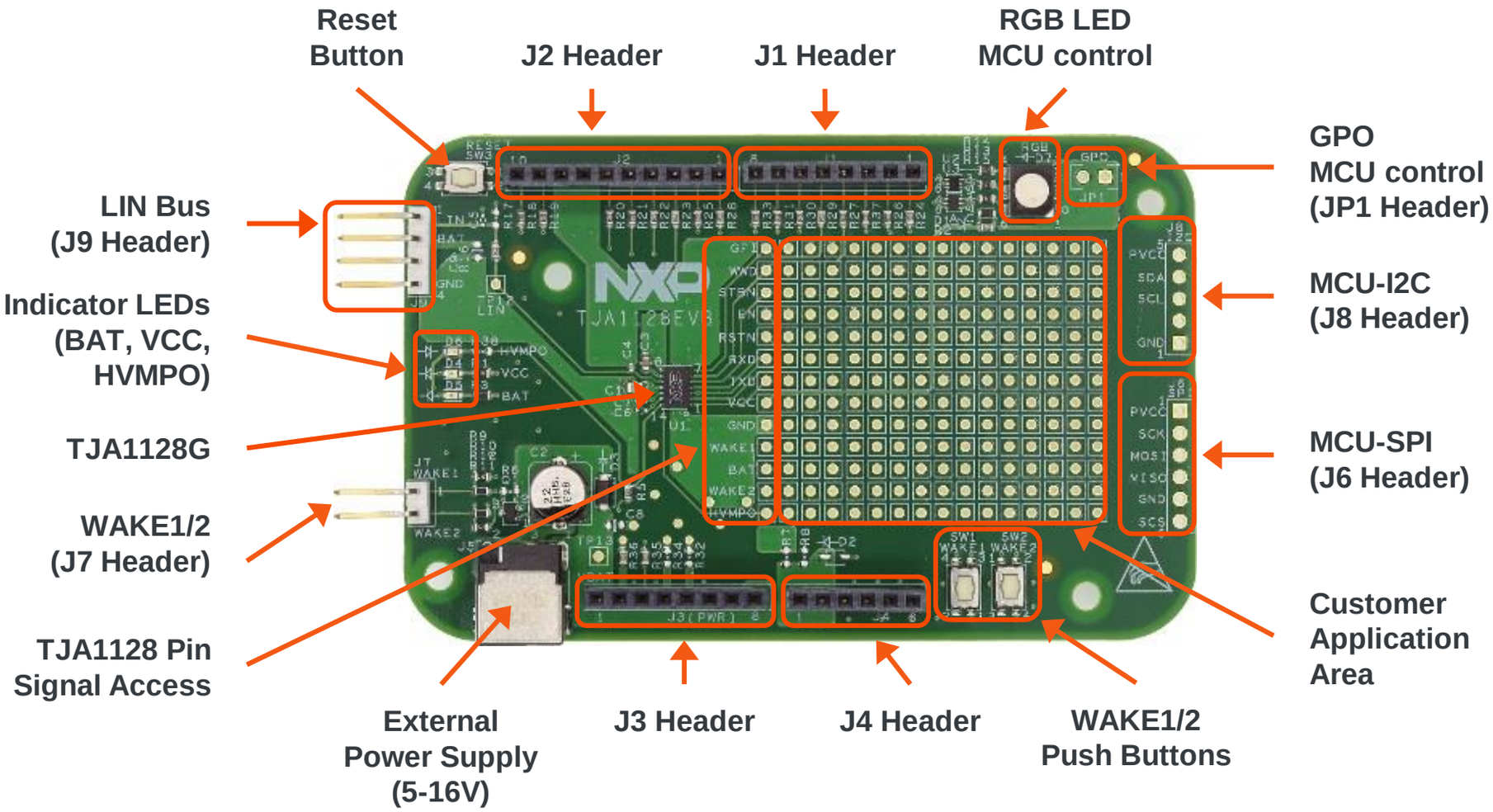


Figure 1: Front side of TJA1128EVB

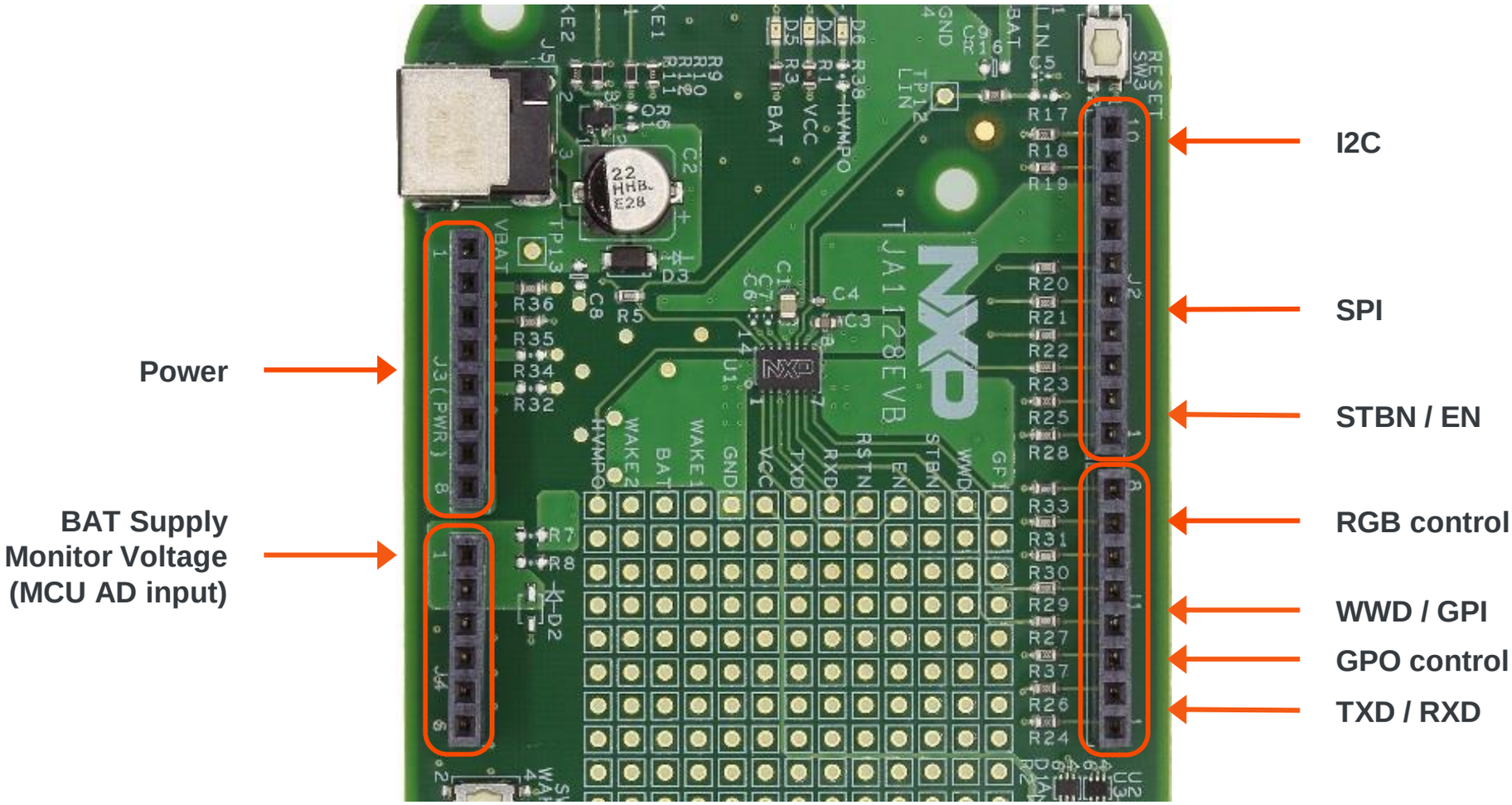


Figure 2: TJA1128EVB footprint

TJA1128EVB

Arduino™ UNO footpint-compatible shield

The TJA1128 EVB has the standard-based form factor compatible with Arduino™ UNO pin layout, that enables rapid prototyping with a wide range of microcontroller development boards.

Example: TJA1128EVB + S32K144EVB

FEATURES

- LIN Mini SBC TJA1128G with
  - Low-dropout voltage regulator (5V)
  - Window watchdog
  - 2 WAKE inputs
  - General purpose input
  - High-voltage multipurpose output
- LIN connector
- WAKE connector
- WAKE push buttons
- Reset button
- Arduino™ UNO footprint-compatible shield
- Power LED indicator
- VCC LED indicator
- HVMPO LED indicators
- RGB LED
- GPO
- Easy access to
  - TJA1128G pins
  - MCU SPI port pins
  - MCU I2C port pins
- On-board application circuit options
  - Cyclic sampled wake-up on WAKE1 and WAKE2 with synchronized bias control via pin HVMPO
  - Continuous wake-up detection on WAKE1 and WAKE2
  - Battery supply voltage monitor circuit with connection to ADC port pin of MCU
- Customer application field
- Small form factor

MICROCONTROLLER BOARD COMPATIBILITY

- S32K142EVB
- S32K144EVB
- DEVKIT-MPC5748G
- FRDM-KEAZ128
- etc.

STEP-BY-STEP INSTRUCTIONS

This section describes how to use the TJA1128 evaluation board as a hardware plug-in board (shield) that supports basic LIN slave prototyping when plugged on existing microcontroller (MCU) development boards.

1 Verification of Supply Setting

The supply connector pin mapping of J3 Header (see Figure 3) must be checked against MCU board supply circuitry and connector. Otherwise TJA1128 and other components on the board can be damaged.

VBAT is the power supply voltage (max 16V). As default configuration TJA_VCC is connected via a zero-ohm resistor (R36) to the output of the low-dropout voltage regulator (LDO) from the TJA1128.

Figure 3: J3 Header (supply connector) pin mapping options

As alternative P3V3 or P5V0 can be used by populating a zero-ohm resistor to the appropriate placeholder (R32 or R34).

If reverse supply from MCU board to TJA1128 LDO output cannot be prevented, it is recommended to remove the zero-ohm resistor R2 to activate the reverse current protection diode D1. See Figure 4.

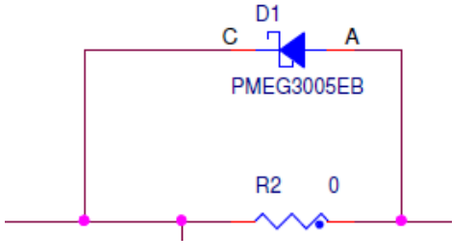


Figure 4: Reverse supply protection with D1

The TJA1128EVB can be supplied by VBAT either via connector J5 or connector J9 or connector J3.

STEP-BY-STEP INSTRUCTIONS (cont.)

2 Microcontroller Supply Current

The TJA1128 LDO output current on pin VCC is limited to maximum 85 mA. Hence, the current consumption of the applied MCU development board must be checked.

Furthermore, if the on-board RGB LED D7 is used, the maximum supply current for the MCU board decreases to 65 mA. See Figure 5.

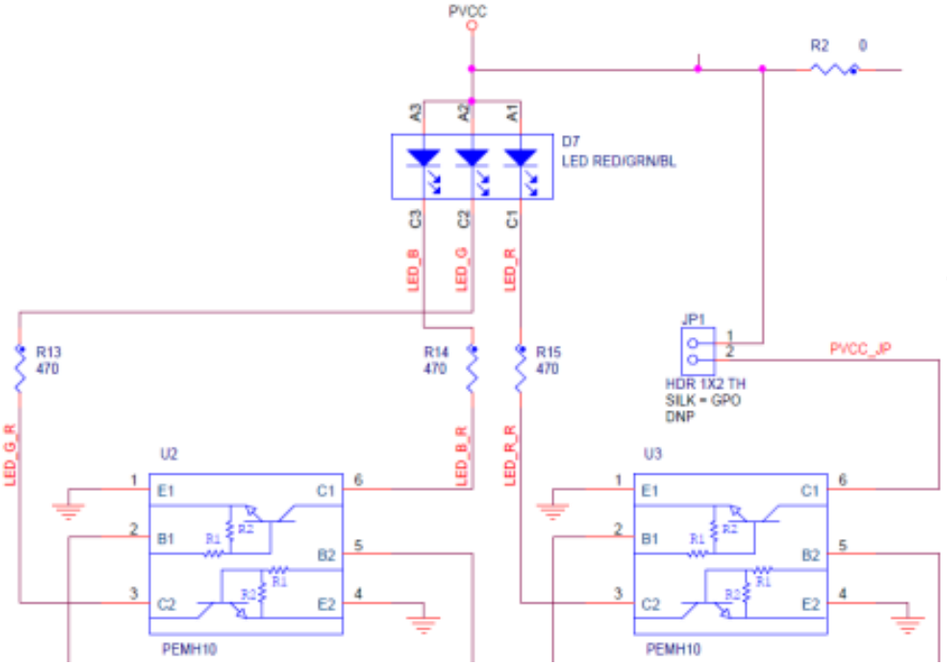


Figure 5: On-board circuit options associated with pin VCC

A load on connector JP1 would further decrease the supply current budget for the MCU board.

3 TJA1128G Configuration on Evaluation Board

The populated TJA1128G is already configured to support the populated default application on the TJA1128EVB. Cyclic sampled wake-up detection on the pins WAKE1 and WAKE2 is activated.

In addition the window watchdog function and software development mode are enabled.

Detailed configuration information is listed on page 8.

Note:

- In software development mode the window watchdog can be disabled when during the transition from RESET to STANDBY the input level on the WWD pin is LOW.
- After a restore to the factory preset values the TJA1128G can be reconfigured with another configuration. See data sheet for further information.

STEP-BY-STEP INSTRUCTIONS (cont.)

4 Default Application: Cyclic Wake Detection

With the default population the TJA1128EVB is prepared for cyclic sampled wake-up detection on WAKE1 (SW1 or J7-1) and WAKE2 (SW2 or J7-2). For this purpose the HVMPO output controls via the PNP Q1 the cyclic pull-up bias for R10 and R12. See Figure 6.

See data sheet for further details about cyclic sampling with WAKE1 and WAKE2.

5 Optional Application: Continuous Wake Detection

For continuous wake detection on WAKE1 (SW1 or J7-1) and WAKE2 (SW2 or J7-2) the continuous bias can be provided by populating zero-ohm resistor on R6 and depopulating the zero-ohm resistor R5. See Figure 6.

This enables the HVMPO output for other application use cases, e.g. to indicate the device mode on D6 by populating R38 with 15kΩ.

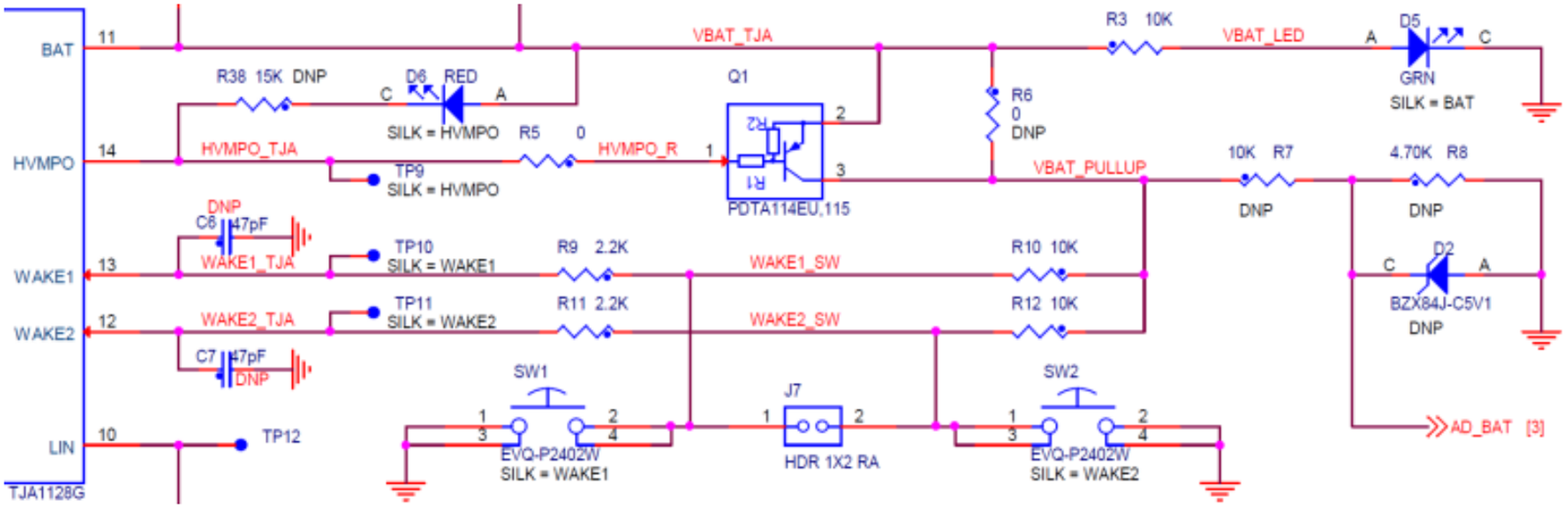


Figure 6: Application circuit options

STEP-BY-STEP INSTRUCTIONS (cont.)

6 Optional Application: LIMP Home Output

The pin HVMPO can be configured as LIMP home output to enable so-called limp home hardware.

The HVMPO LIMP home output signal is available at the customer application area of the TJA1128EVB. With the default population the zero-ohm resistor R5 is populated. It should be checked whether R5 needs to be depopulated.

As an alternative the HVMPO LIMP home output can use the PNP Q1 to get a high-side limp home switch. With the default population this signal is routed to connector J7. It should be checked whether R9 and R11 needs to be depopulated. Further, it should be checked whether the 10kΩ pull-up resistors R10 and R12 fit to the customer limp home hardware.

7 Optional Application: Battery Supply Monitor

The pin HVMPO can be configured to act as a function of the TJA1128 mode. Various TJA1128 mode controlled output functions are available, e.g. HVMPO is active LOW in NORMAL mode, else off. For further configuration details see data sheet.

In such HVMPO configuration the PNP Q1 can be used to switch on the bias current for the voltage divider out of R7 and R8. See Figure 6. This voltage divider can be used to monitor the battery supply voltage. The battery monitor signal AD_BAT is routed to connector J4-1.

For the battery monitoring R7, R8 and D2 have to be populated. The resistor value for R7 and R8 and the clamping voltage of D2 depends on the used MCU. It is recommended to depopulate R10 and R12.

STEP-BY-STEP INSTRUCTIONS (cont.)

8 Application Area with Easy Access TJA1128G

The TJA1128EVB provides a customer application area with easy access to all TJA1128G signals and to MCU SPI and I2C signals. All TJA1128G signals are routed to the left side and the MCU I2C and SPI signals are routed to the right side.

This area can be used to add application specific circuits to support rapid prototyping of LIN slave applications.

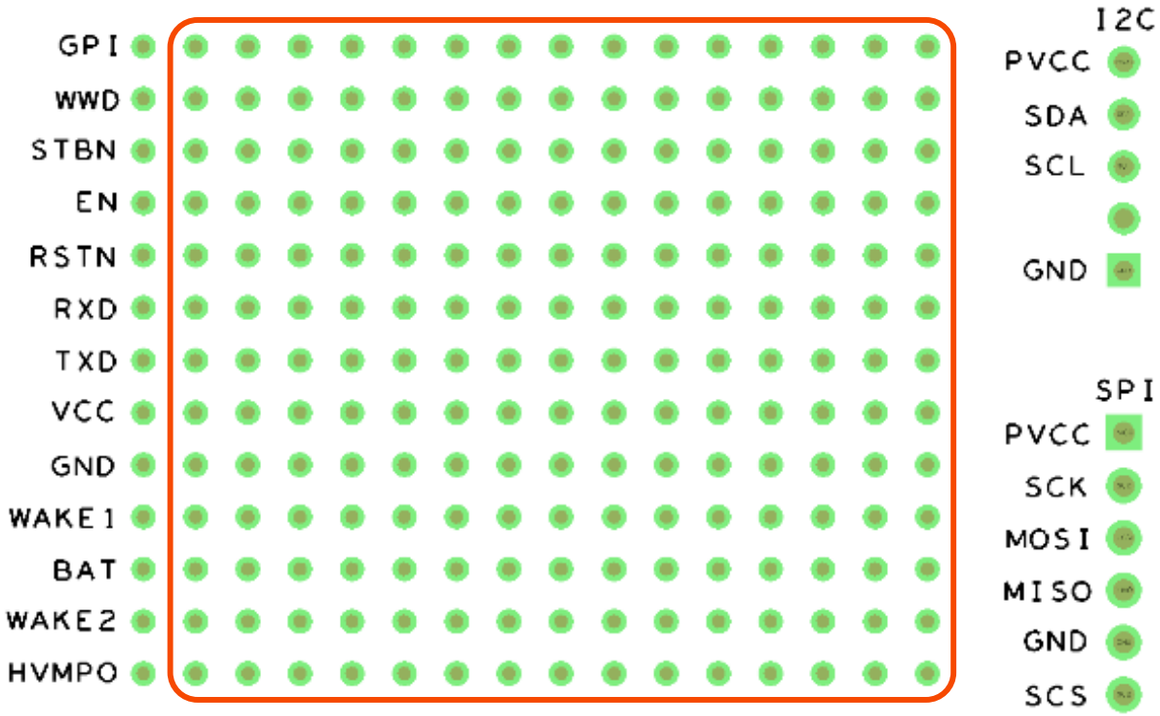


Figure 7: Customer application area

TJA1128G – EVB DEFAULT CONFIGURATION

Register	Bit(s)	Configuration
System	DISSLP	SLEEP mode enabled
	RSTTIM	RSTN output reset pulse width: 4 ms
Wake	LC1WKE	Local wake-up on falling edge
	LC2WKE	Local wake-up on falling edge
	BUSWKE	LIN wake-up enabled
LDO	DISVCCUV	VCC undervoltage detection enabled
LIN	DISTXTO	LIN TXD dominant time-out enabled
	HSMODE	LIN high-speed mode disabled
	DISLIN	LIN transceiver enabled

TJA1128G – EVB DEFAULT CONFIGURATION (cont.)

Register	Bit(s)	Configuration
Watchdog	WDMOD	Window mode
	WDAUTO	Autonomous mode enabled
	WDPER	Watchdog nominal period: 64 ms
	WDSDM	Software development mode enabled
HVMPO	MPOMOD	Bias control output for cyclic wake-up
	MPOINV	HVMPO not inverted
	WKBPER	Cyclic wake nominal period time: 64 ms
	WKBSET	Cyclic wake nominal settle time: 134µs

J1 HEADER – DEFAULT SETTING

J1 Header	Resistor	Default Setting	Signal	Description
J1-1	R24	0	TJA_RXD	TJA1128 RXD (SDO) output
J1-2	R26	0	TJA_TXD	TJA1128 TXD (SDI) input
J1-3	R37	0	GPO	NPN input to control GPO (JP1)
J1-4	R27	0	TJA_WWD	TJA1128 WWD input
J1-5	R29	0	TJA_GPI	TJA1128 GPI input
J1-6	R30	0	LED1	NPN input to control LED1 (RGB red)
J1-7	R31	0	LED2	NPN input to control LED2 (RGB green)
J1-8	R33	0	LED3	NPN input to control LED3 (RGB blue)

J2 HEADER – DEFAULT SETTING

J2 Header	Resistor	Default Setting	Signal	Description
J2-1	R28	open	TJA_EN	TJA1128 EN (SCK) input
J2-2	R25	0	TJA_STBN	TJA1128 STBN (SCSN) input
J2-3	R23	0	SCS	SPI chip select routed to J6-6
J2-4	R22	0	MOSI	SPI slave data input routed to J6-3
J2-5	R21	0	MISO	SPI slave data output routed to J6-4
J2-6	R20	0	SCK	SPI slave clock input routed to J6-2
J2-7	-	-	GND	Ground
J2-8	-	-	-	Not connected
J2-9	R19	0	SDA	I2C serial data routed to J8-4
J2-10	R18	0	SCL	I2C serial clock routed to J8-3

J3 HEADER – DEFAULT SETTING

J3 Header	Resistor	Default Setting	Signal	Description
J3-1	-	-	-	Not connected
J3-2	R36	0	TJA_VCC	TJA1128 VCC (voltage regulator) output
J3-3	R35	0	TJA_RSTN	TJA1128 RSTN (reset) input / output
J3-4	R34	open	P3V3	Alternative TJA1128 VCC output routing
J3-5	R32	open	P5V0	Alternative TJA1128 VCC output routing
J3-6	-	-	GND	Ground
J3-7	-	-	GND	Ground
J3-8	-	-	VBAT	Power supply

J4 HEADER – DEFAULT SETTING

J4 Header	Resistor	Default Setting	Signal	Description
J4-1	-	-	AD_BAT	Supply monitoring voltage for MCU ADC input
J4-2	-	-	-	Not connected
J4-3	-	-	-	Not connected
J4-4	-	-	-	Not connected
J4-5	-	-	-	Not connected
J4-6	-	-	-	Not connected

J5 HEADER – EXTERNAL POWER SUPPLY

J5 Header	Signal	Description
J5-1	VBAT	Power supply
J5-2	GND	Ground
J5-3	GND	Ground

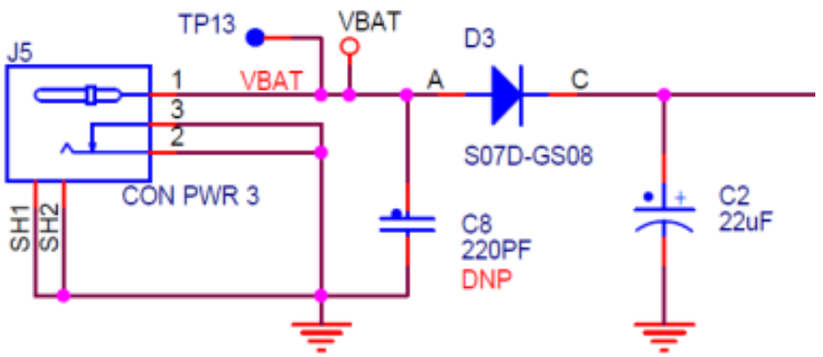


Figure 8: Power supply circuit

J6 HEADER – MCU SPI

J6 Header	Resistor	Default Setting	Signal	Description
J6-1	-	-	PVCC	TJA1128 VCC (voltage regulator) voltage
J6-2	R20	0	SCK	SPI slave clock input routed to J2-6
J6-3	R22	0	MOSI	SPI slave data input routed to J2-4
J6-4	R21	0	MISO	SPI slave data output routed to J2-5
J6-5	-	-	GND	Ground
J6-6	R23	0	SCS	SPI chip select routed to J2-3

J7 HEADER – WAKE1/2

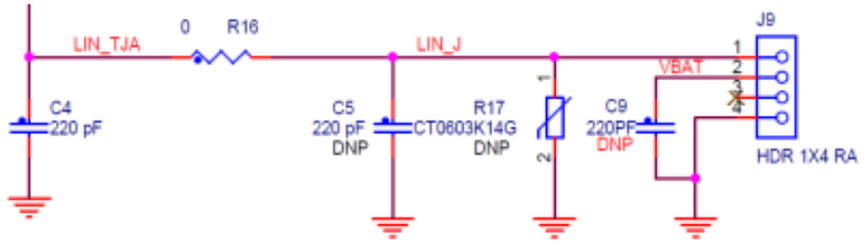
J7 Header	Resistor	Default Setting	Signal	Description
J7-1	R9	2.2kΩ	WAKE1	WAKE1 input
J7-2	R11	2.2kΩ	WAKE2	WAKE2 input

J8 HEADER – MCU I2C

J8 Header	Resistor	Default Setting	Signal	Description
J8-1	-	-	GND	Ground
J8-2	-	-	-	Not connected
J8-3	R18	0	SCL	I2C serial clock routed to J2-10
J8-4	R19	0	SDA	I2C serial data routed to J2-9
J8-5	-	-	PVCC	TJA1128 VCC (voltage regulator) voltage

J9 HEADER – LIN BUS

J9 Header	Resistor	Default Setting	Signal	Description
J9-1	R16	0	LIN	LIN bus
J9-2	-	-	VBAT	Power supply
J9-3	-	-	-	Not connected
J9-4	-	-	GND	Ground



Place C4 close to the LIN pin of TJA1128

Place C5, C9, R17 close to connector J9

Figure 9: LIN circuit

SUPPORT

Visit **www.nxp.com/support** for technical communities and support requests.

WARRANTY

Visit **www.nxp.com/warranty** for complete warranty information.

Get Started

Download example software and documentation from NXP DocStore (NDA required) www.docstore.nxp.com.

In-Vehicle Networking → LIN → TJA1128

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