4 ch Current Driver Integrated, Built-in MOS for Boost DC/DC Controller

White LED Driver for Automotive

BD83A14EFV-M BD83A14MUF-M

General Description

This IC is a white LED driver for LCD backlight.
It has 4 ch current drivers for LED drive, making it ideal for high brightness LED drive. LED pin maximum voltage is 50 V, making it suitable for driving medium LCD panels.
The dimming is controlled by the PWM signal and can be set up to 20,000: 1@100 Hz. It also supports analog dimming and can accommodate even higher brightness ranges by combining with PWM dimming. DC/DC converters can be controlled for boost applications, and the input operating voltage range is 4.5 V to 48.0 V.

Features

- AEC-Q100 Qualified(Note 1)
- Functional Safety Supportive Automotive Products
- Built-in 4 ch Current Driver for LED Driver
- Current Mode Boost DC/DC Converter
- Load Switch (M1) Control Pin
- DC Dimming Function by Pulse Input
- PWM Dimming
  (20,000: 1@100 Hz, 100 Hz to 25 kHz)
- Spread Spectrum Function
- DC/DC Converter Oscillation Frequency External Synchronization Function
- LSI Protect Functions (UVLO, OVP, TSD, OCP)
- LED Anode/Cathode Short Circuit Protection Function
- LED Open/Short Protection Function

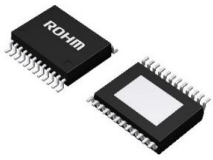
(Note 1) Grade 1

Key Specifications

- Input Operating Voltage Range: 4.5 V to 48.0 V
- Output LED Current Absolute Accuracy:
  ±5.0 %@80.1 mA
  Ta = -40 °C to +125 °C
- DC/DC Oscillation Frequency: 200 kHz to 2420 kHz
- Operating Temperature: -40 °C to +125 °C
- LED Maximum Current: 150 mA / ch
- LED Maximum Dimming Ratio: 20,000: 1@100 Hz
- LED1 to LED4 Pin Maximum Voltage: 50 V

Packages

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B24	7.8 mm x 7.6 mm x 1.0 mm
VQFN24FV4040	4.0 mm x 4.0 mm x 1.0 mm



HTSSOP-B24
BD83A14EFV-M

VQFN24FV4040
BD83A14MUF-M

Applications

- Automotive CID (Center Information Display) Panel
- Navigation
- Cluster Panel
- HUD (Head Up Display)
- Other Small and Medium Sized LCD Panel for Automotive

Typical Application Circuit

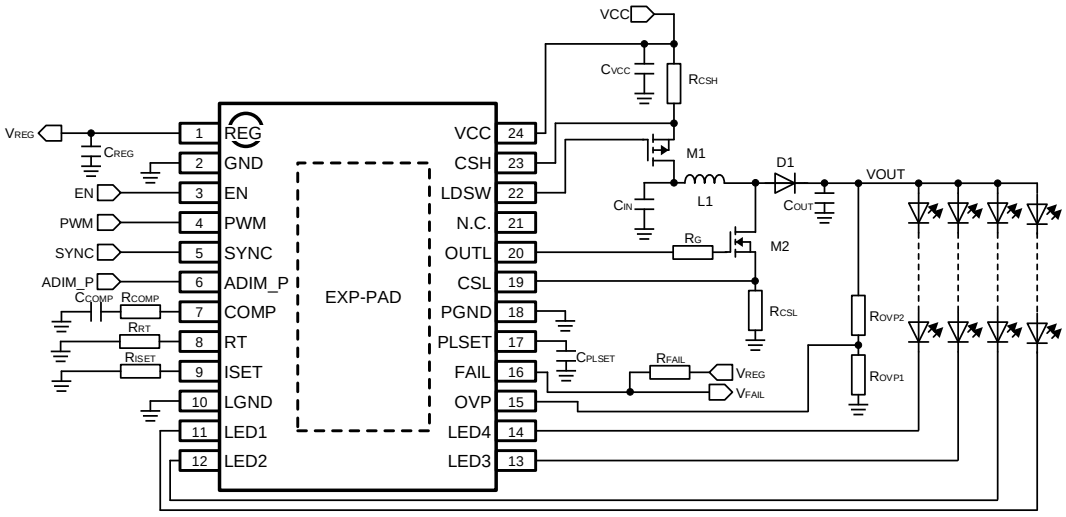


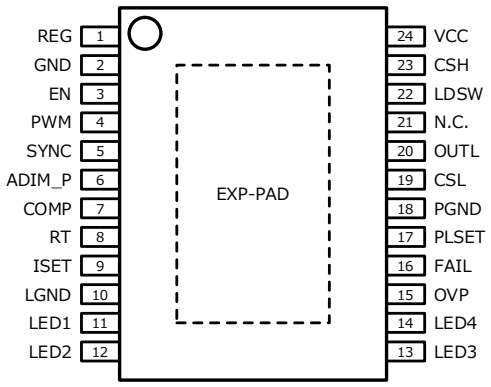
Figure 1. Boost Application Circuit Diagram

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.
○This product is protected by U.S. Patent No.7,235,954, No.7,541,785 and No.7,944,189.

Contents

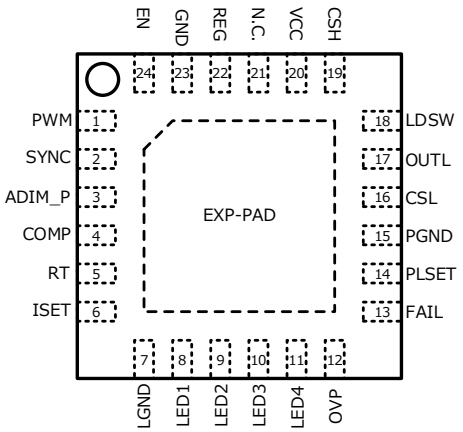
Pin Configurations

(TOP VIEW)



BD83A14EFV-M

(TOP VIEW)



BD83A14MUF-M

Pin Descriptions

Pin No.		Pin Name	Signal Type *(Note 1)*	Function
EFV	MUF			
1	22	REG	A	**Internal reference voltage:** Used as the reference voltage for the internal circuit. 5 V is generated and output by setting the EN pin to High. Connect a capacitance of 2.2 µF for phase compensation.
2	23	GND	A	**Small signal ground:** Use this for the ground of external components connected to the REG, RT, COMP, ADIM_P, ISET, PLSET, OVP, and VCC pins.
3	24	EN	I	**Enable input:** The EN pin is turned High to activate the internal circuit. The internal circuit stops and the standby state is set by setting to Low.
4	1	PWM	I	**PWM dimming signal:** The LED current can be controlled according to On Duty of the input PWM signal.
5	2	SYNC	I	**External synchronization frequency input / SSCG setting:** The internal oscillation frequency can be externally synchronized by inputting an external clock signal to the SYNC pin before the Self Diagnosis is completed. When using spread spectrum mode (SSCG), short the SYNC pin and the REG pin beforehand.
6	3	ADIM_P	I	**DC dimming setting:** The ISET pin voltage can be changed by On Duty of the pulse signal input to the ADIM_P pin. When using only PWM dimming, short the ADIM_P pin with the REG pin.
7	4	COMP	A	**Phase compensating capacitor connection:** The reference voltage and LED pin voltage generated by REF Voltage block are compared and output by Error AMP. Connect a filter for phase compensation.
8	5	RT	A	**Resistor connection for oscillation frequency setting:** The oscillation frequency (f_{OSC}) of DC/DC converter can be set by connecting a resistor (R_{RT}) between the RT pin and the GND pin.
9	6	ISET	A	**Resistor connection for LED current setting:** LED current (I_{LED}) can be set by connecting a resistor (R_{ISET}) between the ISET pin and the GND pin.
10	7	LGND	P	**Large current ground 1:** GND of the current driver (the LED1, LED2, LED3, and LED4 pins).
11	8	LED1	P	**LED cathode connection 1:** Open drain output of the current driver ch 1 for LED drive. Connect to the LED cathode.
12	9	LED2	P	**LED cathode connection 2:** Open drain output of the current driver ch 2 for LED drive. Connect to the LED cathode.
13	10	LED3	P	**LED cathode connection 3:** Open drain output of the current driver ch 3 for LED drive. Connect to the LED cathode.
14	11	LED4	P	**LED cathode connection 4:** Open drain output of the current driver ch 4 for LED drive. Connect to the LED cathode.

(Note 1) **A:** Sensitive signal such as detect and reference, **I:** Input signal from other units, **O:** Output signal to other units, **P:** Large current signal susceptible to impedance, including transient current.

Pin Descriptions – continued

Pin No. EFV	Pin No. MUF	Pin Name	Signal Type *(Note 1)*	Function
15	12	OVP	A	**Overvoltage protection and short circuit protection detection :** When OVP pin voltage rises to 1.21 V or more, the overvoltage protection (OVP) is activated, and DC/DC converters are switched OFF. If OVP pin voltage is 0.1 V or less for 3.56 ms, Short Circuit Protection (SCP) is activated, and both DC/DC converter and the current driver are turned OFF.
16	13	FAIL	O	**Error output flag:** Outputs the status of protective operation from the FAIL pin. Since this pin is an open drain output, use a resistor to pull it up to the REG pin, etc.
17	14	PLSET	A	**Switching pulse number setting:** Pulse addition function is provided to stabilize DC/DC converter output voltage even when PWM Duty is low. The number of switching pulses to be added can be set by the capacitance value connected between the PLSET pin and the GND pin.
18	15	PGND	P	**Large current ground 2:** Use it for external parts connected to the OUTL pin.
19	16	CSL	A	**Overcurrent protection detection input:** The current flowing through the Low side FET (M2) is voltage-converted by the overcurrent detection resistor (R_{CSL}) and detected by the CSL pin. When overcurrent protection (OCPL) is activated, it turns off DC / DC converter switching.
20	17	OUTL	P	**Low side FET gate signal:** The switching signal output of the DC/DC converter. Connect the OUTL pin to the gate of the Low side FET (M2). *(Note 2)*
21	21	N.C.	-	Not connected internally.
22	18	LDSW	P	**Output for driving the load switch gate:** The signal output for driving the gate of the load switch. When the input overcurrent protection is activated, the load switch is turned OFF as LDSW pin voltage = VCC pin voltage. *(Note 2)*
23	19	CSH	A	**Input current detection input:** The input current is converted to voltage by the input current detection resistor (R_{CSH}) connected between the VCC-CSH pin and detected by the CSH pin. Turns the load switch OFF when the input overcurrent protection is activated.
24	20	VCC	P	**Power supply voltage input:** The input operating voltage range is 4.5 V to 48.0 V, but when the IC is started, start it with VCC ≥ 5.5 V. The decoupling capacitor (C_{VCC}) between the VCC pin and the GND pin should be as close to the IC pin as possible.
-		EXP-PAD	-	The EXP-PAD should be connected to the board ground.

(Note 1) **A:** Sensitive signal such as detect and reference, **I:** Input signal from other units, **O:** Output signal to other units, **P:** Large current signal susceptible to impedance, including transient current.

(Note 2) The MUF package requires external components to prevent adjacent short between the OUTL pin and the LDSW pin. If concerned, consider the EFV package.

Block Diagram

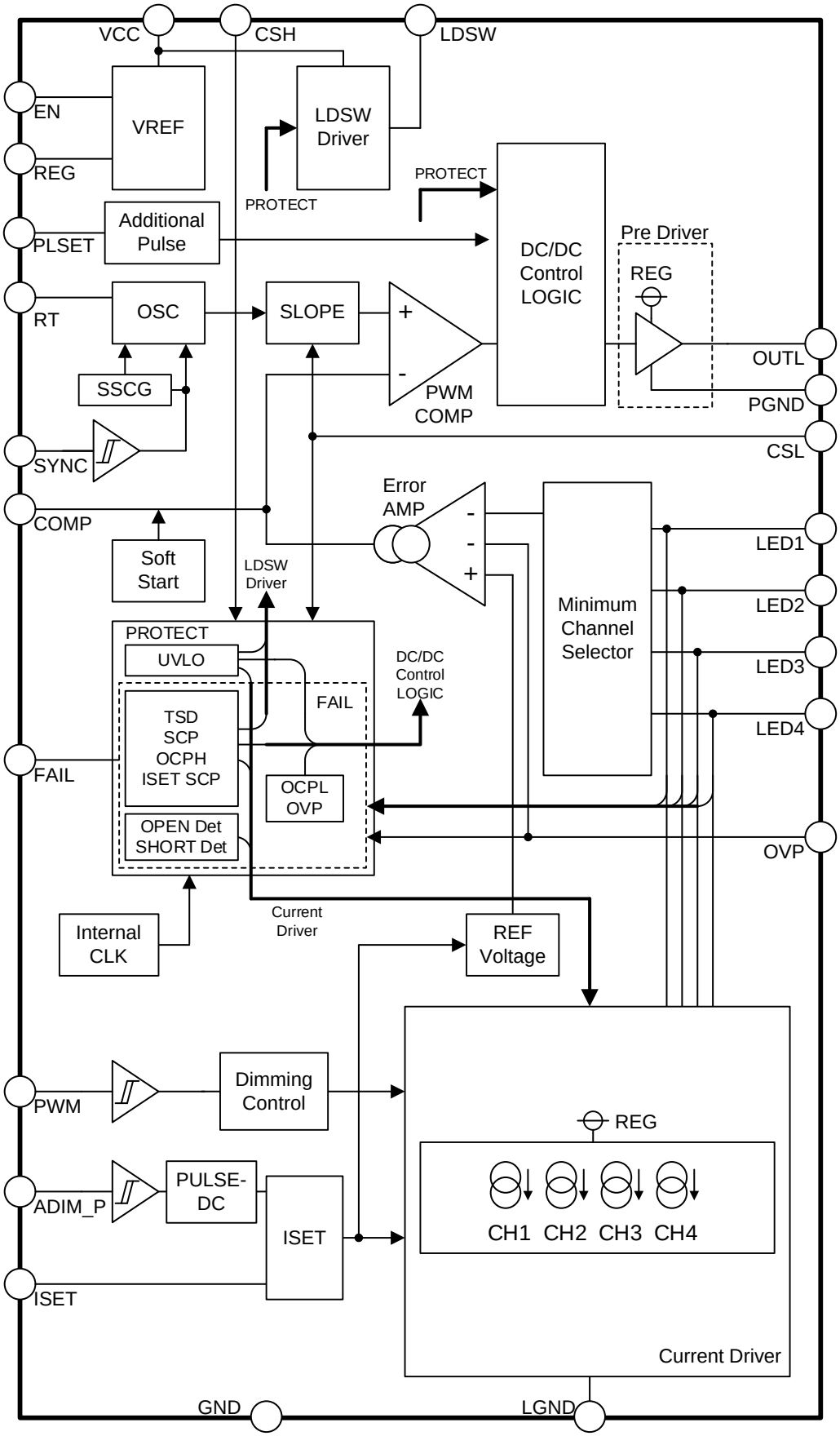


Figure 2. Internal Block Diagram

Description of Blocks

Unless otherwise stated, the value in the sentence is the typical value.

1 VREF

Internal reference voltage circuit. By setting the EN pin to High, 5 V is generated and output to the REG pin. REG voltage is used as the power supply for the internal circuit. Also, this is used to fix each input pin to High voltage outside the IC. Connect REG capacitance (C_{REG} = 2.2 µF) to the REG pin for the phase compensation. Note that if C_{REG} is not connected, unstable operation such as oscillation will occur.

2 LDSW Driver

Input overcurrent protection circuit. If the voltage between the VCC-CSH pin is 0.1 V or more and continues for 10 µs or more, the input overcurrent protection is activated, and the load switch (M1) is turned OFF as LDSW pin voltage = VCC pin voltage. Then, after 56.96 ms elapses, the load switch is turned ON. At this time, if the voltage between the VCC-CSH pin is 0.1 V or more, the load switch is turned OFF again. If the voltage between the VCC-CSH pin is less than 0.1 V, Self Diagnosis is performed and restarted. When the input overcurrent protection is detected, the FAIL pin goes Low. The VCC-LDSW pin is connected by a 3 MΩ resistor inside the IC. Do not connect a resistor between the VCC-LDSW pin because connecting a resistor between the VCC-LDSW pin outside the IC may prevent the load switch from being turned ON.
When the VCC pin voltage is turned ON setting the EN pin to Low, the voltage between the VCC-LDSW pins may open momentarily and an inrush current may flow depending on the VCC startup speed and the type of load switch used. Be sure to check with the actual application.

3 OSC (Oscillator)

Oscillation frequency generator. The oscillation frequency (f_{OSC}) of DC/DC converter can be set by connecting a resistor for oscillation frequency setting (R_{RT}) between the RT pin and ground. In addition, the oscillation frequency of DC/DC converter can be externally synchronized by inputting the external synchronization frequency (f_{SYNC}) to the SYNC pin.

4 SSCG (Spread Spectrum Clock Generator)

Spread spectrum circuit. The spread spectrum function (SSCG) is activated by shorting the SYNC pin and the REG pin. Noise peaks can be reduced by periodically changing the oscillation frequency by SSCG. The fluctuation range of the frequency due to SSCG is from 100 % to 92 % of the set oscillation frequency. The oscillation frequency fluctuation period is 2.3 kHz.

5 SLOPE

This circuit generates a saw wave that serves as the source of the switching pulse of DC/DC converter. SLOPE output signal and COMP pin voltage are compared, and a switching pulse is generated.

6 Minimum Channel Selector

Selector circuit for detecting LED pin voltages. Selects the lowest pin voltage among LED1 to LED4 pin voltages and inputs it in Error AMP.

7 Error AMP (Error Amplifier)

This is an error amplifier that takes LED control voltage and the smallest value of the LED1 to LED4 pin voltages as input. Phase compensation can be set by connecting a resistor and a capacitor to the COMP pin.

8 Soft Start

Soft start circuit for DC/DC converters. This function is used to suppress a steep increase in the inductor current at startup and an overshoot in the output voltage. Controls the change in switching Duty by limiting the rising edge of the output of Error AMP (COMP pin voltage) with the soft start function.

9 PWM COMP (PWM Comparator)

This comparator compares COMP pin voltage, which is the output of Error AMP, with SLOPE output signal. Controls the Duty of the switching pulse of DC/DC converter.

10 Additional Pulse

This circuit adds switching pulses of DC/DC converter. With the pulse addition function, the LED current can be supplied stably even when the PWM dimming ratio decreases.

11 DC/DC Control LOGIC

This circuit generates the logic of the Low side FET gate signal output from the OUTL pin.

Description of Blocks - continued

12 Pre Driver
This is the drive circuit for the Low side FET gate signal output from the OUTL pin.

13 Internal CLK
This circuit generates the internal reference clock. It is a clock of 2.3 MHz and used as a counter.

14 Dimming Control
This circuit controls the dimming rate during PWM dimming.

15 Current Driver / ISET
Current driver circuit for lighting LED. LED current can be set by connecting a resistor to the ISET pin.
In addition, the LED current can be set by the On Duty input signal of the ADIM_P pin.

16 PULSE-DC
This block smooths the pulse input to the ADIM_P pin and outputs the DC voltage to the ISET block.
The DC voltage level can be set by the pulse input Duty of the ADIM_P pin.

17 PROTECT
Outputs the status of protective operation from the FAIL pin. Since this pin is an open drain output, connect it to the REG pin with a resistor. If the status of protective operation is not monitored, turn the FAIL pin to OPEN or connect to the GND pin.

17.1 UVLO (Under Voltage Lock Out)
Under Voltage Lock Out. When VCC pin voltage is 4.10 V or less or REG pin voltage is 3.95 V or less, Under Voltage Lockout (UVLO) is activated, and the load switch (M1), DC/DC switching, and current driver turn OFF. When VCC pin voltage is 4.25 V or more and REG pin voltage is 4.10 V or more, UVLO is released and the IC restarts from Self Diagnosis. When UVLO is detected, output of the FAIL pin does not change. When the FAIL pin is pulled up to REG pin, FAIL pin voltage will also drop as REG pin voltage is decreased.

17.2 TSDLED (Thermal Shutdown for Current Driver)
This is a temperature protection circuit that monitors the vicinity of the current driver on the chip. Prevents chip temperature from rising due to output current fault. When the chip temperature rises to 175 °C or more, the temperature protection circuit (TSDLED) is activated, the load switch (M1), DC/DC switching, and current driver are turned OFF. When TSDLED is detected, the FAIL pin goes Low. When the chip temperature falls 150 °C or less, TSDLED is released, the IC restarts from Self Diagnosis.

17.3 TSDREG (Thermal Shutdown for REG)
This is a temperature protection circuit that monitors the vicinity of the REG pin on the chip. Prevents chip temperature rising due to the REG pin failure. When the chip temperature rises to 175 °C or more, the temperature protection circuit (TSDREG) is activated, and REG pin voltage, load switch (M1), DC/DC switching, and current driver turn OFF. When TSDREG is detected, the FAIL pin goes Low. When the chip temperature falls 150 °C or less, TSDREG is released and the IC restarts from Self Diagnosis.

17.4 OCPL (Over Current Protection for Low side)
The current flowing through the Low side FET (M2) is detected by the overcurrent detection resistor (R_{CSL}), and when the CSL pin voltage becomes 0.3 V or more, the overcurrent protection (OCPL) is activated and the switching of the DC/DC converter is stopped. When the CSL pin voltage drops below 0.3 V, OCPL is released and switching resumes. When OCPL is detected, the output of the FAIL pin does not change.

17.5 OVP (Over Voltage Protection)
Output overvoltage protection circuit. When OVP pin voltage (resistor division of DC/DC converter output voltage) becomes to 1.21 V or more, the overvoltage protection circuit (OVP) activates and only DC/DC switching is stopped. When OVP pin voltage falls 1.16 V or less, OVP is released. When OVP is detected, the output of the FAIL pin goes Low.

17 PROTECT – continued

17.6 OPEN Det (LED Open Detection)

LED open protection circuit. When any of LED1 to LED4 pin voltages is 0.3 V or less and OVP pin voltage is 1.21 V or more, LED open protection (OPEN Det) is activated, and the current driver is latched OFF only for the LED row that is open. OPEN Det is released when V_{EN} = Low or UVLO is detected. When OPEN Det is detected, the FAIL pin goes Low.

17.7 SHORT Det (LED Short Detection)

LED short protection circuit. When LED pin voltage is 5 V or more for 3.56 ms (counter), LED short protection (SHORT Det) is activated, and the current driver is latched OFF only for the corresponding LED row. However, the counter is reset when LED pin voltage does not satisfy the detection condition prior to SHORT Det being activated. SHORT Det is released when V_{EN} = Low or UVLO is detected. Since the 3.56 ms counter is counted up only when PWM = High, the time until SHORT Det is detected varies depending on PWM Duty. When SHORT Det is detected, the FAIL pin goes Low. SHORT Det can be detected when the PWM pulse width is 20 µs (Min) or more.

17.8 SCP (Short Circuit Protection)

Short Circuit Protection circuit. If any of the LED1 to LED4 pin voltages are 0.3 V or less or OVP pin voltage is 0.1 V or less for 3.56 ms (counter), the Short Circuit Protection (SCP) is activated, and the load switch (M1), DC/DC switching, and current driver turn OFF. However, the counter is reset when each pin voltage does not satisfy the condition prior to SCP being activated. The SCP is released when V_{EN} = Low or UVLO is detected. When SCP is detected, the FAIL pin goes Low.

17.9 OCPH (Over Current Protection for High side) / LDSW Driver

Input overcurrent protection circuit. If a condition in which the voltage between the VCC-CSH pins is 0.1 V or more continues for 10 µs or more, the input overcurrent protection (OCPH) is activated. It becomes LDSW pin voltage = VCC pin voltage and the load switch (M1), DC/DC switching, and current driver turn OFF. Then, after 56.96 ms (counter) elapses, the load switch is turned ON. At this time, if the voltage between the VCC-CSH pins is 0.1 V or more, the load switch, DC/DC switching, and current driver are turned OFF again. Also, if the voltage between the VCC-CSH pins is less than 0.1 V, Self Diagnosis is performed and restarted. When OCPH is detected, the FAIL pin goes Low.

17.10 ISET Pin Fault (ISET-GND Short Protection)

ISET pin fault protection circuit. When the resistance value connected to the ISET pin falls 3.5 kΩ or less (when ADIM_P pin voltage = REG pin voltage), ISET pin fault protection is activated, and the load switch (M1), DC/DC switching, and current driver are turned OFF. If the resistance value connected to the ISET pin is more than 3.5 kΩ (when ADIM_P pin voltage = REG pin voltage), ISET pin fault protection is released, and the load switch, DC/DC switching, and current driver are turned ON. When ISET pin fault is detected, the FAIL pin goes Low.

Description of Blocks – continued

Detect Conditions and Operation at Detection of Each Protection Function (All values in the table are Typ values)

No.	Protection Function (Block Name)	Detect Condition		Operation at Detection			
		[Detect]	[Release]	Load Switch	DC/DC Switching	Current Driver	FAIL
1	Under Voltage Lockout (UVLO)	VCC ≤ 4.10 V or V_{REG} ≤ 3.95 V	VCC ≥ 4.25 V and V_{REG} ≥ 4.10 V	OFF	OFF	OFF	High *(Note 5)*
2	Thermal Shutdown LED (TSDLED)	Tj ≥ 175 °C	Tj ≤ 150 °C	OFF	OFF	OFF	Low
3	Thermal Shutdown REG (TSDREG)	Tj ≥ 175 °C	Tj ≤ 150 °C	OFF	OFF	OFF	Low
4	Overcurrent Protection (OCPL)	V_{CSL} ≥ 0.3 V	V_{CSL} < 0.3 V	ON	OFF	ON	High *(Note 5)*
5	Overvoltage Protection (OVP)	V_{OVP} ≥ 1.21 V	V_{OVP} ≤ 1.16 V	ON	OFF	ON	Low
6	LED Open Protection (OPEN Det)	V_{LEDn}*(Note 1)* ≤ 0.3 V and V_{OVP} ≥ 1.21 V	V_{EN} = Low*(Note 6)* or Detects UVLO	ON	ON	Only detection LED pin is OFF	Latch Low
7	LED Short Protection (SHORT Det)	Detects V_{LEDn}*(Note 1)* ≥ 5.0 V for 3.56 ms or more*(Note 2)*	V_{EN} = Low*(Note 6)* or Detects UVLO	ON	ON	Only detection LED pin is OFF	Latch Low
8	Short Circuit Protection (SCP)*(Note 3)*	Detects V_{LEDn}*(Note 1)* ≤ 0.3 V or V_{OVP} ≤ 0.1 V for 3.56 ms or more	V_{EN} = Low*(Note 6)* or Detects UVLO	OFF	OFF	OFF	Latch Low
9	Input Overcurrent Protection (OCPH)*(Note 3)*	Detects voltage between the VCC-CSH pin ≥ 0.1 V for 10 µs or more	Voltage between the VCC-CSH pin < 0.1 V *(Note 4)*	OFF	OFF	OFF	Low
10	ISET-GND Short Protection (ISET Pin Fault)	ISET resistor ≤ 3.5 kΩ (when ADIM_P pin voltage = REG pin voltage)	ISET resistor > 3.5 kΩ (when ADIM_P pin voltage = REG pin voltage)	OFF	OFF	OFF	Low

(Note 1) LEDn indicates one of the LED1 to LED4 pins.
(Note 2) LED pin voltage of at least 1 channel shall be less than $V_{LEDCTL(MIN)}$ x 1.2. When LED pin voltages of all channels are 2.4 V or more, the LED short protection does not operate. Since the 3.56 ms counter is counted up only when PWM = High, the time until SHORT Det is detected varies depending on PWM Duty.
(Note 3) When Short Circuit Protection (SCP) and Input Overcurrent Protection (OCPH) are detected at the same time, the operation of Input Overcurrent Protection takes precedence.
(Note 4) When 56.96 ms elapses after the load switch is turned OFF, the load switch turns ON. At this time, when the voltage between the VCC-CSH pins ≥ 0.1 V, the load switch, DC/DC switching, and current driver are turned OFF again. Also, when the voltage between the VCC-CSH pins < 0.1 V, Self Diagnosis is performed and restarted.
(Note 5) When pulled up to any voltage, it becomes High output.
(Note 6) The Low width of EN pin need 10 µs or more.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VCC, LDSW, CSH Pin Voltage	VCC, V_{LDSW}, V_{CSH}	-0.3 to +50.0	V
Voltage Between VCC-LDSW, VCC-CSH Pins	VCC-V_{LDSW}, VCC-V_{CSH}	-0.3 to +7.0	V
LED1, LED2, LED3, LED4, OVP Pin Voltage	V_{LED1}, V_{LED2}, V_{LED3}, V_{LED4}, V_{OVP}	-0.3 to +50.0	V
RT, COMP, ISET, PLSET, OUTL, CSL Pin Voltage	V_{RT}, V_{COMP}, V_{ISET}, V_{PLSET}, V_{OUTL}, V_{CSL}	-0.3 to V_{REG}	V
EN, REG, SYNC, PWM, ADIM_P, FAIL Pin Voltage	V_{EN}, V_{REG}, V_{SYNC}, V_{PWM}, V_{ADIM_P}, V_{FAIL}	-0.3 to +7.0	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	96.0	34.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	12.0	9.0	°C/W
VQFN24FV4040				
Junction to Ambient	θ_{JA}	116.5	36.2	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	15	8	°C/W

(Note 1) Based on JESD51-2A (Still-Air). The BD83A14EFV-M chip and the BD83A14MUF-M chip are used.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Operating Range		Unit
		Min	Max	
Power Supply Voltage *(Note 1)*	VCC	4.5	48.0	V
DC/DC Oscillation Frequency Range (SSCG = OFF)	f_{OSC}	200	2420	kHz
PWM Frequency Range *(Note 2)*	f_{PWM}	0.1	25.0	kHz
ADIM_P pin Input Frequency Range *(Note 3)*	f_{ADIM_P}	40	400	kHz
ADIM_P pin Input On Duty Range *(Note 3)*	D_{ADIM_P}	18	100	%
External Synchronized Frequency Range *(Note 4)*	f_{SYNC}	Higher of 200 or f_{OSC} x 0.9	Lower of 700 or f_{OSC} x 1.1	kHz
External Synchronized Pulse Duty Range *(Note 5)*	D_{SYNC}	40	60	%
LED Current Setting Range *(Note 6)*	I_{LED}	20	150	mA
Operating Temperature	Topr	-40	+125	°C

(Note 1) When IC is started, the voltage must be UVLO release voltage or more. Therefore, consider the power supply drop caused by the parasitic resistor and start the IC at VCC ≥ 5.5 V.
VCC(Min) = 4.5 V is the minimum value of VCC that can operate the IC alone. The minimum value of power supply voltage that can be set depends on the connected LED load and external components.
(Note 2) Generally, flickering of LEDs is easier to see when the dimming frequency is set lower than 100 Hz. Set after confirming with the actual device evaluation.
(Note 3) If you input a frequency outside the operating range to the ADIM_P pin, the LED flicker will be more visible. Set after confirming with the actual device evaluation.
(Note 4) When the external synchronization function is not used, connect the SYNC pin to V_{REG} (SSCG = ON) or GND (SSCG = OFF).
(Note 5) When using the external synchronization function, switching from the external synchronization state to the internal oscillation frequency is not possible during stable operation.
(Note 6) The amount of current per channel that can be set by the resistor (R_{ISET}) connected to the ISET pin (D_{ADIM_P} = 100 %). Set the LED current so that the maximum junction temperature (Tjmax) is not exceeded.

Operating Conditions (External Constant Range)

Parameter	Symbol	Operating Range			Unit
		Min	Typ	Max	
REG Capacitance	C_{REG}	1.0 *(Note 7)*	2.2	4.7	µF
Resistor for LED Current Setting	R_{ISET}	8.8	-	53.0	kΩ
Resistor for Oscillation Frequency Setting	R_{RT}	4	-	45	kΩ
PLSET Capacitance	C_{PLSET}	-	-	10	nF
Input Capacitance 1	C_{VCC}	1 *(Note 7)*	-	-	µF
Input Capacitance 2	C_{INVCC} *(Note 8)*	10 *(Note 7)*	-	-	µF
Output Capacitance	C_{OUT}	20 *(Note 7)*	-	100	µF

(Note 7) Set the capacitance so that it does not fall below the minimum value in consideration of temperature characteristics, DC bias characteristics, etc.
(Note 8) C_{INVCC} means the total capacitance of C_{IN} and C_{VCC}.

Electrical Characteristics

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	-	10	mA	V_{EN} = 5 V, V_{SYNC} = 0 V, V_{PWM} = 0 V, C_{IN} = 10 µF, RT = OPEN, ISET = OPEN, V_{ADIM_P} = V_{REG}, Resistance between LEDn-GND = 10 kΩ
Standby Current	I_{ST}	-	0	10	µA	V_{EN} = Low
[VREF]						
REG Output Voltage	V_{REG}	4.7	5.0	5.3	V	I_{REG} = -5 mA, C_{REG} = 2.2 µF
[DC/DC Converter]						
OUTL Pin ON Resistor (High side)	R_{ONLH}	1.5	3.0	6.0	Ω	I_{OUTL} = -10 mA
OUTL Pin ON Resistor (Low side)	R_{ONLL}	1.0	2.0	4.0	Ω	I_{OUTL} = 10 mA
LED Control Voltage	V_{LEDCTL}	0.84	1.03	1.22	V	R_{ISET} = 8.8 kΩ, V_{ADIM_P} = V_{REG}
COMP Sink Current	$I_{COMPSINK}$	150	220	290	µA	R_{ISET} = 15.1 kΩ, V_{COMP} = 1.0 V, V_{LED} = 1.5 V, V_{ADIM_P} = V_{REG}
COMP Source Current	$I_{COMPSOURCE}$	-290	-220	-150	µA	R_{ISET} = 15.1 kΩ, V_{COMP} = 1.0 V, V_{LED} = 0 V, V_{ADIM_P} = V_{REG}
Oscillation Frequency 1	f_{OSC1}	270	300	330	kHz	R_{RT} = 33.3 kΩ
Max Duty 1	D_{UTY_MAX1}	95	-	-	%	R_{RT} = 33.3 kΩ
Oscillation Frequency 2	f_{OSC2}	1980	2200	2420	kHz	R_{RT} = 4 kΩ
PLSET Charge Current	I_{PLSET}	35	50	65	µA	V_{PLSET} = 0 V
PLSET Set Voltage	V_{PLSET}	0.4	0.5	0.6	V	

Electrical Characteristics – continued

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[Current Driver]						
LED Current Absolute Variation	I_{LEDn}	76.1	80.1	84.1	mA	R_{ISET} = 15.1 kΩ, $V_{ADIM\_P} = V_{REG}$
LED Current Relative Variation *(Note 1)*	I_{LEDREL}	0	-	5	%	R_{ISET} = 15.1 kΩ, $V_{ADIM\_P} = V_{REG}$
ISET-GND Short Protection Resistor	$R_{ISETLIM}$	-	3.5	-	kΩ	$V_{ADIM\_P} = V_{REG}$
PWM Dimming Minimum Pulse Width	t_{PWMMIN}	0.5	-	-	µs	f_{PWM} = 100 Hz to 25 kHz, I_{LED} = 80.1 mA
PWM Dimming Frequency	f_{PWM}	0.1	-	25.0	kHz	
PWM Low Section Detect Time	t_{PWML}	21.4	28.5	35.6	ms	
[Logic Input (EN)]						
Input High Voltage	V_{INH1}	2.1	-	-	V	
Input Low Voltage	V_{INL1}	-	-	0.5	V	
Input Resistor	R_{IN1}	50	100	150	kΩ	V_{EN} = 5 V
[Logic Input (PWM, SYNC, ADIM_P)]						
Input High Voltage	V_{INH2}	2.1	-	-	V	
Input Low Voltage	V_{INL2}	-	-	0.5	V	
Input Resistor	R_{IN2}	50	100	150	kΩ	$V_{PWM} = V_{SYNC} = V_{ADIM\_P}$ = 5 V

(Note 1) $I_{LEDREL} = (I_{LEDn(MAX)} - I_{LEDn(MIN)}) / I_{LEDn(AVE)} \times 100$

Electrical Characteristics – continued

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[PROTECT]						
VCCUVLO Detect Voltage	$V_{UVLOVCC1}$	3.90	4.10	4.30	V	VCC = Sweep down
VCCUVLO Release Voltage	$V_{UVLOVCC2}$	4.05	4.25	4.45	V	VCC = Sweep up
REGUVLO Detect Voltage	$V_{UVLOREG1}$	3.75	3.95	4.15	V	V_{REG} = Sweep down
REGUVLO Release Voltage	$V_{UVLOREG2}$	3.90	4.10	4.30	V	V_{REG} = Sweep up
OVP Detect Voltage	V_{OVPDET}	1.173	1.210	1.247	V	V_{OVP} = Sweep up
OVP Detect Voltage Hysteresis Width	V_{OVPHYS}	-	50	-	mV	V_{OVP} = Sweep down
Input OCP Detect Voltage	V_{OCPH}	80	100	120	mV	VCC-V_{CSH} = Sweep up
LDSW Operation Voltage at Input OCP Release	V_{LDSW}	4.4	5.4	6.4	V	V_{CSH} = VCC VCC-V_{LDSW}
CSH Pin Input Current	I_{CSH}	-0.8	0.0	+0.8	μA	V_{CSH} = 12 V
OCPL Detect Voltage	V_{OCPL}	0.27	0.30	0.33	V	V_{CSL} = Sweep Up
LED Open Protection Detect Voltage	V_{OPEN}	0.25	0.30	0.35	V	V_{LED} = Sweep down $V_{OVP} \geq V_{OVPDET}$
LED Anode SCP Detect Voltage	V_{SCP1}	0.05	0.10	0.15	V	V_{OVP} = Sweep down
LED Cathode SCP Detect Voltage	V_{SCP2}	0.25	0.30	0.35	V	V_{LED} = Sweep down
LED Anode SCP Detect Delay Time	t_{SCP1}	2.67	3.56	4.45	ms	
LED Cathode SCP Detect Delay Time	t_{SCP2}	2.67	3.56	4.45	ms	
LED Short Protection Detect Voltage	V_{SHORT}	4.7	5.0	5.3	V	V_{LED} = Sweep up
Initial Check Time	t_{INICK}	5.34	7.12	8.90	ms	
FAIL Pin ON Resistor	R_{FAIL}	-	1.0	2.0	kΩ	I_{FAIL} = 1 mA

Typical Performance Curves

(Reference data, unless otherwise specified VCC = 12 V)

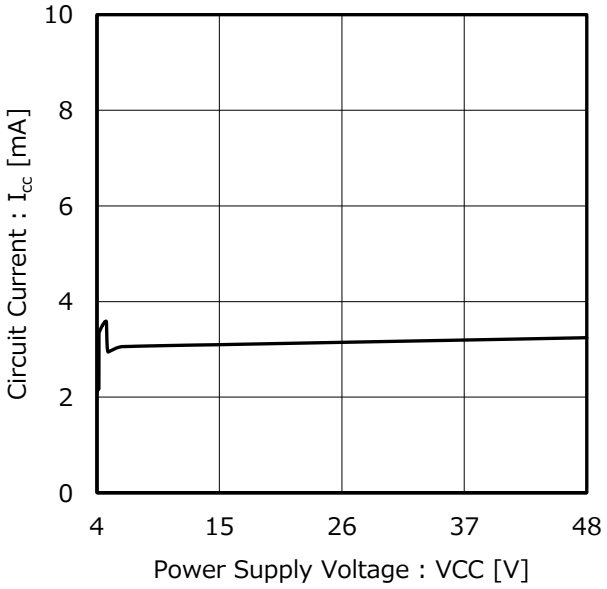


Figure 3. Circuit Current vs Power Supply Voltage

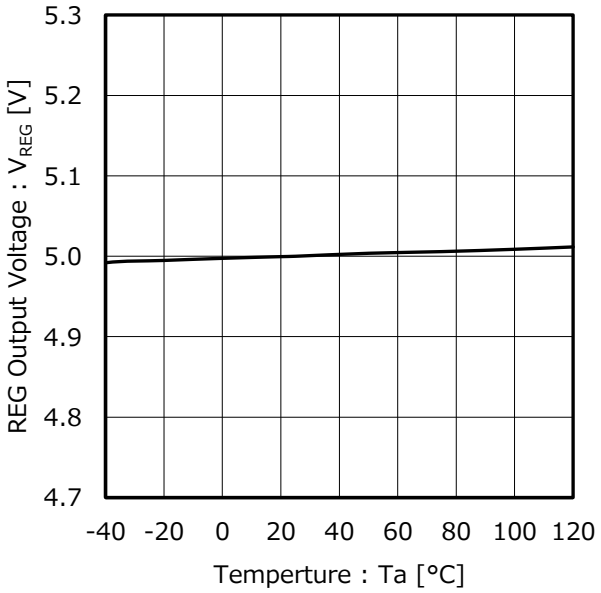


Figure 4. REG Output Voltage vs Temperature

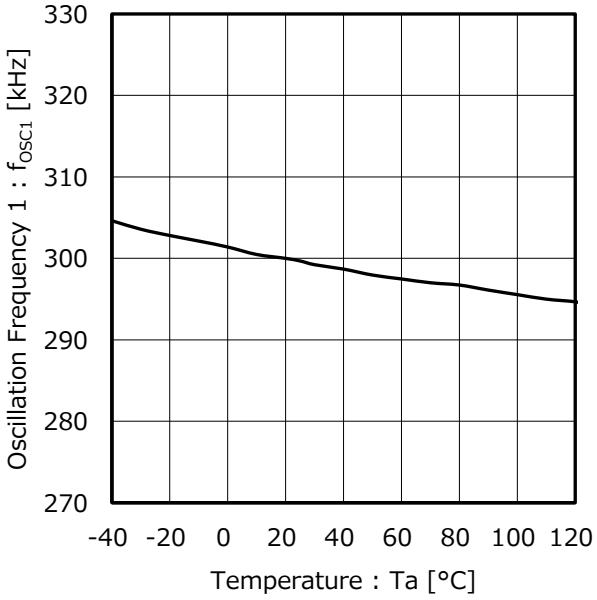


Figure 5. Oscillation Frequency 1 vs Temperature
(R_{RT} = 33.3 kΩ)

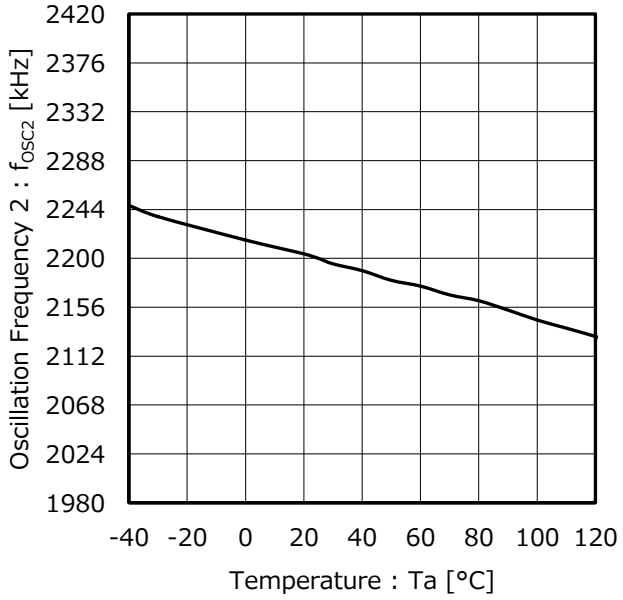


Figure 6. Oscillation Frequency 2 vs Temperature
(R_{RT} = 4 kΩ)

Typical Performance Curves – continued
(Reference Data)

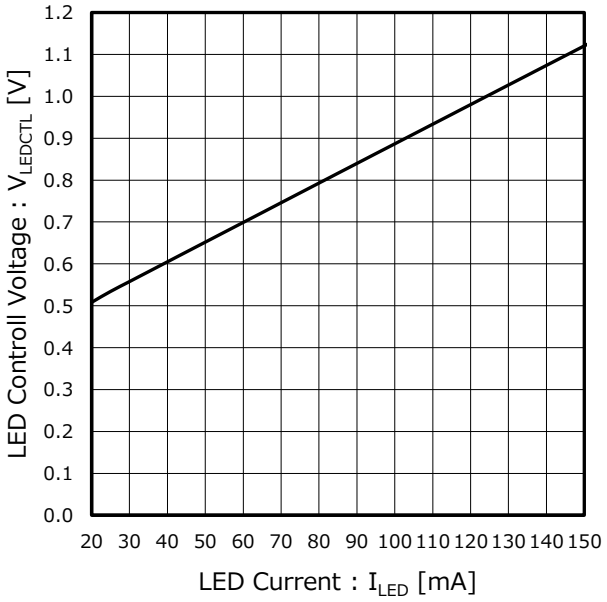


Figure 7. LED Control Voltage vs LED Current

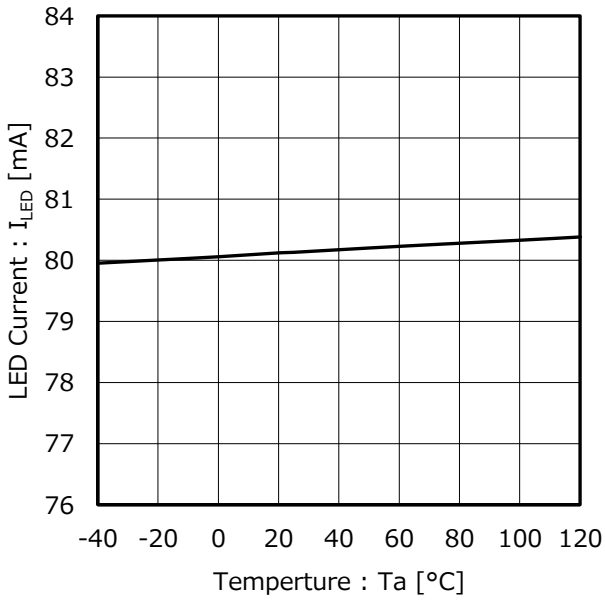


Figure 8. LED Current vs Temperature

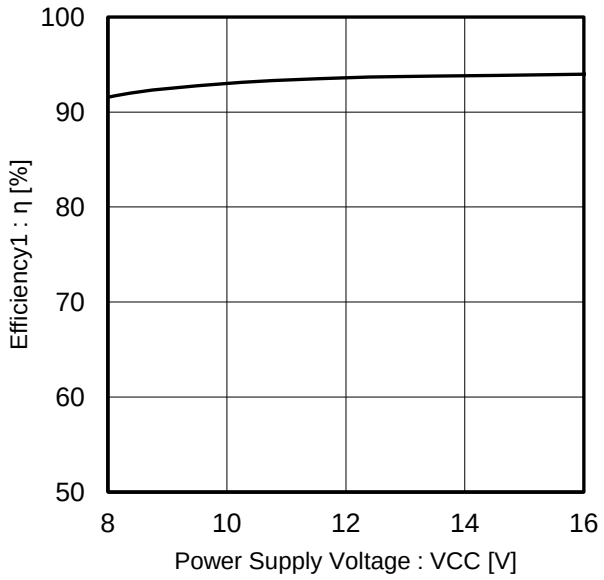


Figure 9. Efficiency 1 vs Power Supply Voltage
(R_{RT} = 33.3 kΩ, R_{ISET} = 15.1 kΩ,
Number of LED Series = 10, Number of LED Parallels = 4)

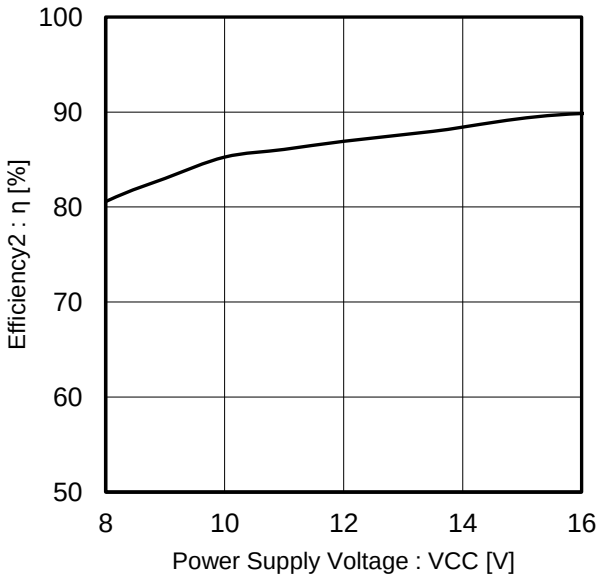


Figure 10. Efficiency 2 vs Power Supply Voltage
(R_{RT} = 4 kΩ, R_{ISET} = 15.1 kΩ,
Number of LED Series = 10, Number of LED Parallels = 4)

Function Descriptions

Unless otherwise stated, the value in the sentence is the Typ value.

1 Current Driver

This model has a built-in 4 ch current driver. The LED current setting range per channel is 20 mA to 150 mA, and the LED current can be adjusted by the resistance value between the ISET pin and GND.

1.1 How to Set LED Current

The LED current I_{LED} can be calculated using the following equation.

$$I_{LED} = \frac{V_{ISET}}{R_{ISET}} \times \frac{10}{9} \times 10^6 \quad [\text{mA}]$$

I_{LED}: Output current per channel (LED current)
(Recommended operating condition: 20 mA to 150 mA)
V_{ISET}: ISET pin voltage 1.089 V
(When ADIM_P pin voltage $V_{ADIM\_P} = V_{REG}$)
R_{ISET}: Resistor for LED current setting
(Recommended operating condition: 8.8 kΩ to 53 kΩ)

Resistance Value Setting Example ($V_{ADIM\_P} = V_{REG}$)

ISET Resistor [kΩ]	LED Current [mA]
53.0	22.8
30.0	40.3
15.1	80.1
8.8	137.5

When $R_{ISET} \leq 3.5$ kΩ, ISET pin short protection detect is activated and, output of the LED current is stopped.

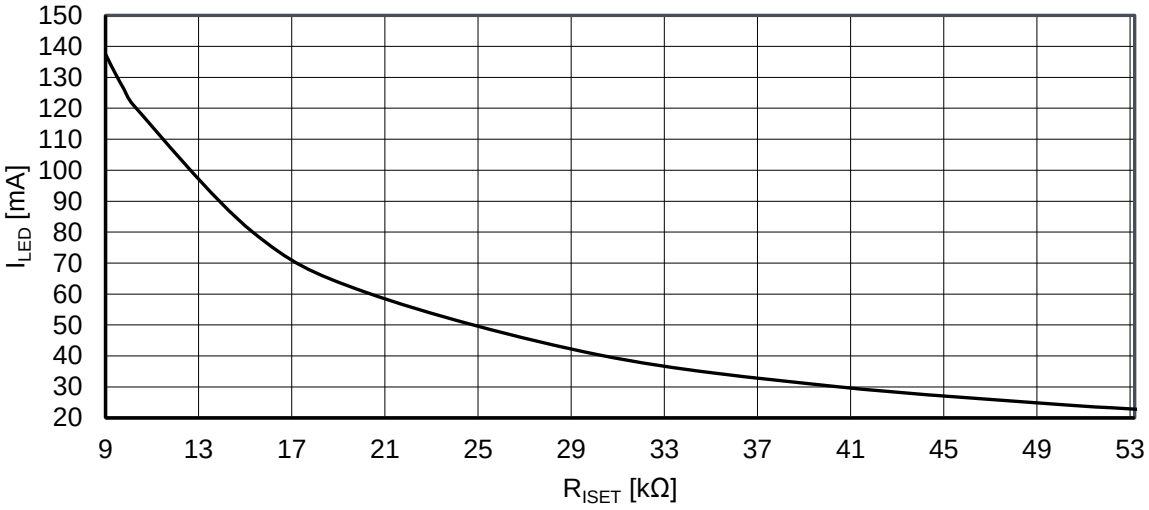


Figure 11. I_{LED} vs R_{ISET} ($V_{ADIM\_P} = V_{REG}$)

1 Current Driver – continued

1.2 When Using Analog Dimming

ISET pin voltage can be adjusted according to the input Duty to the ADIM_P pin. The LED current I_{LED} can be calculated from the following equation as described above.

$$I_{LED} = \frac{V_{ISET}}{R_{ISET}} \times \frac{10}{9} \times 10^6 \quad [\text{mA}]$$

However, V_{ISET} can be adjusted according to ADIM_P pin input On Duty D_{ADIM_P} as follows:

$V_{ISET} = 1.089$ [V]
(90 % ≤ D_{ADIM_P} ≤ 100 %)

$V_{ISET} = 1.089 \times \frac{10}{9} \times D_{ADIM\_P}$ [V]
(18 % < D_{ADIM_P} < 90 %)

I_{LED}: Output current per channel (LED current)
(Recommended operating condition: 20 mA to 150 mA)
R_{ISET}: Resistor for LED current setting
(Recommended operating condition: 8.8 kΩ to 53 kΩ)
D_{ADIM_P}: ADIM_P pin input On Duty
(Recommended operating condition: 18 % to 100 %)

Note : Note that the LED current set by R_{ISET} and the ADIM_P pin cannot be set less than 10 mA

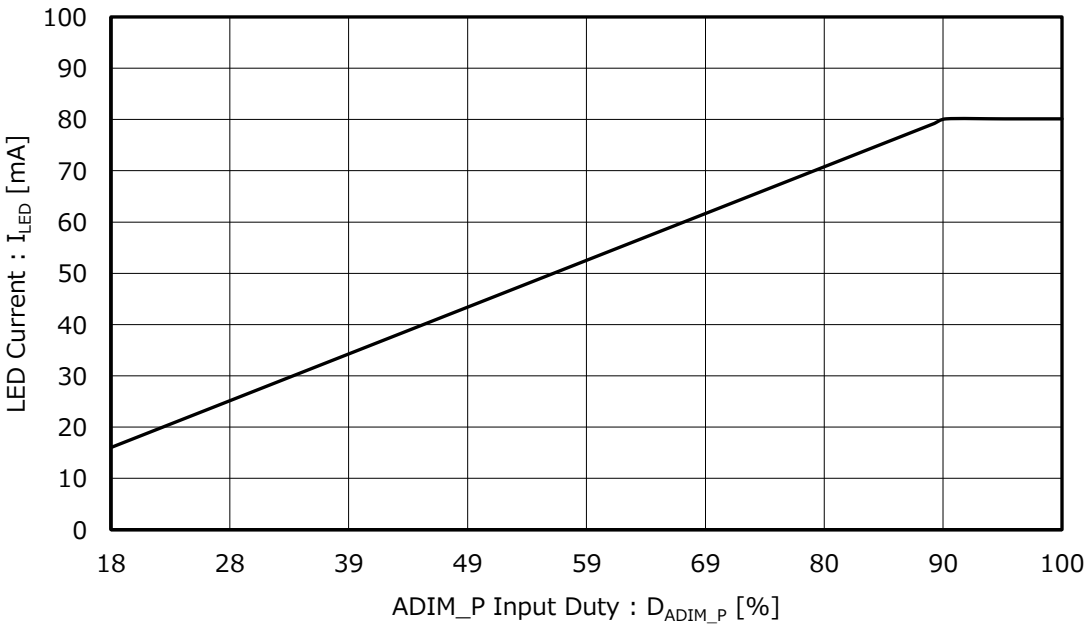


Figure 12. I_{LED} vs D_{ADIM_P} (R_{ISET} = 15.1 kΩ)

1.3 When Using PWM Dimming

The LED current can be controlled according to On Duty of the PWM signal input to the PWM pin. However, in the region where the ON time of the LED current is less than 0.5 µs or the OFF time is less than 0.5 µs, the pulse time is shorter than PWM dimming minimum pulse width, so it cannot be used regularly. It is okay to use this region transiently, so it is also possible to set PWM Duty = 0 % and 100 %.

1 Current Driver – continued

1.4 PWM Low Section Detect Function

Counting starts when PWM = High is switched to Low in the V_{EN} = High state. When PWM Low section reaches 28.5 ms, the operation is regarded as OFF state. After that, when PWM input is turned High, switching operation (pre-boost) is restarted.

1.5 LED Pin Handling of Unused Channels

This model has four built-in constant current circuits. The current can be supplied to the LED by setting the PWM pin to High, and the LED current can be set by inserting a resistor between the ISET pin and GND. The LED current that can be supplied per row is 20 mA to 150 mA.
Pull down the LED pin of the unused channel to GND with 10 kΩ.

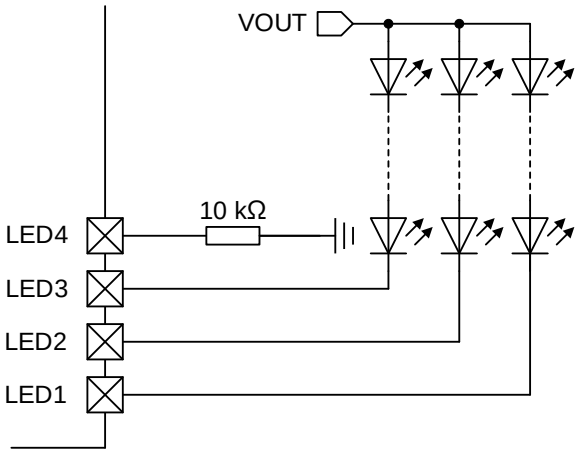


Figure 13. When Setting LED4 Unused

1.6 When Setting the LED Current Above 150 mA

The LED1 to LED4 pins can be used in bundles.
For example, as shown in the figure on the right, if LED1, LED2, LED3, and LED4 are shorted, 4 times the current set by the ISET pin can be passed.
When using only 2 channels in a bundle, mount the pulled-down resistor for each LED pin for unused channels (2 channels).
When connected to multiple LED pins with a resistor, the voltage value may be out of the set range and may not be recognized as an unused channel. In this case, the unintentional protection function may be activated, so perform the LED pin handling correctly.

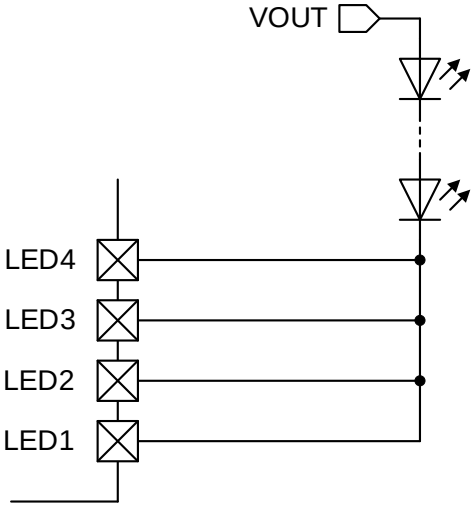


Figure 14. Application Example When LED Pins are Shorted

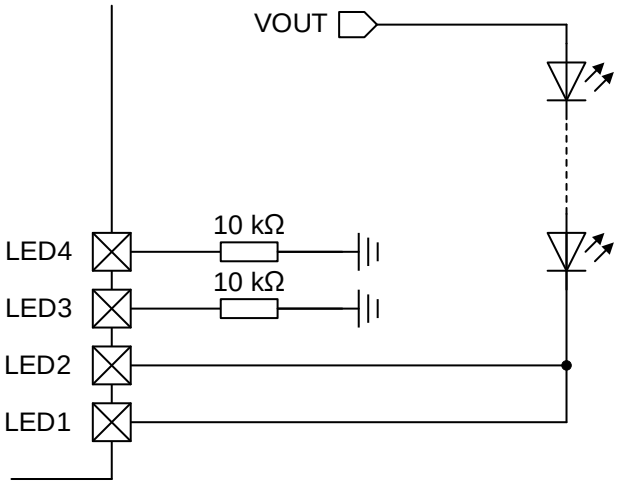


Figure 15. Correct LED Pin Handling When Multiple Channels are Unused

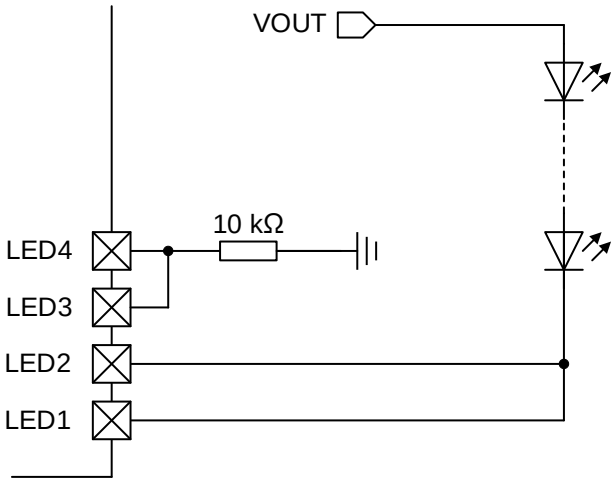


Figure 16. Wrong LED Pin Handling When Multiple Channels are Unused

Function Descriptions – continued

Unless otherwise stated, the value in the sentence is the Typ value.

2 DC/DC Converter

Detects the lowest voltage among LED1 to LED4 pin voltages (LED cathode voltages) in Minimum Channel Selector block and inputs it to Error AMP. The reference voltage of Error AMP is generated in REF Voltage block based on R_{ISET} resistance value, which becomes LED pin control voltage. The output of Error AMP is compared with the output of SLOPE block by PWM COMP block, and a switching signal is output to the OUTL pin through DC/DC Control LOGIC.

2.1 LED Control Voltage V_{LEDCTL}

DC/DC converter operates so that the lowest voltage among LED1 to LED4 pin voltages (LED cathode voltages) is equal to the LED control voltage (V_{LEDCTL}). Power dissipation can be minimized by optimizing the LED control voltage (V_{LEDCTL}) according to the LED current (I_{LED}).

LED Control Voltage Reference Value ($V_{ADIM\_P} = V_{REG}$)

ISET Resistor R_{ISET} [kΩ]	LED Current I_{LED} [mA]	LED Control Voltage V_{LEDCTL} [V]
53.0	22.8	0.53
20.5	59.0	0.69
15.1	80.1	0.78
8.8	137.5	1.03

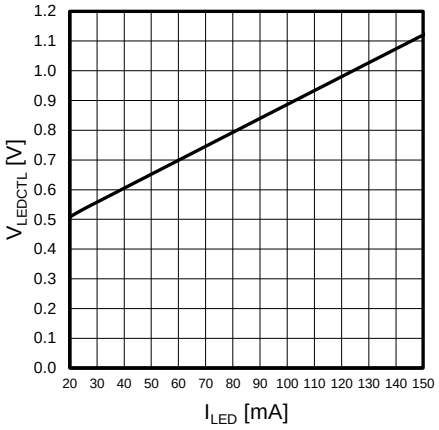


Figure 17. V_{LEDCTL} vs I_{LED}

2.2 VCC Input Voltage and Number of LED Series

To drive the boost DC/DC converter, the LED must be selected so that the output voltage (VOUT) is higher than the input voltage (VCC).

$$VCC_{(MAX)} < VOUT_{(MIN)}$$

$$VCC_{(MAX)} < Vf_{(MIN)} \times N + V_{LEDCTL(MIN)}$$

Select the number of LED series and Vf characteristics that satisfy the above equation.

VCC : Input voltage
$VOUT$: DC/DC converter output voltage
N : Number of LED series
Vf : LED Vf voltage
V_{LEDCTL} : LED control voltage

2.3 LED Variation and Series Number

When operating multiple LED outputs, the LED anode voltages in each row are commonly connected to DC/DC converter output VOUT. LED pin voltage (LED cathode voltage) in the row where the Vf voltage of the LED is the highest is the lowest, and this is controlled to be V_{LEDCTL}. Therefore, the voltage of other LED pin outputs will be higher by the amount of Vf variation. Select the number of LED series and Vf characteristics so that the LED short protection ($V_{LEDn} \geq 5.0$ V) does not operate.

$$N \times \left(Vf_{(MAX)} - Vf_{(MIN)}\right) < V_{SHORT(MIN)} - V_{LEDCTL(MAX)}$$

V_{SHORT} : LED short protection voltage

2 DC/DC Converter – continued

2.4 Overvoltage Protection Function OVP

Inputs the resistor division of the output voltage VOUT in the OVP pin. When OVP pin voltage rises the overvoltage protection detect voltage V_{OVP} (1.21 V) or more, the overvoltage protection is activated, and the switching of DC/DC converter is turned OFF. After that when OVP pin voltage drops to 1.16 V, OVP is released.

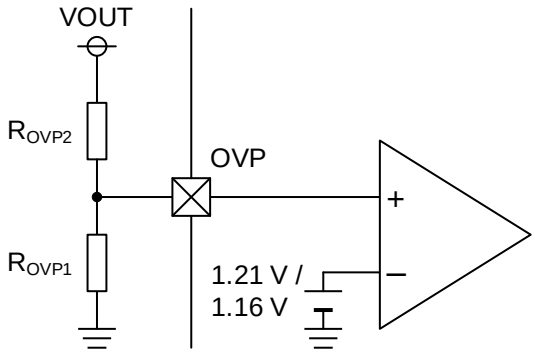


Figure 18. OVP Pin Voltage Setting Sample

$$VOUT_{OVP} = \{(R_{OVP1} + R_{OVP2}) \,/\, R_{OVP1}\} \times V_{OVP} \quad [V]$$

$VOUT_{OVP}$: DC/DC converter output voltage (VOUT) during overvoltage protection operation
V_{OVP} : Overvoltage protection detect voltage

2.5 DC/DC Converter Oscillator Frequency f_{osc}

The oscillation frequency (f_{OSC}) of DC/DC converter can be set by connecting R_{RT} between the RT pin and GND. The oscillator frequency of DC/DC converter is generated in the OSC block. Set the resistor of R_{RT} referring to the data and theoretical formula below.

$$f_{OSC} = (10^7 \,/\, R_{RT}) \times \alpha \quad [kHz]$$

f_{OSC} : Oscillation frequency of DC/DC converter
10^7 : Constants determined inside the circuit
R_{RT} : RT pin connecting resistor
α : Correction factor

α is the correction factor. For the relation between f_{OSC} and R_{RT} including the correction factor, refer to f_{OSC} vs R_{RT} below. Note that operation cannot be guaranteed if f_{OSC} setting value exceeds the recommended range of 200 kHz to 2420 kHz. Determine f_{OSC} setting value in consideration of the variation in electrical characteristics, variation in R_{RT}, and ON/OFF of spread spectrum

Example of Resistance Value for f_{OSC} Setting

R_{RT} [kΩ]	α
45.0	1.006
33.3	1.000
20.8	0.987
20.0	0.986
10.0	0.957
4.0	0.882

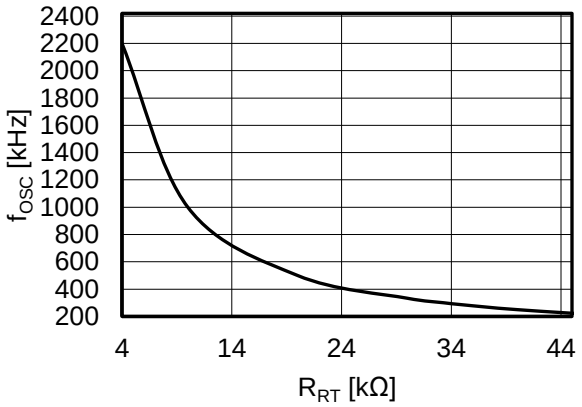


Figure 19. f_{OSC} vs R_{RT}

2 DC/DC Converter – continued

2.6 Pulse Addition Function

A pulse addition function is provided to output a stable DC/DC converter output voltage and LED current even when PWM Duty is low. The output voltage can be held by outputting additional switching of several pulses after the falling edge of the PWM input signal, and the LED can be turned on normally. When the pulse addition function is not used, set the PLSET pin to OPEN

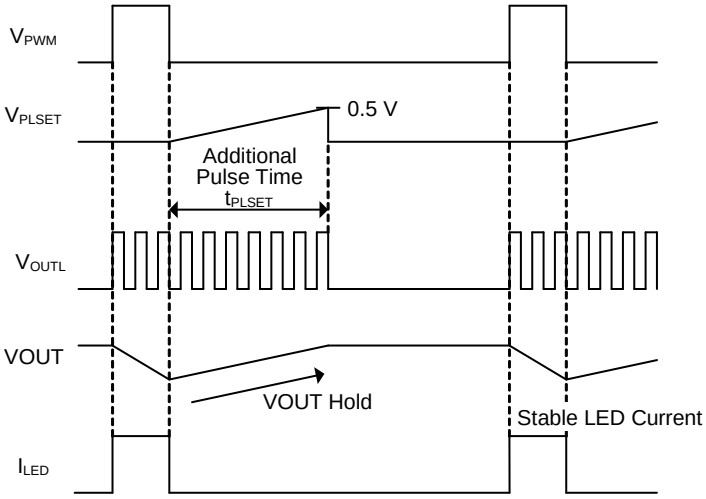


Figure 20. Pulse Addition Function

The number of additional switching pulses is set in the capacitance value C_{PLSET} connected to the PLSET pin. The additional pulse time t_{PLSET} is calculated as follows:

$$t_{PLSET} = 10^{10} \times C_{PLSET} \quad [\mu s]$$

t_{PLSET} : Additional pulse time
C_{PLSET} : PLSET pin capacitance

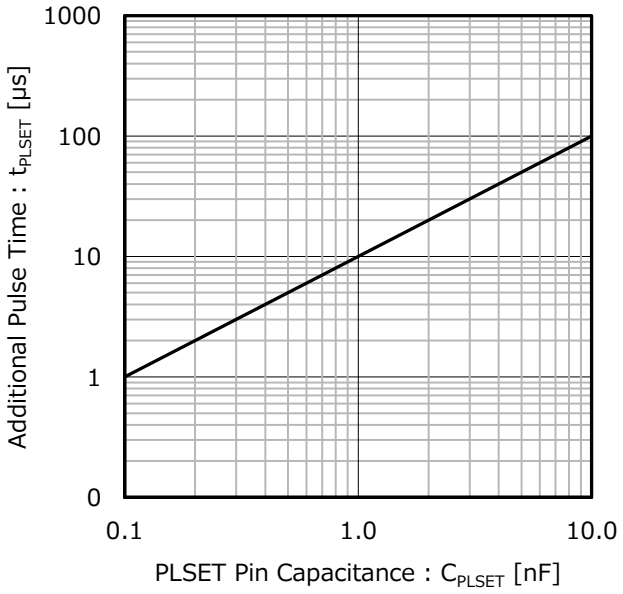


Figure 21. t_{PLSET} vs C_{PLSET}

The additional pulse time required to hold the output voltage VOUT varies depending on various factors such as PWM frequency, output voltage, output capacitance, LED current, as well as the minimum value of PWM Duty used for dimming. Contact your sales representative when you request design verification of the required additional pulse time for your usage conditions.

2 DC/DC Converter – continued

2.7 External Synchronization / Spread Spectrum Function (SSCG)

Three switching modes can be selected according to the voltage input to the SYNC pin.

Mode	V_{SYNC}	DC/DC Switching Frequency
1	Low	Fixed Frequency Mode Determined by R_{RT}
2	High (= V_{REG})	Spread Spectrum Mode of the Frequency Determined by R_{RT}
3	Pulse Input	Mode to Synchronize with the Frequency Input to the SYNC Pin

Mode 1:
When the SYNC pin is fixed Low, DC/DC converter switches at a fixed frequency determined by R_{RT}.

Mode 2:
By shorting the SYNC pin and the REG pin, operation in spread spectrum mode (SSCG) is enabled. With SSCG, noise peaks can be reduced by periodically changing the oscillation frequency. The fluctuation range (Δf) of the frequency due to SSCG is -8 % of the set oscillation frequency from the set oscillation frequency. The oscillation frequency fluctuation period is 2.3 kHz.

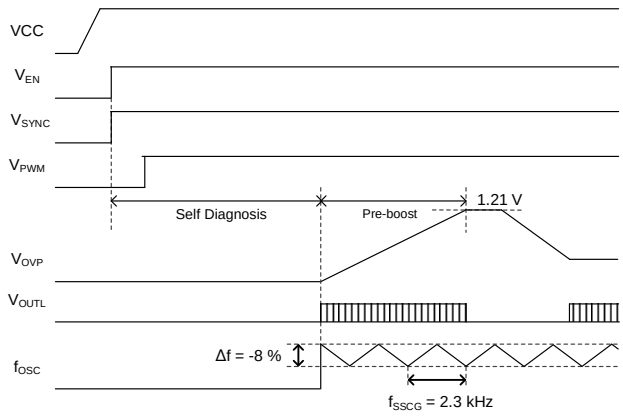


Figure 22. Spread Spectrum Function Timing Chart

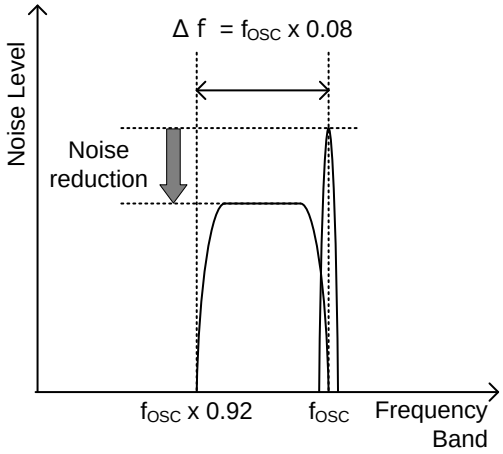


Figure 23. Spread Spectrum Function

$$\Delta f = f_{osc} \times 0.08$$

$$f_{SSCG} = 2.3 \quad [\text{kHz}]$$

Δf : Fluctuation range of the oscillation frequency by SSCG
f_{osc} : DC/DC oscillation frequency
f_{SSCG} : The oscillation frequency fluctuation period by SSCG

When not using SSCG function, short the SYNC pin and the GND pin.
SSCG function cannot be turned ON/OFF during operation.

2.7 External Synchronization / Spread Spectrum Function (SSCG) – continued

Mode 3:

By inputting an external clock signal to the SYNC pin, the internal oscillation frequency can be externally synchronized. However, note the following points.

- ·Since Mode is judged during Self Diagnosis (Initial Check), input the clock signal to the SYNC pin prior to turning the EN pin to High.
- ·After the clock signal is input to the SYNC pin and the EN pin is turned High, it is not possible to switch between internal oscillation and external synchronization. Operation may become unstable. After setting to Mode 3, it is possible to change the external synchronization frequency during operation. However, evaluate the LED flickering due to fluctuations of the output voltage.
- ·When using external synchronization, SSCG cannot be used.
- ·For the external synchronization frequency, input a frequency within ±10 % of the theoretical value of the DC/DC oscillation frequency f_{OSC} set by the RT pin.

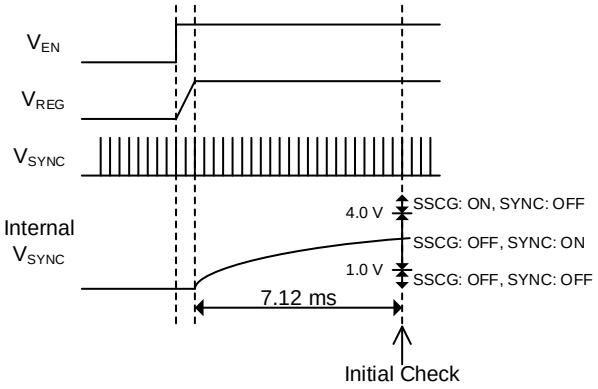


Figure 24. Synchronous Signal (V_{SYNC}) Input and Mode Check (Initial Check) Timing

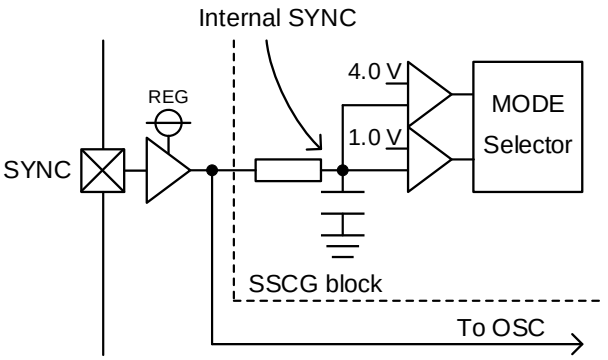


Figure 25. SYNC Pin Equivalence Circuit

2.8 LSDET Function

When the lowest LED pin voltage among LED pins is 2.4 V or more, DC/DC converter is turned OFF, and COMP pin voltage is held. DC/DC converter resumes switching when the lowest LED pin voltage is less than V_{LEDCTL} x 1.2.

LSDET function is intended to reduce the voltage quickly when the output is over boosted. It also prevents the LEDs from flickering by resuming the switching of DC/DC converter just before returning to normal operation.

① The LED4 pin becomes open and LED4 pin voltage becomes 0.3 V or less (Ⓐ).
DC/DC converter output begins boosting further to raise LED4 pin voltage. In conjunction with this, OVP pin voltage also rises (Ⓑ).

② When OVP pin voltage reaches 1.21 V (Ⓒ) due to the boost of DC/DC converter, the LED open protection is activated.
When the LED open protection is activated, the LED4 pin that was open is pulled up to REG pin voltage V_{REG} inside the IC (Ⓓ).
LSDET function operates because LED4 pin voltage, which is the lowest LED pin voltage in the LED pins, is 2.4 V or more (Ⓓ).
LSDET function turns OFF DC/DC converters and holds COMP pin voltage (Ⓔ).

③ DC/DC converter turns OFF, the output voltage drops, and OVP pin voltage also drops (Ⓕ).

④ When the lowest LED pin voltage is less than V_{LEDCTL} x 1.2 (Ⓖ), DC/DC converter resumes switching (Ⓗ).

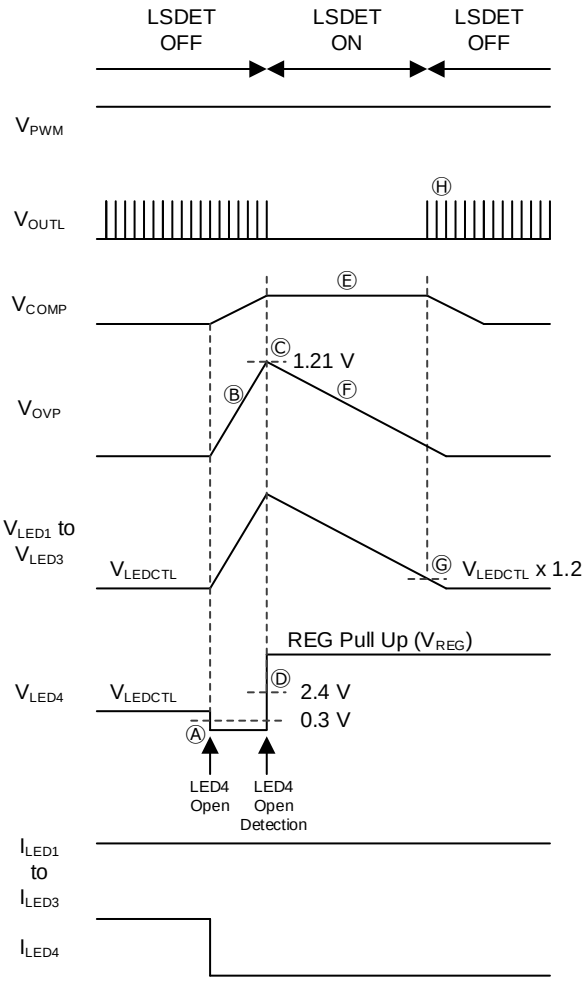


Figure 26. LSDET Function When LEDs are Open

Function Descriptions – continued

Unless otherwise stated, the value in the sentence is the Typ value.

3 Starting Sequence and Effective Section of Each Protection Function

The timing chart at startup and the effective section of each protection function are shown in the figure below.

① Power ON : Input EN pin voltage after the VCC pin voltage is input.
Input the ADIM_P pin voltage at the same time as the EN pin voltage at the latest after inputting the VCC pin voltage.

② Self Diagnosis (Initial check) : After inputting EN pin voltage, this IC becomes the Self Diagnosis status, determines the channel to be used, and sets the external synchronization / spread spectrum function, etc. Self Diagnosis is completed after 7.12 ms, and the diagnostic status is latched.

③ Pre-boost : After Self Diagnosis, pre-boost starts at V_{PWM} = High, and after 7.12 ms, pre-boost is completed.

④ Stable operation : The LED current flows according to On Duty of the PWM signal input to the PWM pin. The output transition section voltage of DC/DC converter with switching turned OFF drops according to the load current.

⑤ Stable state : When LED pin voltage (the lowest voltage in LED1 to LED4) drops to LED control voltage x 1.2, DC/DC converter switches again.

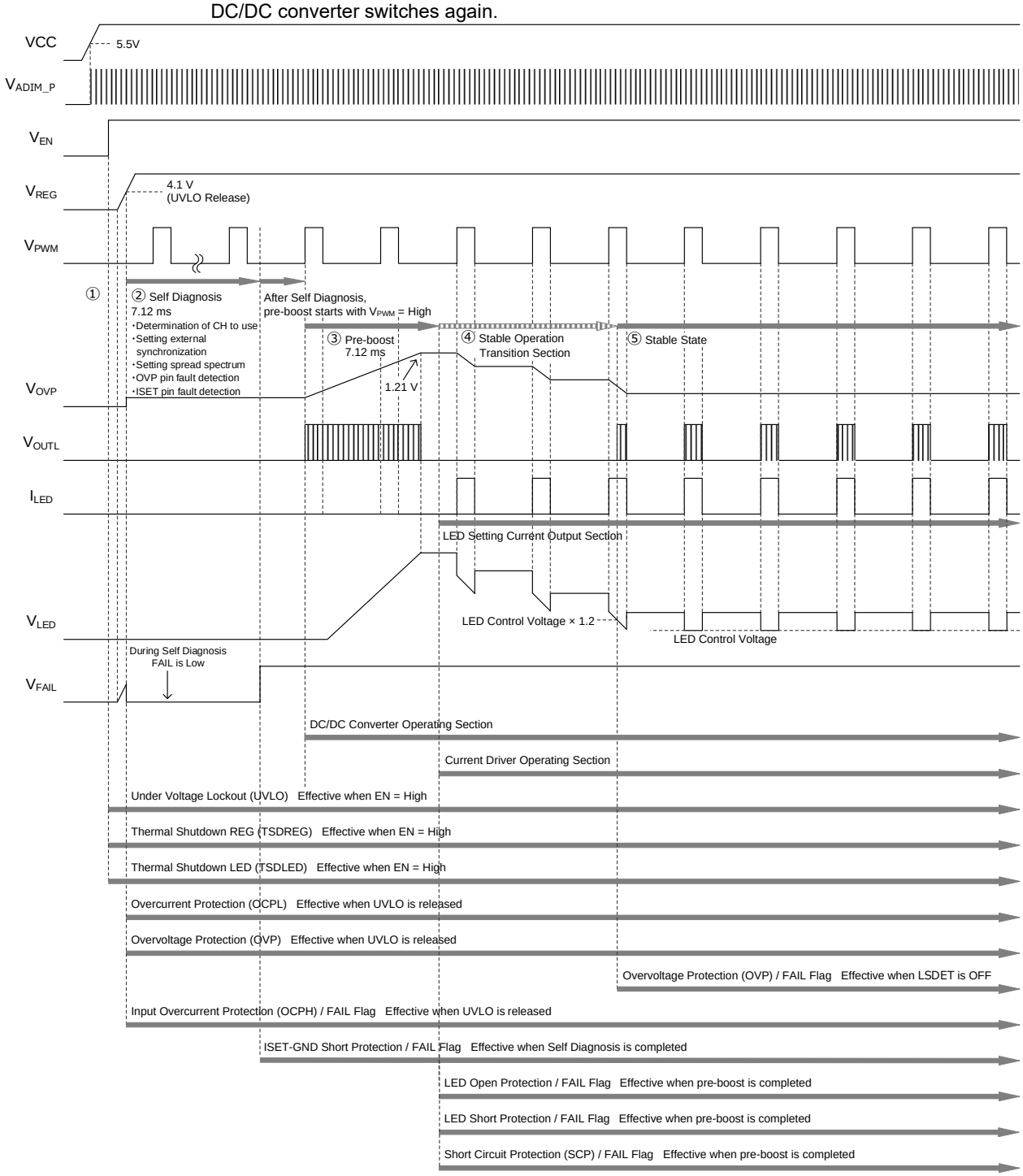


Figure 27. Timing Chart at Startup and Effective Section of Each Protection Function

3 Starting Sequence and Effective Section of Each Protection Function – continued

Unless otherwise stated, the value in the sentence is the Typ value.

3.1 Self Diagnosis (Initial Check)

The contents of Self Diagnosis are as follows.

3.1.1 LED Pin Used / Unused Check

It is possible to check whether the LED pin is used or not by LED pin voltage at the end of Self Diagnosis. If LED pin voltage is 0.3 V or more and 2.5 V or less during Self Diagnosis, the LED pin is diagnosed as unused. If it is diagnosed as unused, the LED pin does not operate and is pulled up to REG pin voltage V_{REG} inside the IC. To select unused channels correctly, the capacitance value to be connected to the LED pin should be 470 pF or less.

3.1.2 SYNC Pin Setting Check

ON/OFF of the external synchronization or spread spectrum function can be set by SYNC pin voltage at the end of Self Diagnosis.

3.1.3 FAIL Pin Connection Check

During Self Diagnosis, the FAIL pin can check the connection between the monitor pin of MCU and the FAIL pin by turning ON the open drain output (ON resistor = 1 kΩ). Determine the pull up voltage and pull up resistor according to FAIL detection voltage on the MCU.

3.1.4 ISET-GND Short Check

In Self Diagnosis, ISET-GND Short Check is done under the same conditions as ISET pin fault (ISET-GND short protection). When ISET-GND short is confirmed, the load switch, DC/DC switching, and current driver are latched OFF. It is reset when V_{EN} = Low or UVLO is detected.

3.1.5 OVP Pin Setting Check

Self Diagnosis checks OVP pin setting. The OVP pin during Self Diagnosis is pulled down with IC built-in resistor of 1 MΩ. When an open failure of the OVP pin occurs, OVP pin voltage falls to 0.1 V or less, and the load switch, DC/DC switching, and the current driver latch OFF. It is reset when V_{EN} = Low or UVLO is detected.

Function Descriptions – continued

4 Stopping Sequence and Effective Section of Each Protection Function

The figure below shows the timing chart when stopping and the effective section of each protection function.

⑤ Stable state : When LED pin voltage (the lowest voltage in LED1 to LED4) drops to the LED control voltage x 1.2, DC/DC converter is switched again.

⑥ Standby state : Decrease EN pin voltage and ADIM_P pin voltage prior to the VCC pin voltage falling. Internal circuit is stopped by falling EN pin voltage, and IC is in standby state.

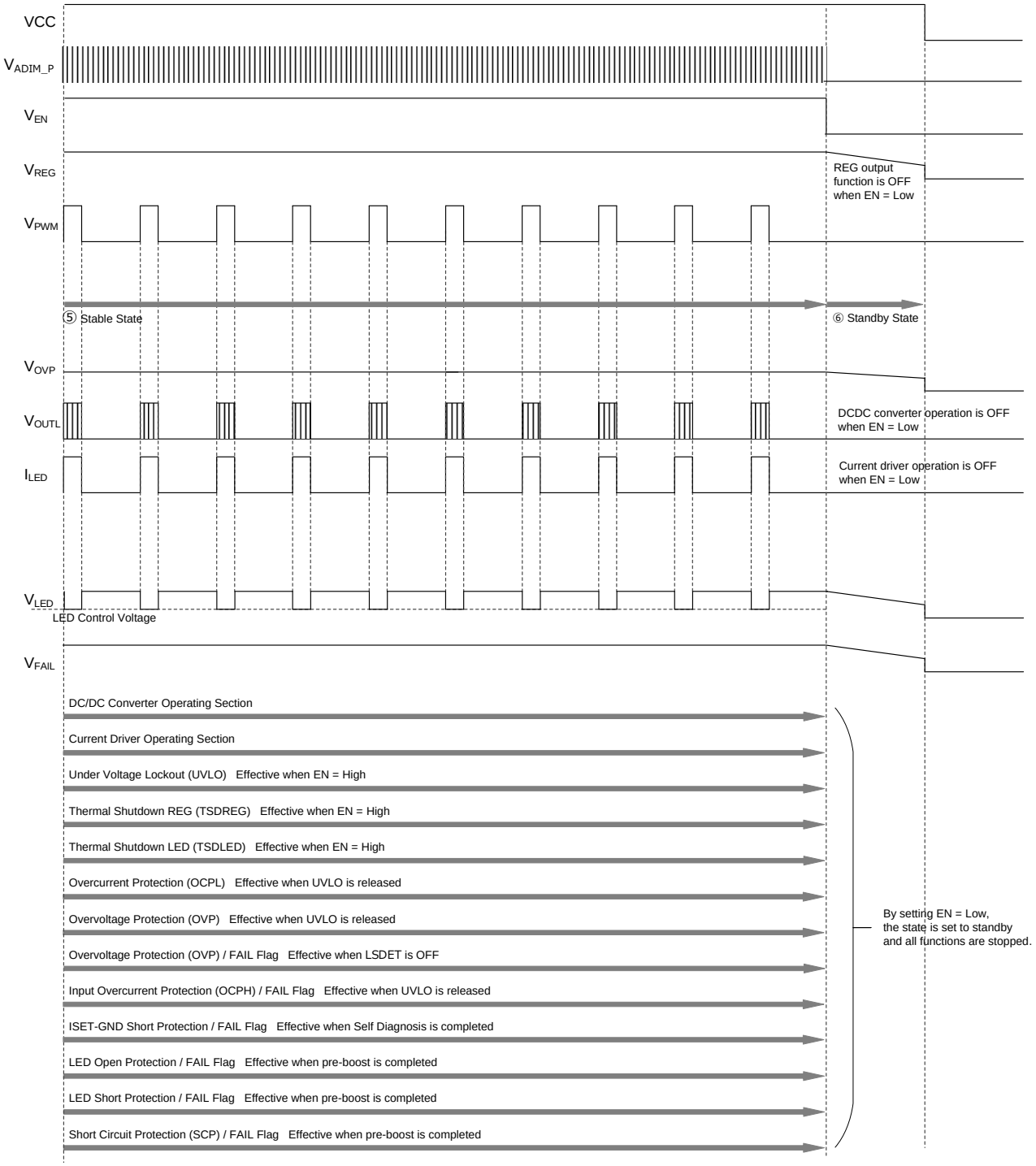
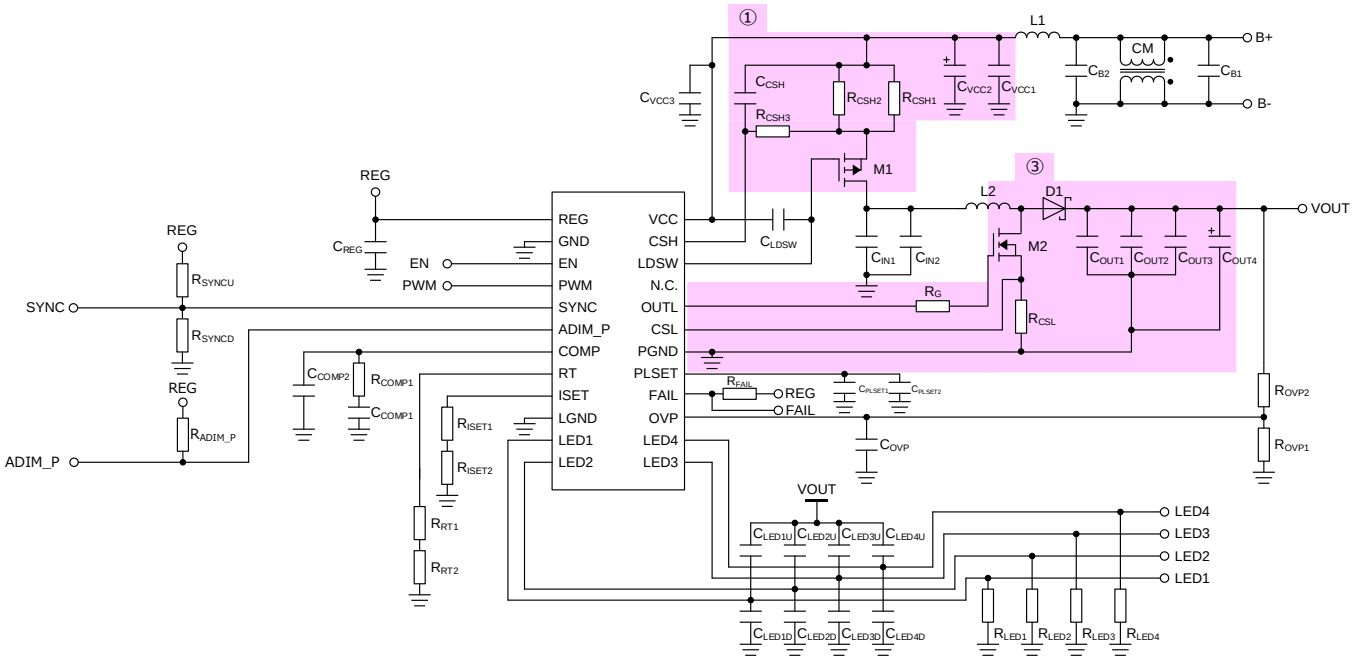


Figure 28. Timing Chart at Stopping and Effective Section of Each Protection Function

PCB Application Circuit Diagram



① Place the Input overcurrent detect resistors R_{CSH1}, R_{CSH2}, VCC pin capacitors C_{VCC1}, C_{VCC2}, and the load switch M1 so that they are shortest. Also, place the input filters R_{CSH3}, C_{CSH} for detecting the input overcurrent close to the CSH pin. They can be placed on the opposite side of the IC and connected with a via.

② Place the input capacitors C_{IN1}, C_{IN2} so that they are as short as the components of both the inductor L2 and the load switch M1. Connect the ground of C_{IN1}, C_{IN2} to the PGND pin via EXP-PAD on the surface layer.

③ To reduce high frequency noises, the wires of the boost "Loop" must be as short as possible. Do not widen the wiring width more than necessary.
- ·Place the boost FET M2 Drain, the inductor L2 and the anodes of the diode D1 so that they are the shortest.
- ·Place the cathode of D1 and the output decoupling capacitors C_{OUT1}, C_{OUT2}, C_{OUT3}, and C_{OUT4} and R_{CSL} so that they are the shortest.
- ·Place the output decoupling capacitors C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} and the PGND pin so that they are the shortest.
- ·Place the PGND pin, R_{CSL} and the boost FET M2 Source so that they are the shortest.
- ·Place the IC and each component on the same surface layer of the board and make connections in the same layer.

④ Place the ground plane on the layer closest to the surface layer where the IC is placed.

⑤ Connect the EXP-PAD to the board ground. Wire the ground pattern connected from the EXP-PAD as wide as possible to improve heat dissipation and connect it to the ground plane with many vias. To ensure heat dissipation according to power loss, place the required number of thermal vias directly under the EXP-PAD and connect them to the ground plane.

⑥ There is no problem if the GND pin, the LGND pin and the PGND pin are connected via the EXP-PAD. However, the power system ground such as the ground of the output decoupling capacitor and the PGND pin contains the noise component of the switching frequency. To reduce this noise component, it is recommended to connect to the ground plane using many vias in the ground pattern around the power system ground.

⑦ Place the bypass capacitor (C_{REG}) between the REG pin and the GND pin as close to pin as possible.

⑧ The connection from VOUT to the anode of the LED panel and the connection from the cathode of the LED panel to the LED1, LED2, LED3, LED4 pins should be as short as possible. Depending on the parasitic inductance component, the LED current may become unstable.

⑨ Do not run the wiring from the cathode of the LED panel to the LED1, LED2, LED3, LED4 pins in parallel with other active lines. Also, place the noise reduction capacitors (C_{LED1D}, C_{LED2D}, C_{LED3D}, C_{LED4D}) so that they are as short as the LED pin. R_{LED1}, R_{LED2}, R_{LED3}, R_{LED4} are pull-down resistors connected to the LED pin of unused channel and is required to generate LED pin voltage that is judged to be unused.

⑩ When using the PWM function, the PWM pin is the active line, so keep it away from other sense lines.

⑪ When using the external synchronization function, the SYNC pin is an active line, so keep it away from other sense lines.

⑫ When using the DC dimming function, the ADIM_P pin is an active line, so keep it away from other sense lines.

⑬ Place R and C connected to the ADIM_P pin, the COMP pin, the RT pin, the ISET pin, the PLSET pin, and the OVP pin as close to the IC as possible. They can be placed on the opposite side of the IC and connected with a via.

⑭ Since OVP pin voltage must be 0.1 V or more during Self Diagnosis, when installing the C_{OVP}, use about 1000 pF as a guide.

⑮ When the VCC voltage is turned ON setting the EN pin to Low, the voltage between the VCC-LDSW pins may open momentarily and an inrush current may flow depending on the VCC startup speed and the type of load switch(M1) used. Be sure to check with the actual application.

⑯ The MUF package requires external components to prevent adjacent short between the OUTL pin and LDSW pin. If concerned, consider the EFV package.

List of External Components

Serial No.	Component Name	Component Value	Product Name	Manufacturer
1	C_{B1}	-	-	-
2	CM	Short	-	-
3	C_{B2}	-	-	-
4	L1	Short	-	-
5	C_{VCC1}	1 µF	GCM21BR71H105KA03	murata
6	C_{VCC2}	-	-	-
7	C_{VCC3}	1 µF	GCM21BR71H105KA03	murata
8	R_{CSH1}	15 mΩ	LTR18 Series	Rohm
9	R_{CSH2}	-	-	-
10	R_{CSH3}	100 Ω	MCR03 Series	Rohm
11	C_{CSH}	100 pF	GCM1882C2A101JA01	murata
12	C_{LDSW}	-	-	-
13	M1	60 V / 36 A	SQJ457EP	VISHAY
14	C_{IN1}	10 µF	GCM32EC71H106KA03L	murata
15	C_{IN2}	10 µF	GCM32EC71H106KA03L	murata
16	L2	22 µH	CLF10060NIT-220M-D	TDK
17	D1	60 V / 5 A	RB088LAM-60TF	Rohm
18	M2	60 V / 8 A	RD3L080SN	Rohm
19	R_{CSL}	75 mΩ	LTR18 Series	Rohm
20	R_G	Short	-	-
21	C_{OUT1}	10 µF	GCM32EC71H106KA03L	murata
22	C_{OUT2}	10 µF	GCM32EC71H106KA03L	murata
23	C_{OUT3}	-	-	-
24	C_{OUT4}	33 µF	GYA1H330MCQ1GS	nichicon
25	R_{OVP1}	10 kΩ	MCR03 Series	Rohm
26	R_{OVP2}	330 kΩ	MCR03 Series	Rohm
27	C_{OVP}	1000 pF	GCM1887U1H102JA01	murata
28	R_{FAIL}	100 kΩ	MCR03 Series	Rohm
29	C_{PLSET1}	1000 pF	GCM1887U1H102JA01	murata
30	C_{PLSET2}	-	-	-
31	R_{LED1}	-	-	-
32	R_{LED2}	-	-	-
33	R_{LED3}	-	-	-
34	R_{LED4}	-	-	-
35	C_{LED1U}	-	-	-
36	C_{LED2U}	-	-	-
37	C_{LED3U}	-	-	-
38	C_{LED4U}	-	-	-
39	C_{LED1D}	-	-	-
40	C_{LED2D}	-	-	-
41	C_{LED3D}	-	-	-
42	C_{LED4D}	-	-	-

List of External Components – continued

Serial No.	Component Name	Component Value	Product Name	Manufacturer
43	C_{REG}	2.2 µF	GCM21BR71C225KA49	murata
44	R_{SYNCU}	-	-	-
45	R_{SYNCD}	100 kΩ	MCR03 Series	Rohm
46	R_{RT1}	33 kΩ	MCR03 Series	Rohm
47	R_{RT2}	Short	-	-
48	R_{COMP1}	200 Ω	MCR03 Series	Rohm
49	C_{COMP1}	0.1 µF	GCM155R11C104KA40D	murata
50	C_{COMP2}	-	-	-
51	R_{ISET1}	15 kΩ	MCR03 Series	Rohm
52	R_{ISET2}	Short	-	-
53	R_{ADIM_P}	100 kΩ	MCR03 Series	Rohm

Note: The component constants vary depending on the operating conditions and the load used.

Selection of Components Externally Connected

Unless otherwise stated, the values in sentences are the values in continuous mode.

Select the application components according to the following procedure.

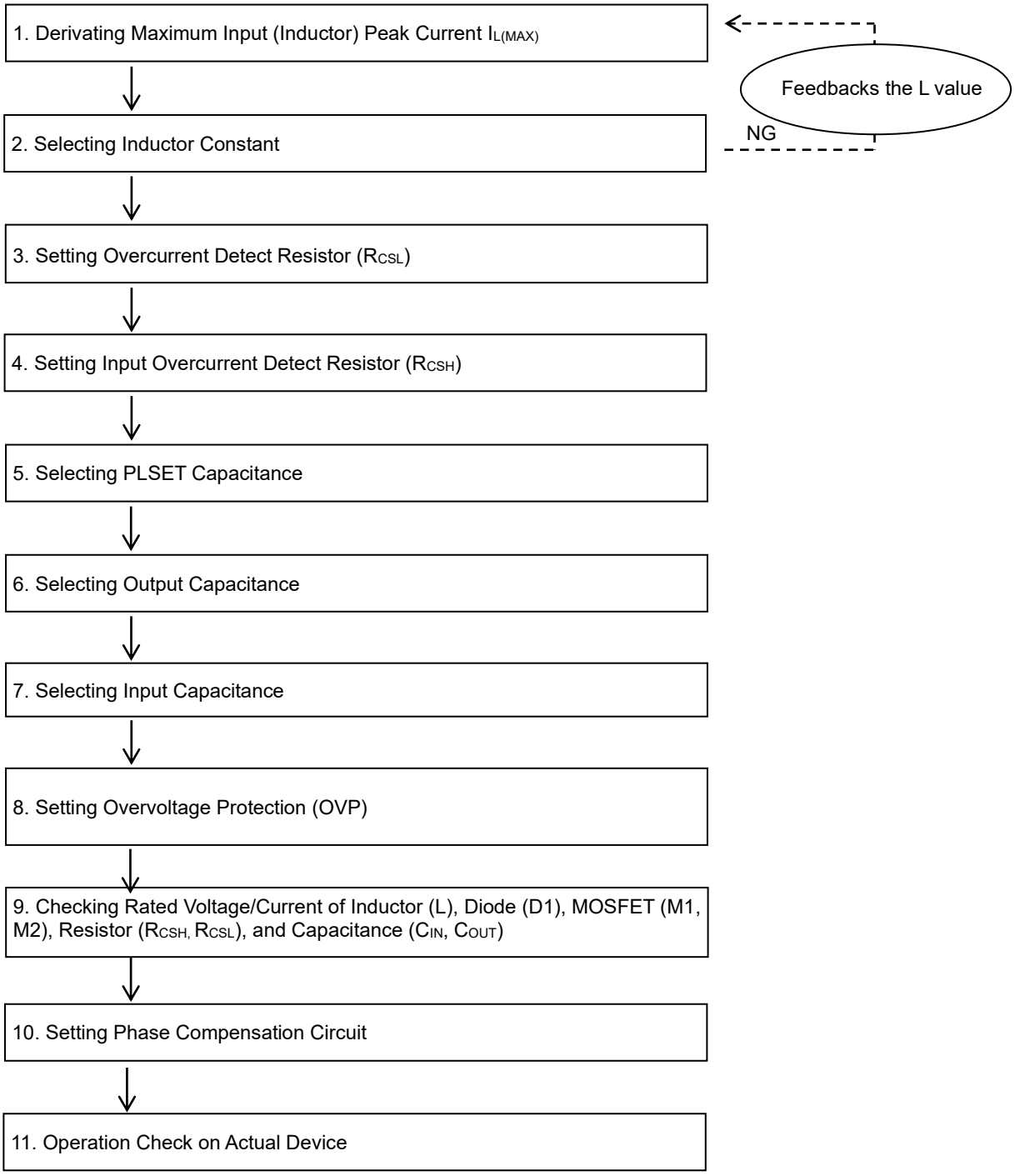


Figure 29. Application Components Selection Procedure

Selection of Components Externally Connected – continued

1 Derivating Maximum Input (Inductor) Peak Current $I_{L(MAX)}$

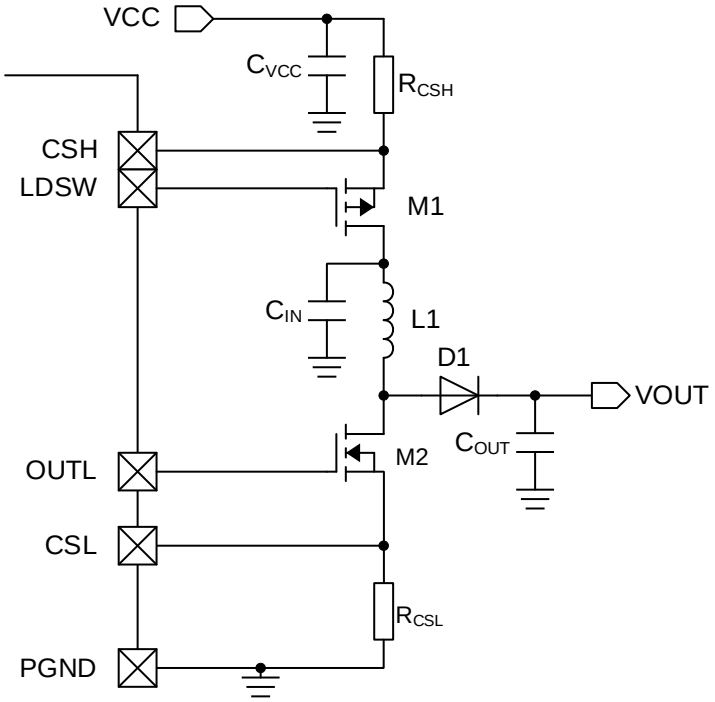


Figure 30. Output Application Circuit Diagram

1.1 Calculating Maximum Output Voltage $VOUT_{(MAX)}$

Calculates $VOUT_{(MAX)}$ in consideration of LED Vf variation and the number of LED stages.

$$VOUT_{(MAX)} = Vf_{(MAX)} \times N + V_{LEDCTL(MAX)}$$

$VOUT_{(MAX)}$: Maximum output voltage
$Vf_{(MAX)}$: Maximum value of LED Vf voltage
N : Number of LED series
$V_{LEDCTL(MAX)}$: Maximum value of LED control voltage

1.2 Calculating Maximum Output Current $I_{OUT(MAX)}$

$$I_{OUT(MAX)} = I_{LED(MAX)} \times M$$

$I_{OUT(MAX)}$: Maximum output current
$I_{LED(MAX)}$: Maximum value of LED current per channel
M : Number of LED parallels

1.3 Calculating Maximum Input (Inductor) Peak Current $I_{L(MAX)}$

$$I_{L(MAX)} = I_{LAVG(MAX)} + \frac{1}{2}\Delta I_{L(MAX)}$$

$$\begin{cases} I_{LAVG(MAX)} = VOUT_{(MAX)} \times \dfrac{\mathrm{I_{OUT(MAX)}}}{\eta \times VCC_{(MIN)}} \\ \Delta I_{L(MAX)} = \dfrac{VCC_{(MIN)}}{L_{(MIN)}} \times \dfrac{1}{f_{OSC(MIN)}} \times \dfrac{\mathrm{VOUT_{(MAX)}} - VCC_{(MIN)}}{\mathrm{VOUT_{(MAX)}}} \end{cases}$$

$I_{L(MAX)}$: Maximum input (inductor) peak current
$I_{LAVG(MAX)}$: Maximum input (inductor) average current
$\Delta I_{L(MAX)}$: Maximum input (inductor) current amplitude
$VCC_{(MIN)}$: Minimum power supply voltage
η : Efficiency (about. 85 %)
$L_{(MIN)}$: Minimum value of inductance
$f_{OSC(MIN)}$: Minimum value of DC/DC oscillation frequency

Selection of Components Externally Connected – continued

2 Selecting Inductor Constant

To maintain stable continuous operation of the current mode DC/DC converter, the L (inductance) value must satisfy the following requirements:

$$R_{CSL} \times \frac{VOUT-VCC}{L \times 10^6} \leq \frac{4020}{R_{RT}}$$

$VOUT$: Output voltage
VCC : Power supply voltage
L : Inductance value
R_{RT} : RT pin connecting resistor
R_{CSL} : CSL pin connecting resistor

Rewriting about L is as follows

$$L \geq \frac{(\mathrm{VOUT}-VCC) \times R_{RT} \times R_{CSL}}{4020 \times 10^6}$$

Consider the variation of the L value and set it with sufficient margin.

3 Setting Overcurrent Detect Resistor (R_{CSL})

$$I_{OCPL(MIN)} = \frac{V_{OCPL(MIN)}}{R_{CSL(MAX)}} > I_{L(MAX)} + \frac{VCC_{(MAX)}}{L_{(MIN)}} \times t_{OCPL}$$

Select the R_{CSL} value so that it will be as above.

$I_{OCPL(MIN)}$: Minimum value of overcurrent protection detect current
$V_{OCPL(MIN)}$: Minimum value of overcurrent protection detect voltage
$R_{CSL(MAX)}$: Maximum value of overcurrent detect resistor
t_{OCPL} : OCPL detect delay time (Max = 84 ns)

4 Setting Input Overcurrent Detect Resistor (R_{CSH})

$$I_{OCPH(MIN)} = \frac{V_{OCPH(MIN)}}{R_{CSH(MAX)}} > \frac{V_{OCPL(MAX)}}{R_{CSL(MIN)}} + \frac{VCC_{(MAX)}}{L_{(MIN)}} \times \mathrm{t_{OCPL}}$$

Select the R_{CSH} value so that it will be as above.

$I_{OCPH(MIN)}$: Minimum value of input overcurrent protection detect current
$V_{OCPH(MIN)}$: Minimum value of input overcurrent protection detect voltage
$R_{CSH(MAX)}$: Maximum value of input current detect resistor
$V_{OCPL(MAX)}$: Maximum value of overcurrent protection detect voltage
$R_{CSL(MIN)}$: Minimum value of overcurrent detect resistor
t_{OCPL} : OCPL detect delay time (MAX = 84 ns)

5 Selecting PLSET Capacitance

$$I_{OFFLOAD(MAX)} = \frac{VOUT_{(MAX)}}{R_{OVP(MIN)}} + I_{SBD(MAX)}$$

$$Q_{OFFLOSS(MAX)} = I_{OFFLOAD(MAX)} \times t_{PWMOFF(MAX)}$$

$$Q_{PWMRISE} = \frac{2.5}{f_{OSC(MIN)}} \times I_{OUT(MIN)}$$

$$Q_{PLSET(MIN)} = \frac{V_{PLSET(MIN)} \times C_{PLSET(MIN)}}{I_{PLSET(MAX)}} \times I_{OUT(MIN)}$$

$$Q_{PLSET(MIN)} > Q_{OFFLOSS(MAX)} + Q_{PWMRISE}$$

Select the C_{PLSET} value so that it will be as above.

$I_{OFFLOAD(MAX)}$: Maximum value of load current when PWM = OFF
$R_{OVP(MIN)}$: Minimum value of overvoltage protection detect resistor
$I_{SBD(MAX)}$: Maximum value of rectifier diode leakage current
$Q_{OFFLOSS(MAX)}$: Maximum value of consumed charge when PWM = OFF
$t_{PWMOFF(MAX)}$: Maximum value of PWM = OFF time
$Q_{PWMRISE}$: Insufficient charge after PWM rise
$Q_{PLSET(MIN)}$: Minimum value of additional pulse output supply charge
$V_{PLSET(MIN)}$: Minimum value of PLSET threshold voltage
$C_{PLSET(MIN)}$: Minimum value of PLSET pin capacitance
$I_{PLSET(MAX)}$: Maximum value of PLSET charging current
$I_{OUT(MIN)}$: Minimum output current

Selection of Components Externally Connected – continued

6 Selecting Output Capacitance

The capacitor C_{OUT} used for the output is determined by the allowable amount of $VOUT_{PP}$ which is the ripple voltage of VOUT.

$$VOUT_{PP(MAX)} = \frac{V_{PLSET(MAX)} \times C_{PLSET(MAX)} \times I_{OUT(MAX)}}{I_{PLSET(MIN)} \times C_{OUT(MIN)}} + \frac{I_{OUT(MAX)} \times D_{ON(MAX)}}{C_{OUT(MIN)} \times f_{OSC(MIN)}} + I_{L(MAX)} \times R_{ESR(MAX)}$$

$VOUT_{PP(MAX)}$	: Maximum value of VOUT ripple voltage	$V_{PLSET(MAX)}$	: Maximum value of PLSET threshold voltage
$I_{PLSET(MIN)}$	: Minimum value of PLSET charging current	$C_{PLSET(MAX)}$	: Maximum value of PLSET pin capacitance
$I_{OUT(MAX)}$	: Maximum output current	$D_{ON(MAX)}$	: Maximum value of DCDC Duty
$C_{OUT(MIN)}$	: Minimum value of output capacitance	$f_{OSC(MIN)}$	: Minimum value of DC/DC oscillation frequency
$I_{L(MAX)}$	: Maximum input (inductor) peak current	$R_{ESR(MAX)}$	: Maximum value of equivalence serial resistor for output capacitance C_{OUT}

The actual VOUT ripple voltage is affected by board layout and component characteristics. Be sure to check on the actual device and set the capacitance value considering sufficient margin so that it will be within the allowable ripple voltage. The maximum value of C_{OUT} that can be set is 100 µF.

7 Selecting Input Capacitance

A ceramic capacitor with an input capacitance of 10 µF or more and a low ESR is recommended. If a capacitor outside this range is selected, an excessive ripple voltage may be superimposed on the input voltage, causing IC malfunction. In addition, the capacitor C_{IN} used for the input is determined by the allowable amount of V_{INPP} which is the ripple voltage of V_{IN}.

8 Setting Overvoltage Protection (OVP)

Overvoltage protection (OVP) is set by an external resistors R_{OVP1}, R_{OVP2}. When the OVP pin becomes 1.21 V or more, it detects overvoltage and stops DC/DC switching. Also, when the OVP pin is 1.21 V or more and the LED1 to LED4 pin voltage is 0.3 V or less, the open state is detected, and the circuit is latched off (Reference PROTECT).

To prevent an open false detection, the resistor division voltage of the maximum value of the output voltage must be below the minimum value of open detection voltage.

Set R_{OVP1}, R_{OVP2} so that they satisfy the following formulas.

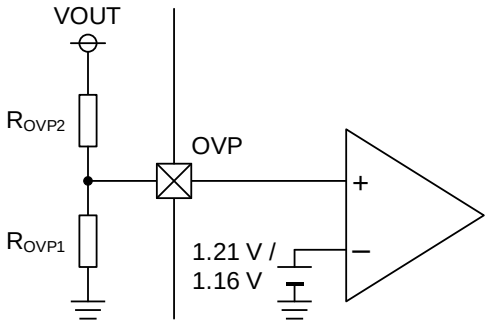


Figure 31. OVP Application Circuit Diagram

$$VOUT_{(MAX)} \times \frac{R_{OVP1}}{(R_{OVP1} + R_{OVP2})} < V_{OVPDET(MIN)} \quad (1)$$

$VOUT_{(MAX)}$	: Maximum output voltage
R_{OVP1}	: Overvoltage protection detect resistor (GND side)
R_{OVP2}	: Overvoltage protection detect resistor (VCC side)
$V_{OVPDET(MIN)}$	: Minimum value of overvoltage protection detect voltage

e.g.) When using 8 series of LEDs with R_{ISET} = 15.1 kΩ and Vf = 3.2 V ±0.2 V.

$$VOUT_{(MAX)} = (3.2 + 0.2) \times 8 + V_{LEDCTL(MAX)}$$

$$= 28.06 \text{ [V]}$$

$$V_{OVPDET(MIN)} = 1.173 \text{ [V]}$$

If R_{OVP1} = 20 kΩ, it is necessary to set R_{OVP2} > 459 kΩ from equation (1).

R_{ISET}	: Resistor for LED current setting
$VOUT_{(MAX)}$	: Maximum output voltage
$V_{LEDCTL(MAX)}$	: Maximum value of LED control voltage
R_{OVP1}	: Overvoltage protection detect resistor (GND side)
R_{OVP2}	: Overvoltage protection detect resistor (VCC side)
$V_{OVPDET(MIN)}$	: Minimum value of overvoltage protection detect voltage

Selection of Components Externally Connected – continued

9 Checking Rated Voltage/Current of Inductor (L), Diode (D1), MOSFET (M1, M2), Resistor (R_{CSH}, R_{CSL}), and Capacitance (C_{IN}, C_{OUT})

(Note 1)	Rated Current	Rated Voltage	Power Dissipation
Input Overcurrent Detect Resistor R_{CSH}	-	-	> $I_{OCPH(MAX)}^2$ x $R_{CSH(MIN)}$
Overcurrent Detect Resistor R_{CSL}	-	-	> $I_{OCPL(MAX)}^2$ x $R_{CSL(MIN)}$
MOSFET M1	> $I_{OCPH(MAX)}$ *(Note 2)*	> $VCC_{(MAX)}$	-
MOSFET M2	> $I_{OCPL(MAX)}$ *(Note 3)*	> $VCC_{(MAX)}$	-
Input Capacitance C_{IN}	-	> $VCC_{(MAX)}$	-
Inductor L	> $I_{A(MAX)}$ *(Note 4)*	-	-
Diode D1	> $I_{A(MAX)}$ *(Note 4)*	> $VOUT_{OVP(MAX)}$ *(Note 5)*	-
Output Capacitance C_{OUT}	-	> $VOUT_{OVP(MAX)}$	-

(Note 1) Consider the variation of external components and make setting with sufficient margin.
(Note 2) $I_{OCPH(MAX)} = V_{OCPH(MAX)}/R_{CSH(MIN)}$
(Note 3) $I_{OCPL(MAX)} = V_{OCPL(MAX)}/R_{CSH(MIN)}$
(Note 4) $I_{A(MAX)} = I_{OCPL(MAX)} + \frac{VCC_{(MAX)}}{L_{(MIN)}} \times t_{OCPL}$ t_{OCPL} : OCPL detect delay time (MAX = 84 ns)

Since the inductor current reaches I_{OCPL} at startup, the recommended setting is Rated Current > $I_{A(MAX)}$.
However, it is possible to set Rated Current > $I_{L(MAX)}$ after confirming that no damage occurs in the actual device.
(Note 5) DC reverse voltage

10 Setting Phase Compensation Circuit

About application stability conditions
The stability conditions of the LED voltage feedback system are as follows.
(1) Phase delay when gain is 1 (0 dB) is 150° or less (i.e., phase margin is 30° or more)
(2) Frequency (unity gain frequency) when gain is 1 (0 dB) is 1/10 or less of switching frequency

By inserting phase lead fz near the unity gain frequency, stability can be ensured by phase compensation.
The phase delay fp1 is determined by C_{OUT} and the output impedance R_L. Each is as follows.

Phase lead $fz = 1/(2\pi \times R_{PC} \times C_{PC})$ [Hz]

Phase delay $fp1 = 1/(2\pi \times R_L \times C_{OUT})$ [Hz]

* Output impedance calculated by $R_L = VOUT/I_{OUT}$

Good results can be obtained by setting fz from 1 kHz to 10 kHz. Substitute the value at maximum load for R_L.

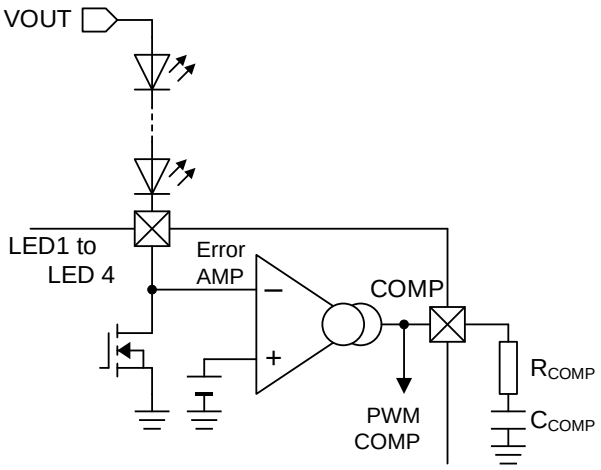


Figure 32. Error AMP Block Application Circuit Diagram

In addition, this setting is a simple calculation and is not calculated exactly, so it may be necessary to make adjustments on the actual device. Also, these characteristics will change depending on the board layout, load conditions, etc., so when designing for mass production, make sure to check the actual device before setting.

Selection of Components Externally Connected – continued

11 Operation Check on Actual Device

Select the constant according to the above procedure and precautions regarding constant setting. In addition, since this selection is calculated by theoretical calculation, it does not include variations in external components or changes in their characteristics and is not guaranteed. The parameters that affect the characteristics of the product will change depending on the actual layout pattern, such as power supply voltage, LED current / number of lamps, inductor, output capacitance, and switching frequency, so be sure to check with the actual device.

Additional Components for EMC Countermeasure

The figure below shows the examples of EMC countermeasure components.

(1) Capacitor for boost FET current loop noise reduction
(2) Capacitor for output current loop noise reduction
(3) Capacitor for power line high frequency noise reduction
(4) Low-pass filter for power line noise reduction
(5) Common mode filter for power line noise reduction
(6) Snubber circuit for boost FET high frequency noise reduction
(7) Snubber circuit for ringing reduction during boost FET switching

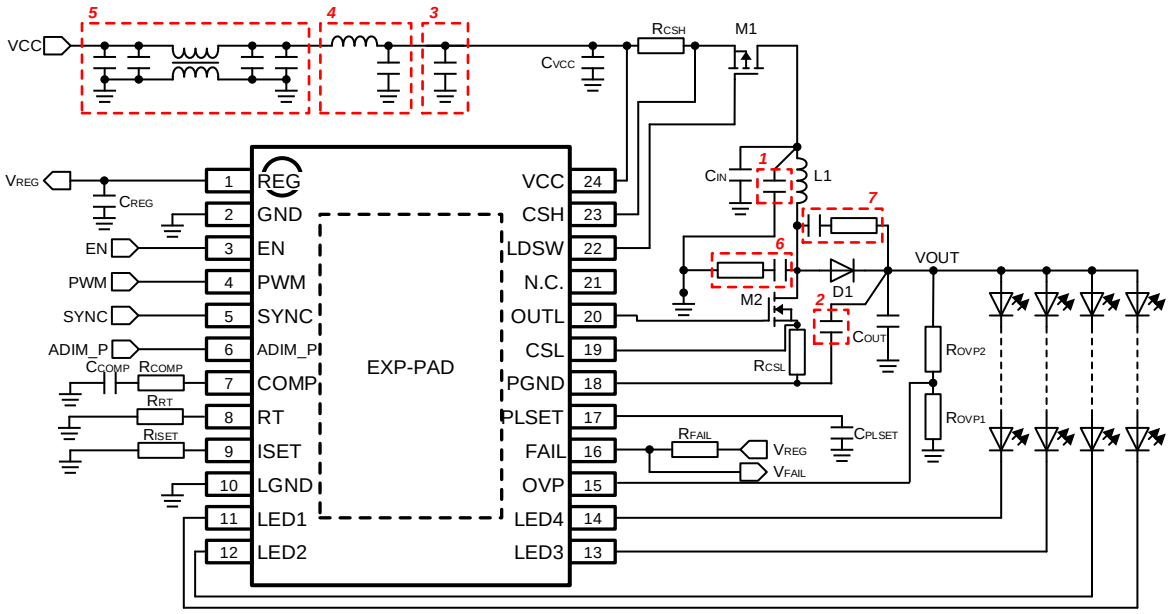


Figure 33. Application Circuit Diagram Reference Example (including EMC countermeasure components)

Precautions for PCB Layout

PCB layout patterns have a significant impact on efficiency and ripple characteristics, so care must be taken when designing. In the boost configuration, there is a "Loop" as shown in the figure on the right. Place the components in the Loop as close as possible (e.g., place GND of C_{OUT} and PGND as close together).
Also, make sure that the wiring in each loop is as low impedance as possible.
Refer to "PCB Application Circuit Diagram" for other detailed precautions regarding PCB layout.

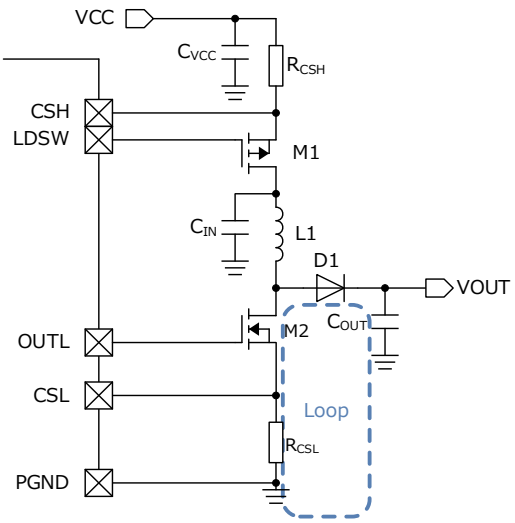


Figure 34. Circuit of DC/DC Block

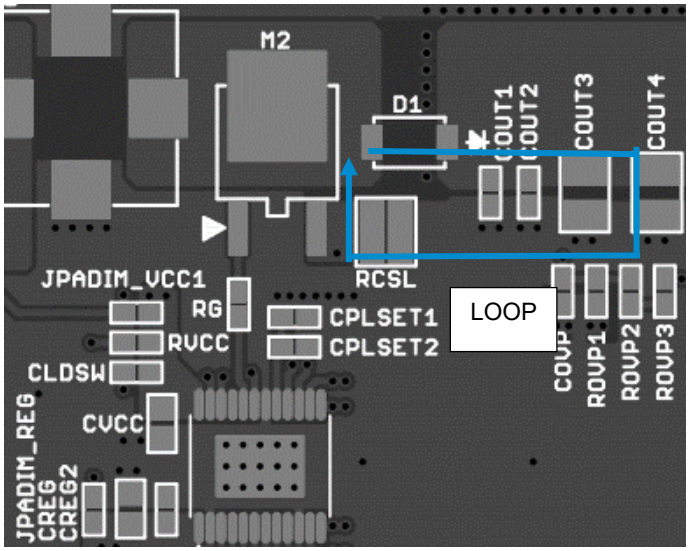


Figure 35. BD83A14EFV-M PCB TOP-layer

Power Consumption Calculation Example

The maximum value of IC power consumption can be easily calculated by the following procedure. Take heat dissipation measures so that the rise in chip temperature due to this power consumption does not exceed Tjmax under the environmental conditions (ambient temperature, heat dissipation fins, etc.) used by the customer.

$$P_{C(MAX)} = I_{CC(MAX)} \times VCC_{(MAX)} \quad \text{(1) Circuit power}$$

$$+C_{ISS(MAX)} \times V_{REG(MAX)} \times f_{OSC(MAX)} \times V_{REG(MAX)} \quad \text{(2) OUTL FET drive stage power}$$

$$+\{V_{LEDCTL(MAX)} \times M + (Vf_{(MAX)} - Vf_{(MIN)}) \times N \times (M-1)\} \times I_{LED(MAX)} \quad \text{(3) Current driver power}$$

$$VOUT_{(MAX)} = Vf_{(MAX)} \times N + V_{LEDCTL(MAX)} \quad \text{(4) Output voltage}$$

$$I_{OUT(MAX)} = I_{LED(MAX)} \times M \quad \text{(5) Output current}$$

$$I_{LAVG(MAX)} = VOUT_{(MAX)} \times I_{OUT(MAX)} / (\eta \times VCC_{(MIN)}) \quad \text{(6) Input (inductor) average current}$$

$P_{C(MAX)}$	: Maximum value of IC power consumption	$Vf_{(MAX)}$	: Maximum value of LED Vf voltage
$I_{CC(MAX)}$	: Maximum value of circuit current	$Vf_{(MIN)}$	: Minimum value of LED Vf voltage
$VCC_{(MAX)}$	: Maximum value of power supply voltage	N	: Number of LED series
$C_{ISS(MAX)}$	: Maximum value of OUTL FET gating capacitance	$I_{LED(MAX)}$	: Maximum value of LED current per channel
$f_{OSC(MAX)}$	: Maximum value of DC/DC oscillation frequency	$VOUT_{(MAX)}$	: Maximum output voltage
$V_{REG(MAX)}$	: Maximum value of reference voltage	$I_{OUT(MAX)}$	: Maximum value of output current
$V_{LEDCTL(MAX)}$	: Maximum value of LED control voltage	$I_{LAVG(MAX)}$	: Maximum value of input (inductor) average current
M	: Number of LED parallels	η	: Efficiency (about 85 %)

Power Consumption Calculation Example – continued

<Calculation Example>

Calculate IC power consumption using the following conditions as an example.

$I_{CC(MAX)}$	Maximum value of circuit current	10 mA	M	Number of LED parallels	4 rows
$VCC_{(MAX)}$	Maximum value of power supply voltage	13.5 V	$Vf_{(MAX)}$	Maximum value of LED Vf voltage	3.4 V
$C_{ISS(MAX)}$	Maximum value of the OUTL pin external FET gating capacitance	380 pF	$Vf_{(MIN)}$	Minimum value of LED Vf voltage	3.0 V
$f_{OSC(MAX)}$	Maximum value of DC/DC oscillation frequency	330 kHz	N	Number of LED series	8 stages
$V_{REG(MAX)}$	Maximum value of reference voltage	5.3 V	$I_{LED(MAX)}$	Maximum value of LED current per channel	65 mA
$V_{LEDCTL(MAX)}$	Maximum value of LED control voltage	0.84 V	η	Efficiency (about 85 %)	0.85

From equation (3),

$$\begin{aligned} VOUT_{(MAX)} &= Vf_{(MAX)} \times N + V_{LEDCTL(MAX)} \\ &= 3.4\,V \times 8 + 0.84\,V \\ &= 28.04 \text{ [V]} \end{aligned}$$

From equation (5),

$$\begin{aligned} I_{OUT(MAX)} &= I_{LED(MAX)} \times M \\ &= 65\,mA \times 4 \\ &= 260 \text{ [mA]} \end{aligned}$$

Therefore, the maximum value of IC power consumption $P_{C(MAX)}$ is calculated as follows:

$$\begin{aligned} P_{C(MAX)} = {} & 10\,mA \times 13.5\,V \\ & +380\,pF \times 5.3\,V \times 330\,kHz \times 5.3\,V \\ & +\{0.84\,V \times 4 + (3.4\,V - 3.0\,V) \times 8 \times (4-1)\} \times 65\,mA \\ = {} & 0.98 \text{ [W]} \end{aligned}$$

From thermal resistance θja = 34.9 °C/W, the maximum calorific value $\Delta t_{(MAX)}$ can be estimated by the following equation.

$$\Delta t_{(MAX)} = P_{C(MAX)} \times \theta ja = 0.98\,W \times 34.9\,℃/W = 34.2 \text{ [°C]}$$

When the ambient temperature is 85 °C, the maximum chip temperature $t_{C(MAX)}$ is following.

$$t_{C(MAX)} = 85\,℃ + 34.2\,℃ = 119.2 \text{ [°C]}$$

Make sure that $t_{C(MAX)}$ calculated here is less than Tjmax = 150 °C.

The above is a simple calculation example only. The value of thermal resistance varies depending on the actual board conditions and layout. Confirm the calculation here as a guide for thermal design.

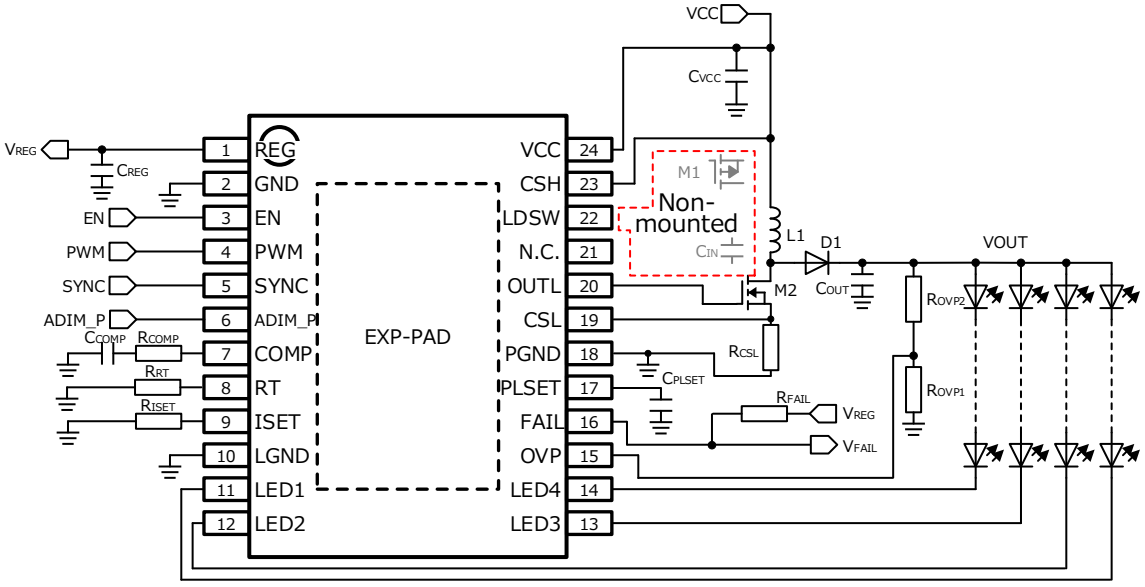
Application Circuit Example

1 Peripheral Circuit When PMOS Is Not Used

When the load switch M1 is not required, such as when using FUSE on the input side, connect the CSH pin and inductor L1 and open the LDSW pin.
Also, set FUSE rating to I_{FUSE} or more.

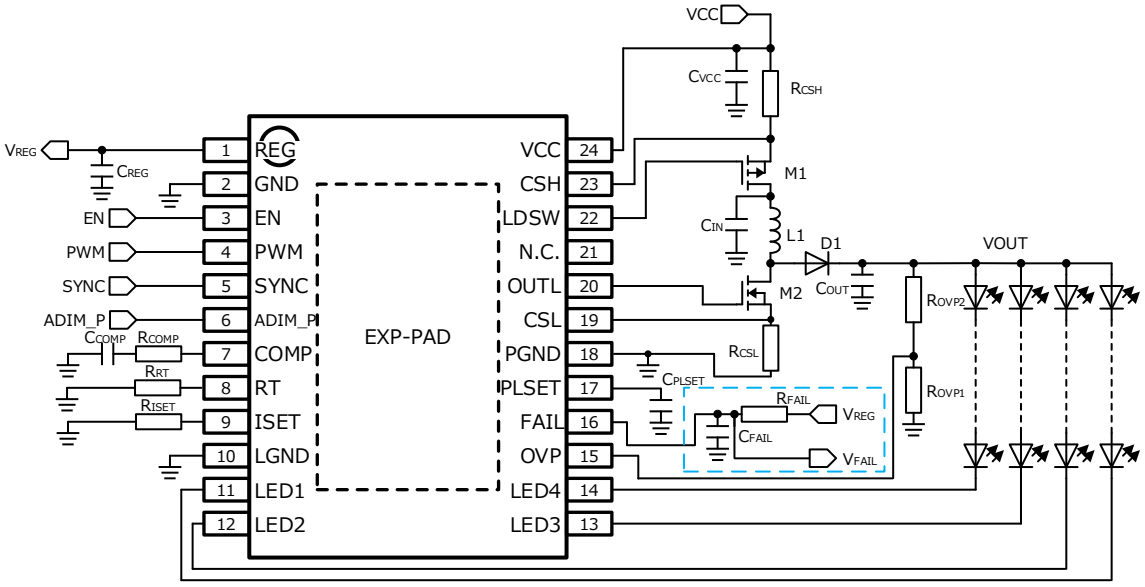
$$I_{FUSE} > \frac{V_{OCPL(MAX)}}{R_{CSL(MIN)}} + \frac{VCC_{(MAX)}}{L_{(MIN)}} \times t_{OCPL}$$

I_{FUSE} : FUSE rated current
$VCC_{(MAX)}$: Maximum value of power supply voltage
$L_{(MIN)}$: Minimum value of inductance
t_{OCPL} : OCPL detect delay time (MAX = 84 ns)
$V_{OCPL(MAX)}$: Maximum value of overcurrent protection detect voltage
$R_{CSL(MIN)}$: Minimum value of overcurrent detect resistor

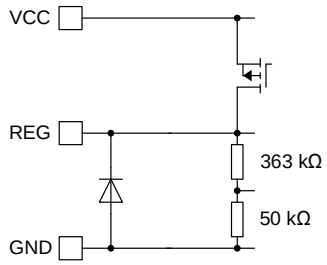
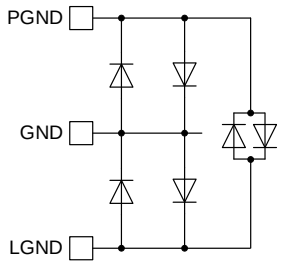
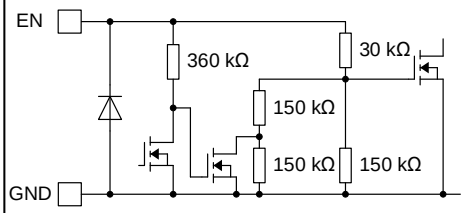


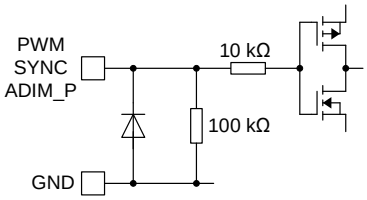
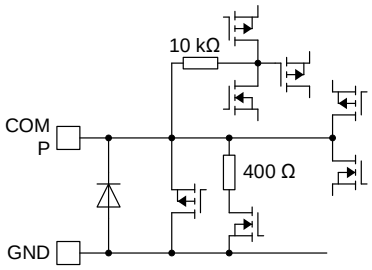
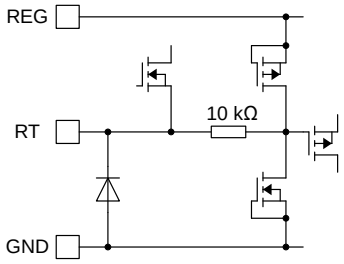
2 Monitoring the Status of the FAIL Pin with Microcontroller

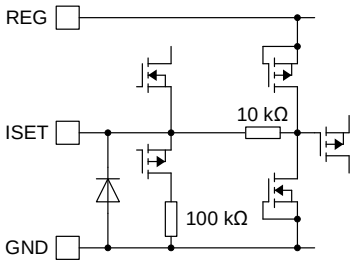
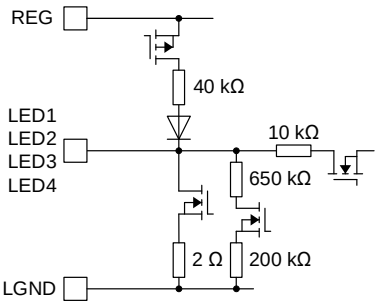
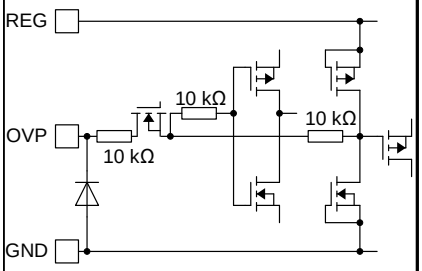
OCPH function starts operation again after stopping operation for the specified timer time. Therefore, the FAIL pin periodically outputs the detect/release flag until the error is cleared. In the case of a system configuration that monitors the FAIL pin with a microcontroller, there is a possibility that it will be erroneously determined as a normal state even though it is in an abnormal state. By adding C_{FAIL} as shown below, it is possible to fix the FAIL output to Low in an abnormal state.

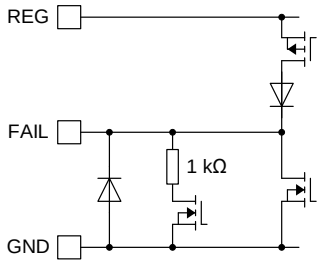
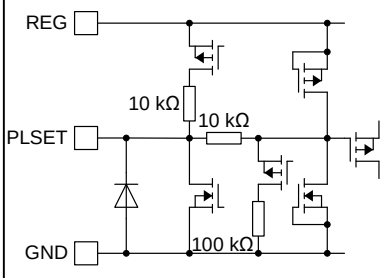
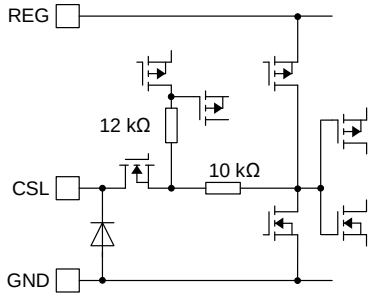


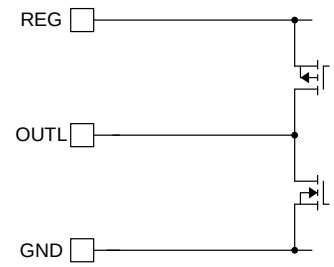
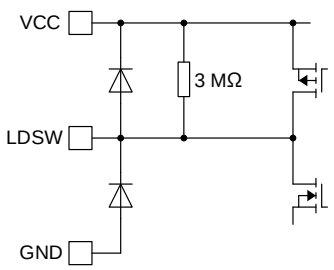
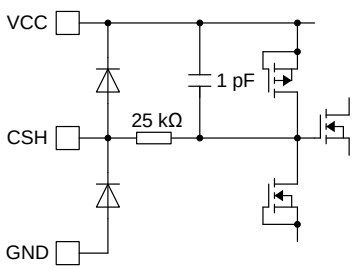
I/O Equivalence Circuit

REG, VCC	GND, LGND, PGND	EN
		

PWM, SYNC, ADIM_P	COMP	RT
		

ISET	LED1 - LED4	OVP
		

FAIL	PLSET	CSL
		

OUTL	LDSW	CSH
		

All values are Typ values.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

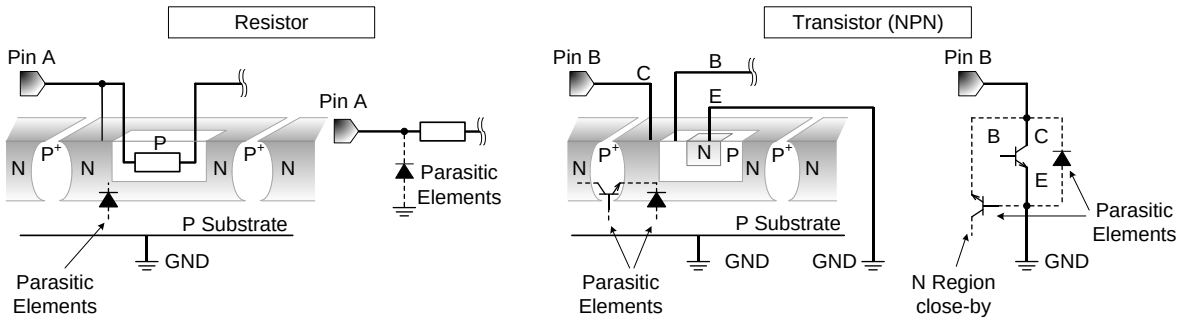


Figure 36. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

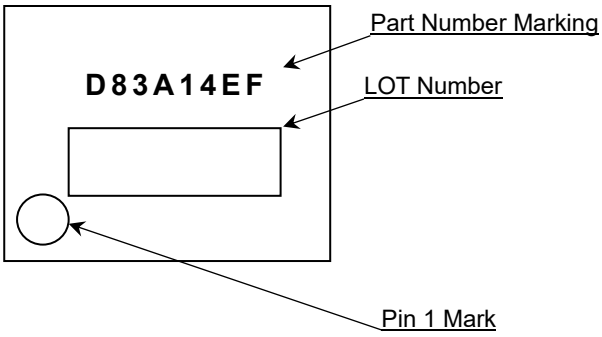
B	D	8	3	A	1	4	x	x	x	-	M E 2

Package
EFV: HTSSOP-B24
MUF: VQFN24FV4040

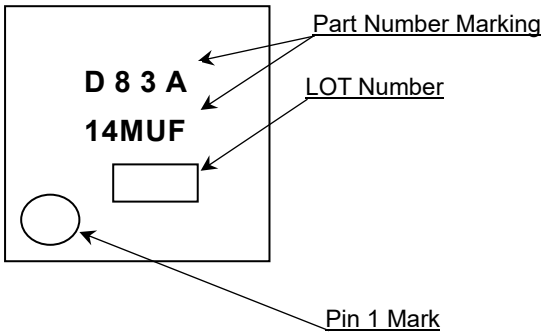
Product rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams

HTSSOP-B24 (TOP VIEW)

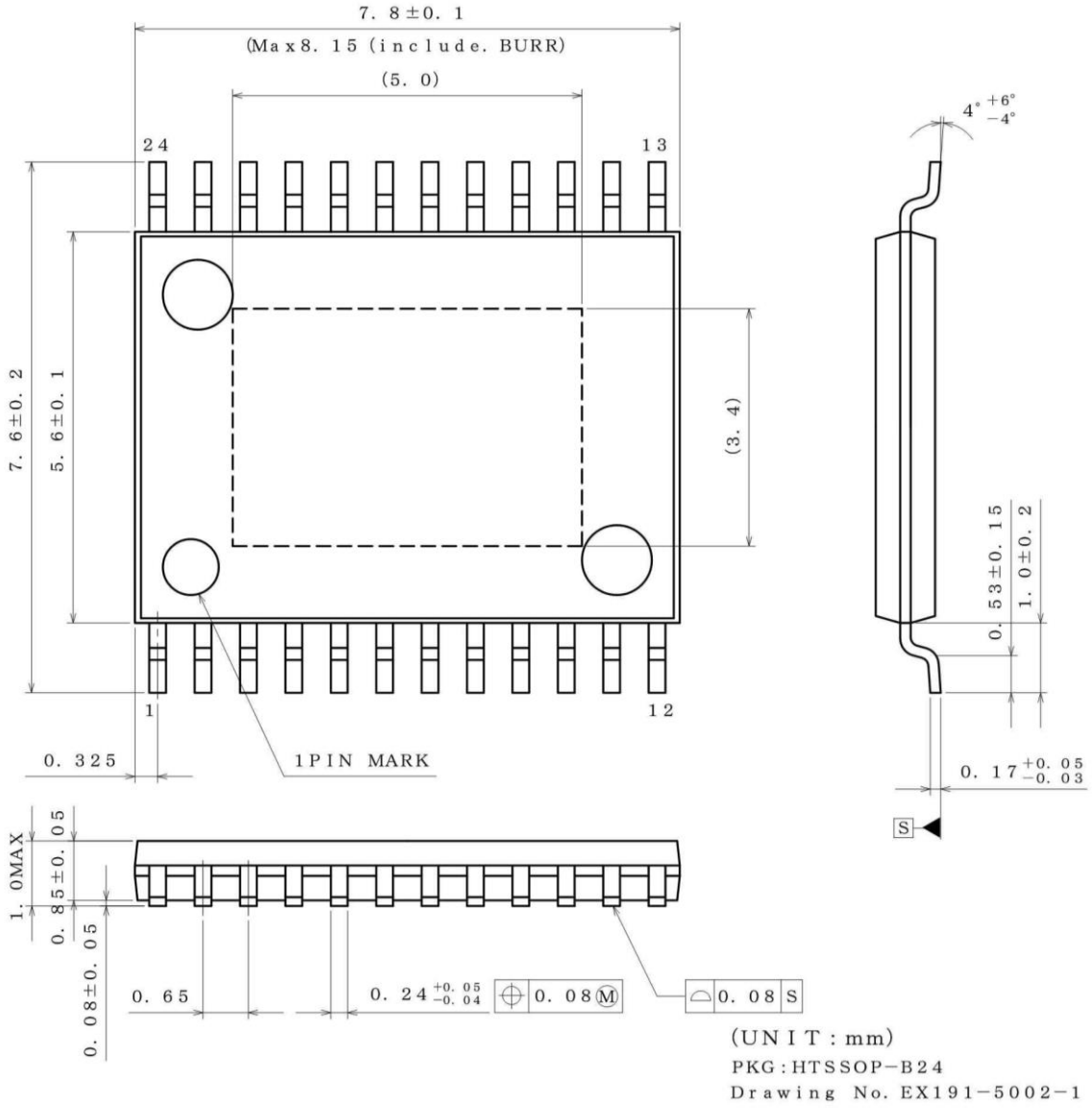


VQFN24FV4040 (TOP VIEW)



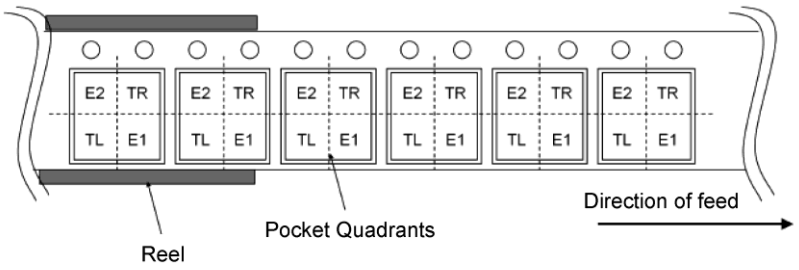
Physical Dimension and Packing Information

Package Name	HTSSOP-B24



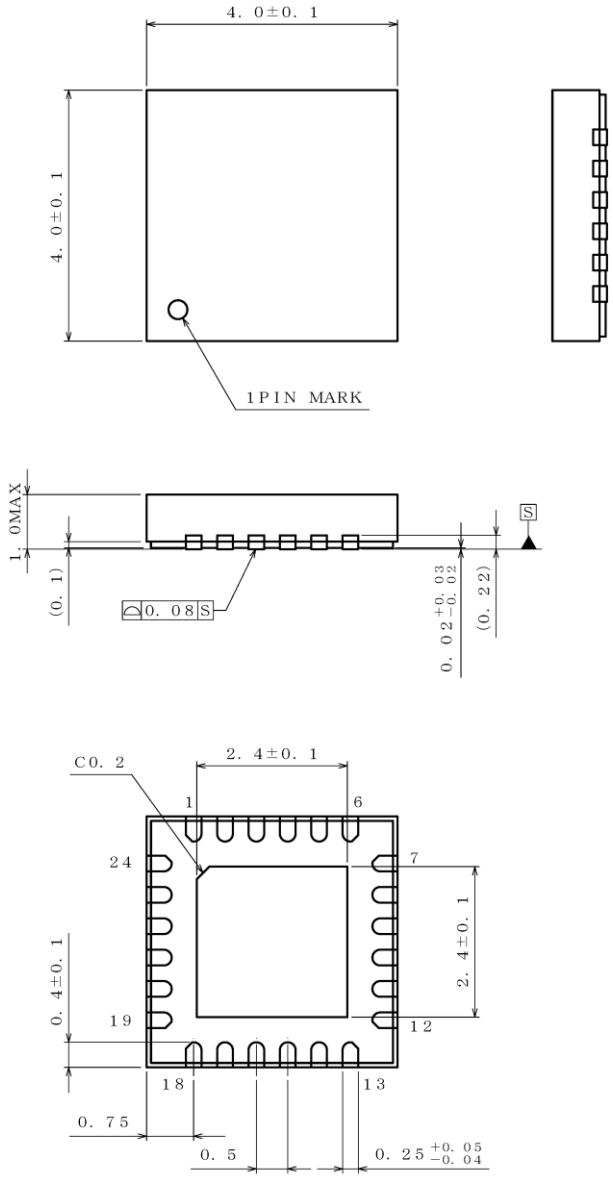
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Physical Dimension and Packing Information - continued

Package Name	VQFN24FV4040



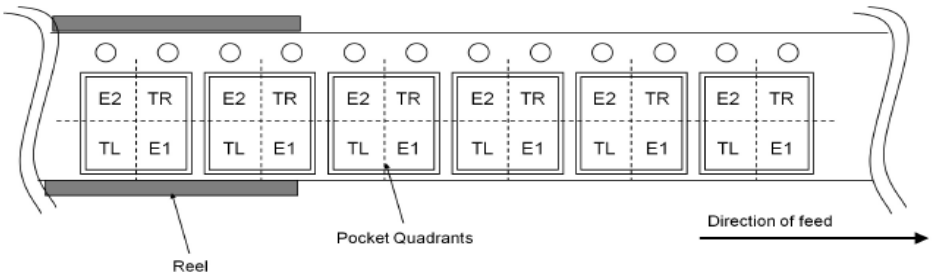
(UNIT : mm)

PKG : VQFN24FV4040
Drawing No. EX394−5001−1

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
08.Jul.2022	001	New Release
30.Nov.2022	002	P.1 Add VQFN24FV4040 package information. P.3 Add signal type ”O: Output signal to other units” P.3, 4 Add Pin assign of VQFN24FV4040 package. ADIM_P Signal Type change A to I. P.4 Add Note 2. P.9 Add Note1 of No.6, 7, 8 protect function. Add Note6. P.10 Add thermal resistance of VQFN24FV4040 package. P.22 Figure.21 X axis name change P.25 Modify the diagram of ADIM_P input timing. P.28 Add sentence ⑯. P.37 Remove P.28 of P.28 PCB Application Circuit Diagram P.46 Add physical Dimension and Packing Information of VQFN24FV4040 package.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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