SLG46108

GreenPAK
Ultra-small Programmable Mixed-signal Matrix

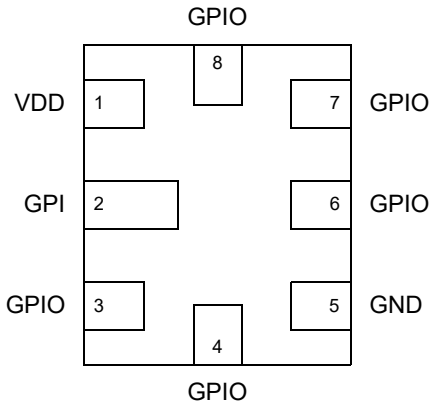
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 8-pin STQFN: 1.0 x 1.2 x 0.55 mm, 0.4 mm pitch

Applications

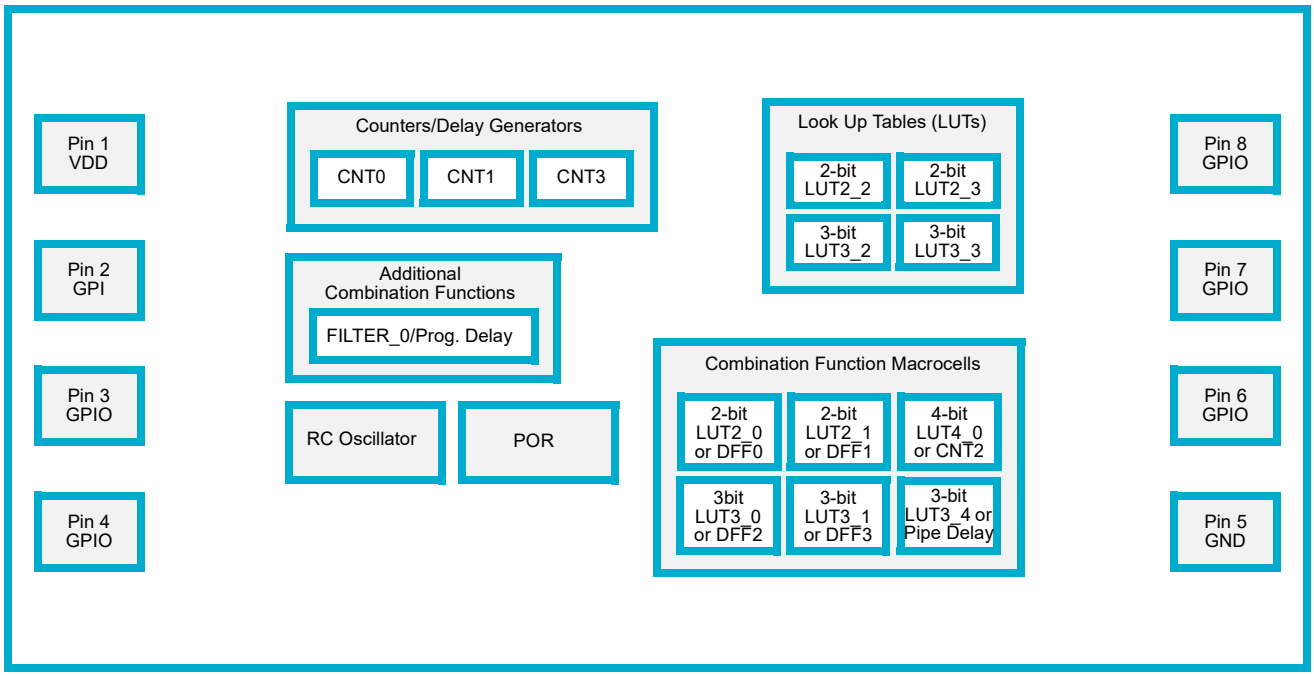
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-8
(Top View)

Block Diagram



1.0 Overview

The SLG46108 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46108. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Four Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven Combination Function Macrocell
  - Two Selectable D Flip-Flop / Latches (DFF) or 2-bit LUTs
  - Two Selectable D Flip-Flop / Latches (DFF) or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output
  - One Selectable Counter/Delay (CNT/DLY) or 4-bit LUT
  - One Programmable Delay / Deglitch Filter
- Three 8-bit Counter / Delay Generators (CNT/DLY) with external clock/reset
- RC Oscillator (RC OSC)
- Power On Reset (POR)

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O
4	GPIO	General Purpose I/O
5	GND	GND
6	GPIO	General Purpose I/O
7	GPIO	General Purpose I/O
8	GPIO	General Purpose I/O

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46108's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Dialog semiconductor to integrate into the production process.

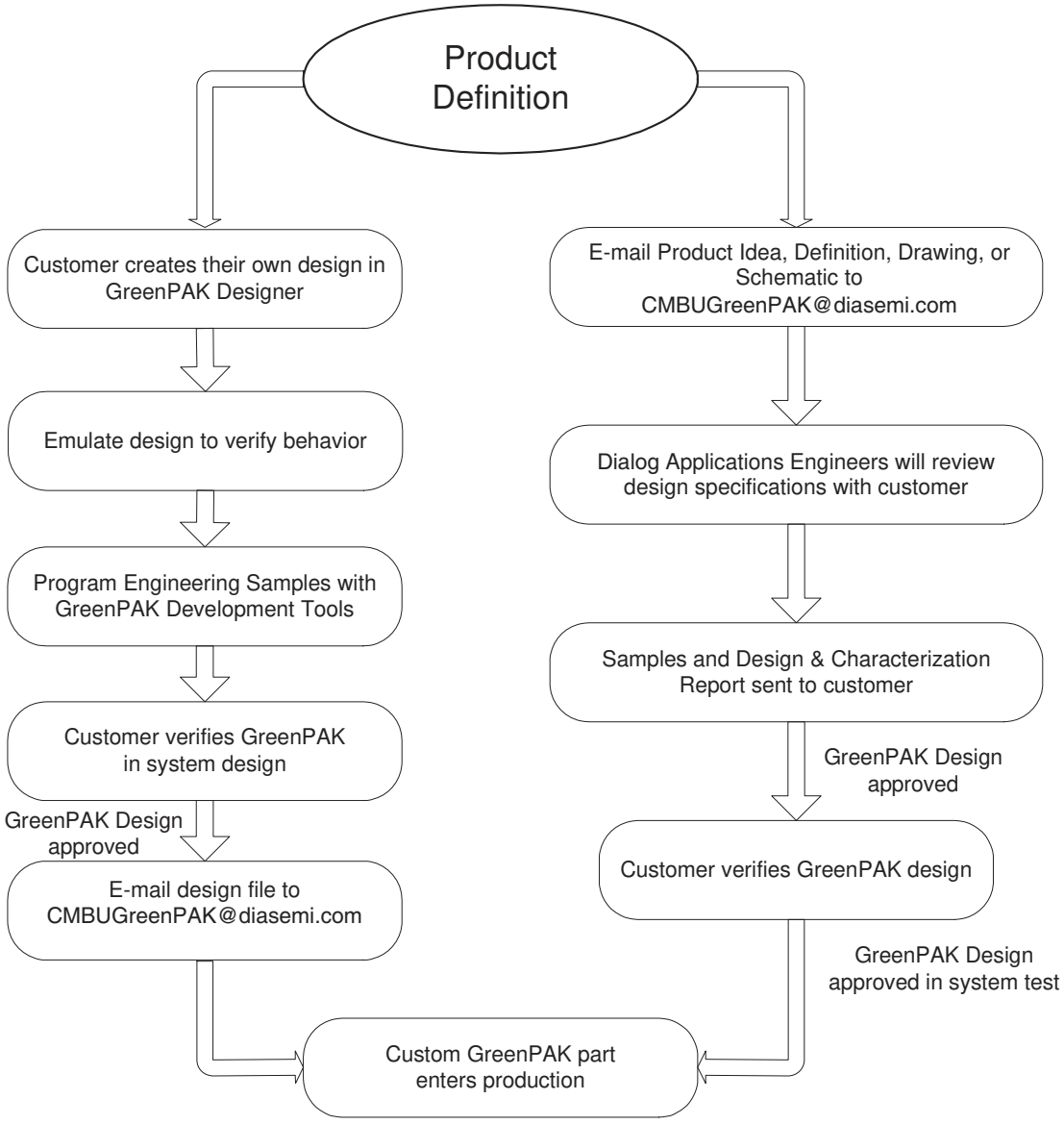


Figure 1. Steps to create a custom GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46108V	8-pin STQFN
SLG46108VTR	8-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.28	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.071	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.276	--	V_{DD}	V
		Low-Level Logic Input	0.936	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.730	V
		Logic Input with Schmitt Trigger	--	--	0.475	V
		Low-Level Logic Input	--	--	0.517	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.26	0.47	0.60	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.692	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.794	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL} = 100 µA	--	0.01	0.016	V
		Push-Pull 2X, I_{OL} = 100 µA	--	0.005	0.007	V
		Open Drain NMOS 1X, I_{OL} = 100 µA	--	0.005	0.006	V
		Open Drain NMOS 2X, I_{OL} = 100 µA	--	0.003	0.003	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.045	1.506	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.097	2.982	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.984	1.363	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	2.011	2.743	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	2.029	2.763	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	4.020	5.471	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	--	0.54	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.302	1.505	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.681	0.902	1.170	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	927	1083	1271	kΩ
		100 k Pull Up	93	110	130	kΩ
		10 k Pull Up	10.9	12.7	14.8	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	915	1084	1271	kΩ
		100 k Pull Down	93	125	130	kΩ
		10 k Pull Down	10.4	14.0	14.9	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.3 Electrical Characteristics (3.3 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.52	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.840	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.170	--	V_{DD}	V
		Low-Level Logic Input	1.086	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.255	V
		Logic Input with Schmitt Trigger	--	--	0.934	V
		Low-Level Logic Input	--	--	0.669	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.56	0.71	0.86	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.721	3.108	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.864	3.204	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL} = 3 mA	--	0.175	0.257	V
		Push-Pull 2X, I_{OL} = 3 mA	--	0.086	0.122	V
		Open Drain NMOS 1X, I_{OL} = 3 mA	--	0.085	0.121	V
		Open Drain NMOS 2X, I_{OL} = 3 mA	--	0.043	0.061	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.774	11.066	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.351	21.730	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.491	6.438	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.124	12.884	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	9.227	12.995	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	17.995	25.459	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	--	0.52	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.718	0.901	1.173	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	922	1082	1272	kΩ
		100 k Pull Up	92	109	129.0	kΩ
		10 k Pull Up	9.6	11.6	14.1	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	916	1083	1270	kΩ
		100 k Pull Down	96	109	129	kΩ
		10 k Pull Down	9.7	11.4	14.2	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.81	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.744	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.190	--	V_{DD}	V
		Low-Level Logic Input	1.185	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.877	V
		Logic Input with Schmitt Trigger	--	--	1.488	V
		Low-Level Logic Input	--	--	0.765	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.77	0.94	1.14	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.171	4.761	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.336	4.879	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL} = 5 mA	--	0.225	0.325	V
		Push-Pull 2X, I_{OL} = 5 mA	--	0.111	0.156	V
		Open Drain NMOS 1X, I_{OL} = 5 mA	--	0.110	0.155	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.057	0.080	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.656	30.203	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.170	56.319	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.087	8.611	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	12.321	17.147	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	12.444	17.282	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	24.032	33.581	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}			0.51	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.675	0.901	1.174	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	921	1080	1269	kΩ
		100 k Pull Up	92	108	129	kΩ
		10 k Pull Up	8.8	11.0	13.9	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	916	1082	1277	kΩ
		100 k Pull Down	92	108	129	kΩ
		10 k Pull Down	8.6	10.9	14.0	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	Chip Quiescent	0.27	0.51	0.79	µA
		OSC 2 MHz, predivide = 1, divide = 1	21.86	32.18	45.29	µA
		OSC 2 MHz, predivide = 1, divide = 8	21.77	31.96	44.88	µA
		OSC 2 MHz, predivide = 1, divide = 64	21.70	31.82	44.70	µA
		OSC 2 MHz, predivide = 2, divide = 1	18.97	26.19	35.69	µA
		OSC 2 MHz, predivide = 2, divide = 8	18.92	26.07	35.49	µA
		OSC 2 MHz, predivide = 2, divide = 64	18.89	26.01	35.40	µA
		OSC 2 MHz, predivide = 4, divide = 1	17.53	23.21	30.93	µA
		OSC 2 MHz, predivide = 4, divide = 8	17.51	23.16	30.83	µA
		OSC 2 MHz, predivide = 4, divide = 64	17.49	23.12	30.78	µA
		OSC 2 MHz, predivide = 8, divide = 1	16.81	21.70	28.51	µA
		OSC 2 MHz, predivide = 8, divide = 8	16.80	21.67	28.46	µA
		OSC 2 MHz, predivide = 8, divide = 64	16.79	21.65	28.43	µA
		OSC 25 kHz, predivide = 1, divide = 1, 8 , 64	5.16	5.71	6.73	µA
		OSC 25 kHz, predivide = 2, divide = 1, 8 , 64	5.13	5.65	6.63	µA
		OSC 25 kHz, predivide = 4, divide = 1, 8 , 64	5.11	5.62	6.57	µA
		OSC 25 kHz, predivide = 8, divide = 1, 8 , 64	5.10	5.60	6.54	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	33.4	36.4	13.6	15.0	9.8	10.6	ns
tpd	Delay	Digital Input to PP 2X	31.1	34.1	12.8	14.1	9.3	10.1	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	33.4	35.7	13.8	15.2	10.0	11.0	ns
tpd	Delay	Low Voltage Digital input - to PP 1X (Vih = min)	214.1	623.0	216.8	184.6	105.0	120.0	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 1x NMOS	--	79.4	--	28.0	--	18.0	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 1x PMOS	33.8	--	13.8	--	10.0	--	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 2x NMOS	--	71.3	--	25.1	--	16.1	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 2x PMOS	31.4	--	12.9	--	9.4	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	33.5	--	13.7	--	9.9	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	--	36.3	--	15.0	--	10.9	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	24.5	22.3	10.8	9.5	8.0	7.0	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	25.8	24.8	11.3	10.5	8.4	7.6	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	29.5	26.0	12.7	10.9	9.3	8.0	ns

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	30.1	34.6	13.2	14.7	9.7	10.6	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	28.3	25.7	12.3	10.6	9.0	7.7	ns
tpd	Delay	2-bit LUT	17.5	19.4	7.8	8.1	5.9	5.9	ns
tpd	Delay	3-bit LUT	21.7	24.2	9.4	9.8	7.1	7.1	ns
tpd	Delay	CNT/DLY Logic	50.6	42.5	22.0	18.6	15.5	13.3	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	54.2	46.3	23.4	20.1	16.5	14.3	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	108.9	--	49.2	--	34.0	--	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	108.1	--	48.9	--	33.9	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	108.4	108.2	49.0	48.9	34.0	33.9	ns
tw	Pulse Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	49.7	--	21.7	--	15.8	--	ns
tw	Pulse Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	49.1	--	21.2	--	15.5	ns
tw	Pulse Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	47.7	47.1	20.8	20.3	15.2	14.9	ns
tpd	Delay	DFF	29.6	22.1	12.9	9.7	9.5	7.3	ns
tpd	Delay	DFF nReset	--	28.9	--	12.3	--	9.0	ns
tpd	Delay	DFF nSet	--	35.1	--	14.8	--	10.7	ns
tpd	Delay	Filter	183.7	196.7	75.4	78.4	49.5	52.2	ns
tpd	Delay	PDLY 1 Cell Both Edge Delay	352.0	346.5	160.6	157.9	119.2	117.3	ns
tpd	Delay	PDLY 1 Cell Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 1 Cell Rising Edge Detect	39.1	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 1 Cell Falling Edge Detect	--	37.7	--	16.1	--	11.7	ns
tpd	Delay	PDLY 2 Cells Both Edge Delay	657.4	653.0	313.2	310.8	224.2	222.5	ns
tpd	Delay	PDLY 2 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 2 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 2 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns
tpd	Delay	PDLY 3 Cells Both Edge Delay	965.1	959.0	460.1	457.0	329.5	324.4	ns
tpd	Delay	PDLY 3 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 3 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 3 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns
tpd	Delay	PDLY 4 Cells Both Edge Delay	1271.5	1266.1	606.9	604.0	434.9	432.8	ns
tpd	Delay	PDLY 4 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 4 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 4 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
offset	25 kHz	auto	19	14	12	µs
offset	2 MHz	auto	7	4	4	µs
frequency settling time	25 kHz	auto	19	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Width	Width, 1 cell	mode:(any)edge detect, edge detect output	305	140	105	ns
Width	Width, 2 cell	mode:(any)edge detect, edge detect output	611	281	210	ns
Width	Width, 3 cell	mode:(any)edge detect, edge detect output	918	423	315	ns
Width	Width, 4 cell	mode:(any)edge detect, edge detect output	1225	564	420	ns
time1	Delay, 1 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 2 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 3 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 4 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	344	157	117	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	650	298	222	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	957	440	327	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1264	581	432	ns

5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

5.10 OSC Specifications

5.10.1 25 kHz RC Oscillator

Table 6. 25 kHz RC OSC frequency limits

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min., kHz	Max. kHz	Min., kHz	Max. kHz	Min., kHz	Max. kHz
1.8 V ±5%	24.442	25.552	23.613	26.037	23.190	26.916
3.3 V ±10%	24.453	25.542	23.566	26.044	23.194	26.945
5 V ±10%	24.207	26.109	23.417	26.220	23.086	26.907
2.5 V - 4.5 V	24.320	25.606	23.487	26.093	23.194	26.998
1.71 V….5.5 V	23.855	26.484	23.257	26.484	23.180	27.048

Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.23%	2.21%	-5.55%	4.15%	-7.24%	7.66%
3.3 V ±10%	-2.19%	2.17%	-5.73%	4.18%	-7.22%	7.78%
5 V ±10%	-3.17%	4.44%	-6.33%	4.88%	-7.66%	7.63%
2.5 V - 4.5 V	-2.72%	2.42%	-6.05%	4.37%	-7.22%	7.99%
1.71 V….5.5 V	-4.58%	5.93%	-6.97%	5.93%	-7.28%	8.19%

5.10.2 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min., MHz	Max. MHz	Min., MHz	Max. MHz	Min., MHz	Max. MHz
1.8 V ±5%	1.906	2.068	1.826	2.122	1.762	2.212
3.3 V ±10%	1.937	2.065	1.845	2.140	1.747	2.191
5 V ±10%	1.878	2.267	1.815	2.295	1.691	2.295
2.5 V - 4.5 V	1.873	2.114	1.786	2.187	1.741	2.191
1.71 V….5.5 V	1.690	2.377	1.623	2.394	1.623	2.394

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.71%	3.38%	-8.67%	6.10%	-11.90%	10.61%
3.3 V ±10%	-3.15%	3.26%	-7.74%	7.02%	-12.66%	9.56%
5 V ±10%	-6.10%	13.35%	-9.23%	14.73%	-15.45%	14.73%
2.5 V - 4.5 V	-6.36%	5.73%	-10.70%	9.37%	-12.95%	9.56%
1.71 V….5.5 V	-15.50%	18.84%	-18.85%	19.72%	-18.85%	19.72%

5.10.3 OSC Power On Delay

Table 10. Oscillators Power On delay at room temperature, RC OSC power setting, "Auto Power On"

Power Supply Range (VDD), V	2 MHz		2 MHz Fast start-up mode		25 kHz		25 kHz Fast start-up mode	
	Typ., ns	Max., ns	Typ., ns	Max., ns	Typ., µs	Max., µs	Typ., µs	Max., µs
1.71	108	376.4	60	306.7	0.14	41.10	0.43	41.33
1.80	95	351.6	53	291.3	0.12	41.31	0.41	41.23
1.89	83	332.0	46	278.5	0.11	41.04	0.40	41.18
2.30	53	279.0	30	244.0	0.07	41.18	0.34	41.28
2.50	44	265.1	24	234.9	0.06	41.12	0.33	40.93
2.70	38	254.3	21	227.9	0.05	41.24	2.78	41.17
3.00	31	243.5	17	220.5	0.04	41.30	8.73	41.06
3.30	26	235.8	14	215.4	0.04	41.31	11.30	41.19
3.60	23	230.5	13	211.8	0.03	41.19	16.55	41.40
4.20	16	224.3	7	207.8	0.02	41.27	19.65	41.31
4.50	14	223.1	5	206.9	0.41	41.27	19.64	41.20
5.00	12	230.1	5	211.3	1.25	41.25	19.60	41.19
5.50	10	228.1	4	212.0	1.32	41.25	19.54	40.99

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs (NMOS and PMOS, 1X and 2X)
- Push Pull Outputs (1X and 2X)
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- Pins 4 and 8 can be configured as bidirectional IO

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Combinational Logic Look Up Tables (LUTs – 4 total)

- Two 2-bit Lookup Tables
- Two 3-bit Lookup Tables

6.4 Combination Function Macrocells (7 total)

- Two Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay or Deglitch Filter

6.5 Delays/Counters (3 total)

- Three 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.6 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1 to 8 stage selectable outputs

6.7 Programmable Delay

- 140 ns/280 ns/420 ns/560 ns @ VDD = 3.3 V
- Includes Edge Detection function

6.8 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell

6.9 RC Oscillator

- 25 kHz or 2 MHz selectable frequency
- First Stage Clock pre-divider: OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1: selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.10 Power On Reset (POR)

7.0 I/O Pins

The SLG46108 has a total of multi-function I/O pins which can function as either a user defined Input. Refer to Section *2.0 Pin Description* for pin definitions.

Of the 6 user defined I/O pins on the SLG46108, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input.

7.2 Output Modes

Pins 3, 4, 6, 7, and 8 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 11. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <350:349>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <352:351>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 12. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <355:353>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 3 Pull Up/Down Resistor Value Selection	reg <357:356>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <358>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <359>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 13. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control (sig_PIN4_oe = 0)	reg <361:360>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Reserved
PIN 4 Mode Control (sig_PIN4_oe = 1)	reg <363:362>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 4 Pull Up/Down Resistor Value Selection	reg <365:364>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <366>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.4 PIN 6 Register Settings

Table 14. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	reg <370:368>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 6 Pull Up/Down Resistor Value Selection	reg <372:371>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Value Selection	reg <373>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <374>	0: 1X 1: 2X

7.4.5 PIN 7 Register Settings

Table 15. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control	reg <377:375>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 7 Pull Up/Down Resistor Value Selection	reg <379:378>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	reg <380>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 7 Driver Strength Selection	reg <381>	0: 1X 1: 2X

7.4.6 PIN 8 Register Settings

Table 16. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control (sig_PIN8_oe = 0)	reg <383:382>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Reserved
PIN 8 Mode Control (sig_PIN8_oe = 1)	reg <385:384>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 8 Pull Up/Down Resistor Value Selection	reg <387:386>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <388>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 GPI IO Structure

7.5.1 GPI IO Structure (for Pin 2)

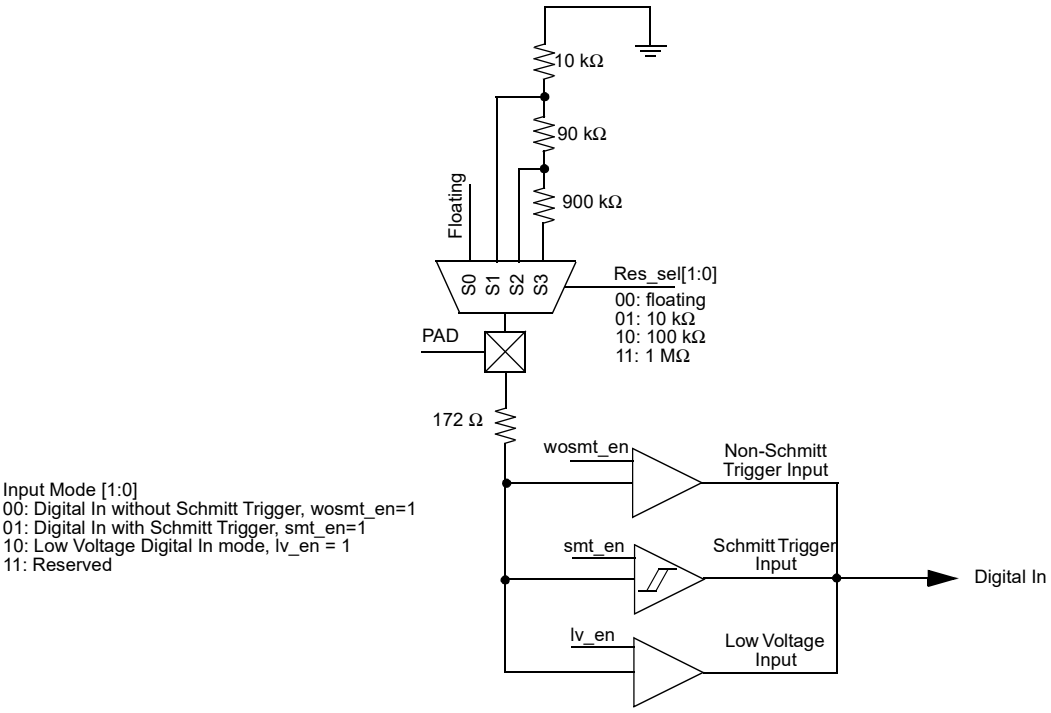


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pin 4, 8)

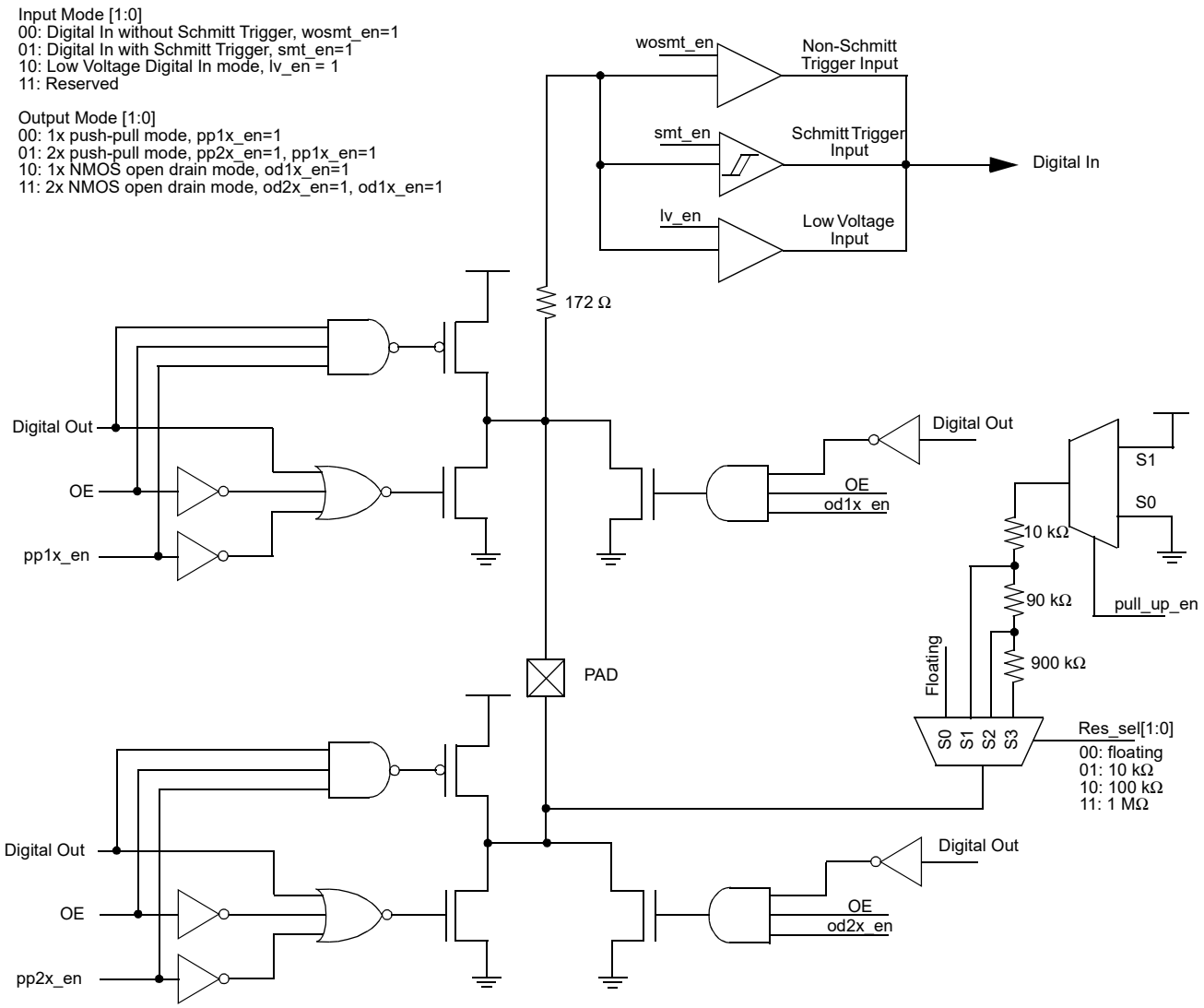


Figure 3. Matrix OE IO Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 3, 6, 7)

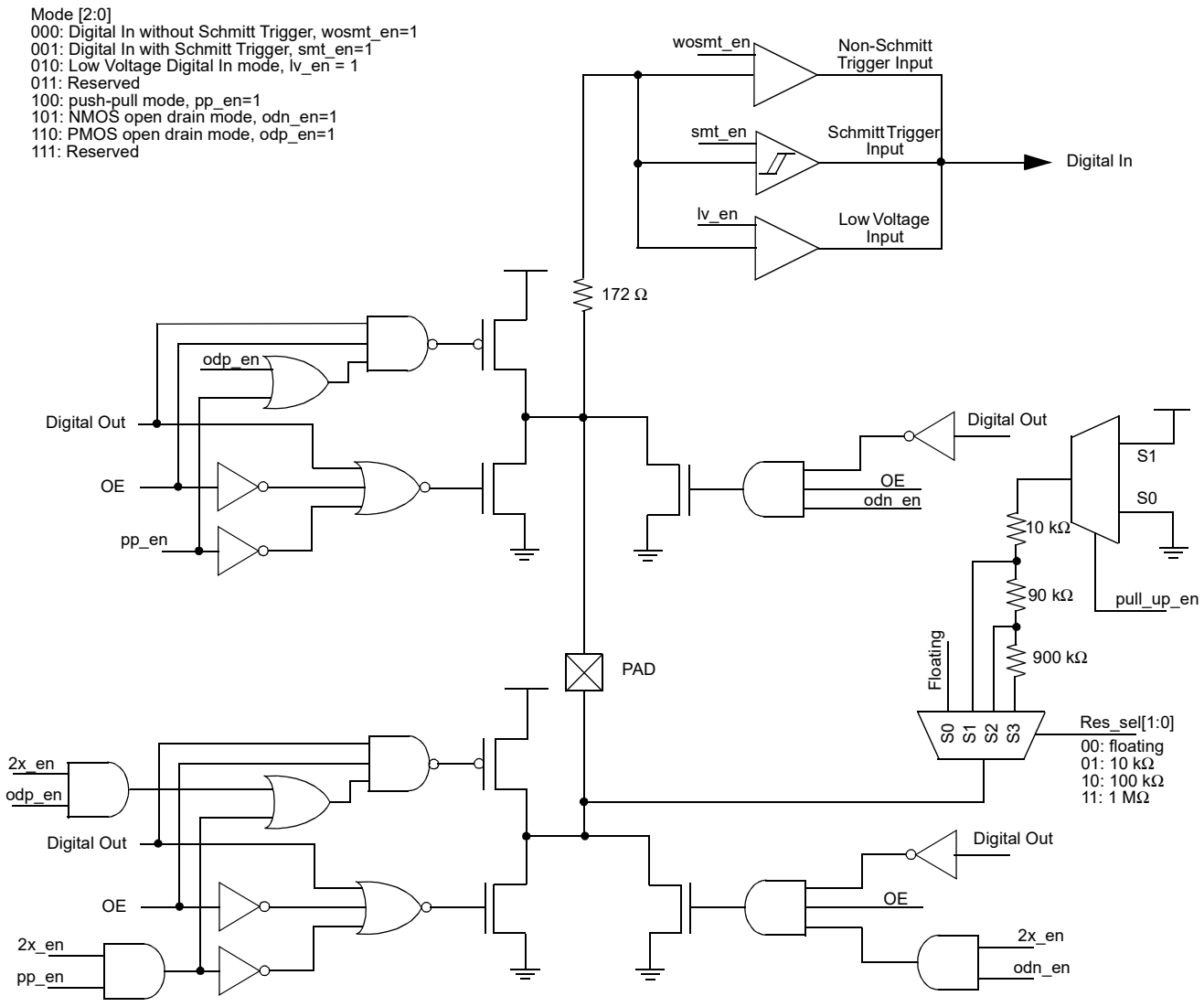


Figure 4. Register OE IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46108 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46108 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 463 register bits within the SLG46108 are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 40 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, other digital resources, and V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46108’s register table, see Section *14.0 Appendix A - SLG46108 Register Definition*.

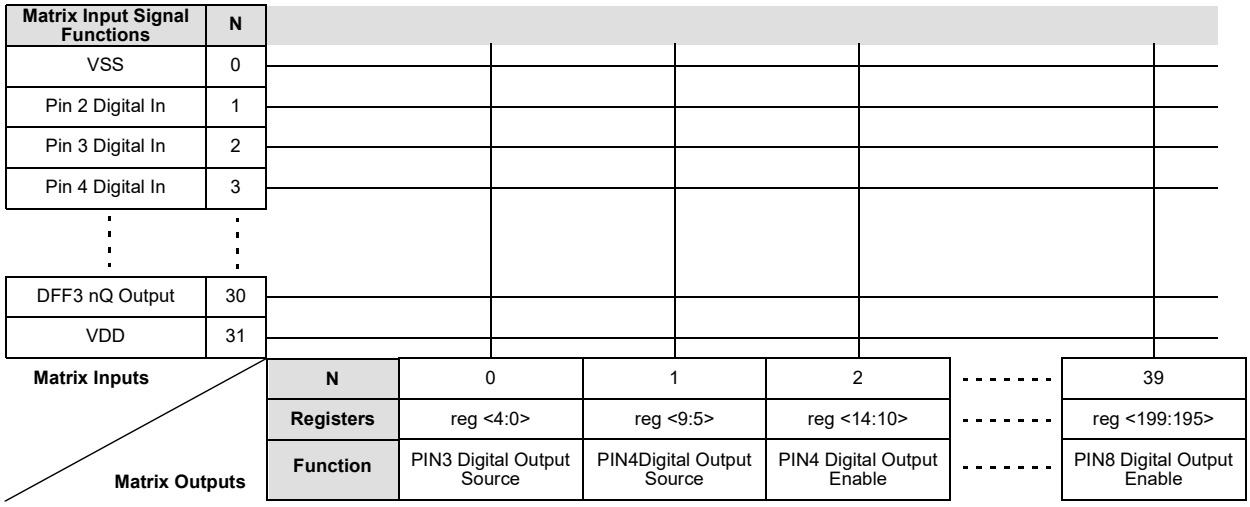


Figure 5. Connection Matrix

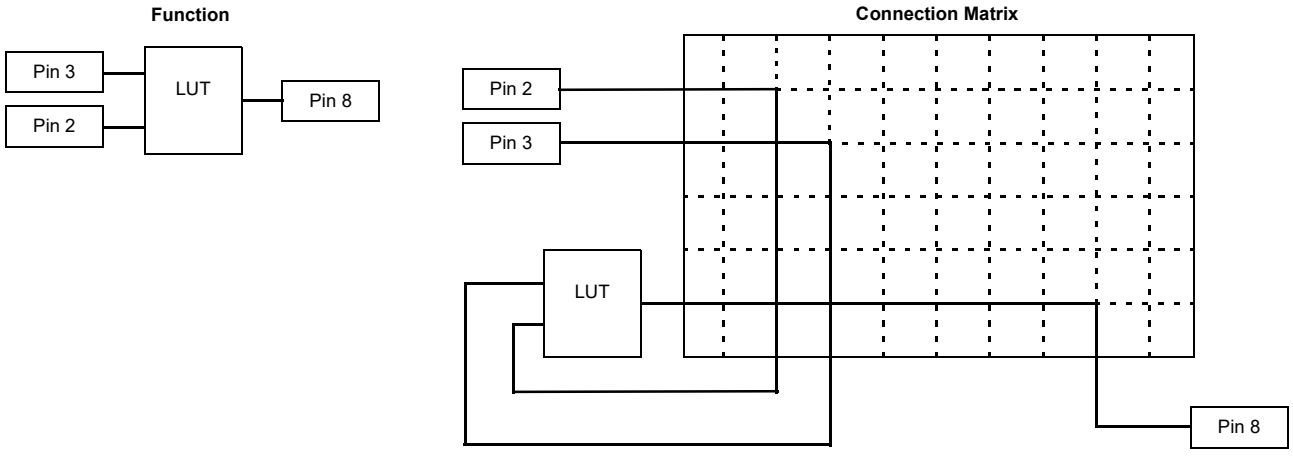


Figure 6. Connection Matrix Example

8.1 Matrix Input Table

Table 17. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	GND	0	0	0	0	0
1	Pin2 digital Input	0	0	0	0	1
2	Pin3 digital Input	0	0	0	1	0
3	Pin4 digital Input	0	0	0	1	1
4	LUT2_0 output (DFF/LATCH_0 output)	0	0	1	0	0
5	LUT2_1 output (DFF/LATCH_1 output)	0	0	1	0	1
6	LUT2_2 output	0	0	1	1	0
7	LUT2_3 output	0	0	1	1	1
8	LUT3_0 output (DFF/LATCH_2 output with nRST or nSET)	0	1	0	0	0
9	LUT3_1 output (DFF/LATCH_3 output with nRST or nSET)	0	1	0	0	1
10	LUT3_2 output	0	1	0	1	0
11	LUT3_3 output	0	1	0	1	1
12	LUT3_4 output (pipe delay ouput0)	0	1	1	0	0
13	Pipe delay ouput1	0	1	1	0	1
14	LUT4_0 output (CNT_DLY2 output (8 bit w/ ext CK, reset))	0	1	1	1	0
15	CNT_DLY0 output (8 bit w/ ext CK (shared with CNT_DLY1 ext CK), reset)	0	1	1	1	1
16	CNT_DLY1 output (8 bit w/ ext CK (shared with CNT_DLY0 ext CK), reset)	1	0	0	0	0
17	CNT_DLY3(8 bit) output	1	0	0	0	1
18	CNT_DLY3(8 bit) Edge detect output	1	0	0	1	0
19	Programmable delay with edge detector output (deglitch filter output)	1	0	0	1	1
20	internal oscillator output0 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	0	0
21	internal oscillator output1 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	0	1
22	GND	1	0	1	1	0
23	Resetb_core POR as matrix input	1	0	1	1	1
24	Pin6 digital Input	1	1	0	0	0
25	Pin7 digital Input	1	1	0	0	1
26	Pin8 digital Input	1	1	0	1	0
27	DFF0 nQ output	1	1	0	1	1
28	DFF1 nQ output	1	1	1	0	0
29	DFF2 nQ output	1	1	1	0	1
30	DFF3 nQ output	1	1	1	1	0
31	VDD	1	1	1	1	1

8.2 Matrix Output Table

Table 18. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <4:0>	Pin 3 digital out source	0
reg <9:5>	Pin 4 digital out source	1
reg <14:10>	Pin 4 output enable	2
reg <19:15>	in0 of LUT2_0 (Clock Input of DFF0)	3
reg <24:20>	in1 of LUT2_0 (Data Input of DFF0)	4
reg <29:25>	in0 of LUT2_1 (Clock Input of DFF1)	5
reg <34:30>	in1 of LUT2_1 (Data Input of DFF1)	6
reg <39:35>	in0 of LUT2_2	7
reg <44:40>	in1 of LUT2_2	8
reg <49:45>	in0 of LUT2_3	9
reg <54:50>	in1 of LUT2_3	10
reg <59:55>	in0 of LUT3_0 (Clock Input of DFF2 with nReset/nSet)	11
reg <64:60>	in1 of LUT3_0 (Data input of DFF2 with nReset/nSet)	12
reg <69:65>	in2 of LUT3_0 (nRST or nSET of DFF2 with nReset/nSet)	13
reg <74:70>	in0 of LUT3_1 (Clock Input of DFF3 with nReset/nSet)	14
reg <79:75>	in1 of LUT3_1 (Data input of DFF3 with nReset/nSet)	15
reg <84:80>	in2 of LUT3_1 (nRST or nSET of DFF3 with nReset/nSet)	16
reg <89:85>	in0 of LUT3_2	17
reg <94:90>	in1 of LUT3_2	18
reg <99:95>	in2 of LUT3_2	19
reg <104:100>	in0 of LUT3_3	20
reg <109:105>	in1 of LUT3_3	21
reg <114:110>	in2 of LUT3_3	22
reg <119:115>	in0 of LUT3_4 (Input of pipe delay)	23
reg <124:120>	in1 of LUT3_4 (nRST of pipe delay)	24
reg <129:125>	in2 of LUT3_4 (Clock of pipe delay)	25
reg <134:130>	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 external Clock)	26
reg <139:135>	in1 of LUT4_0 (Input for Delay2 or counter2 reset input)	27
reg <144:140>	in2 of LUT4_0 (Input for Counter2 FSM keep signal)	28
reg <149:145>	in3 of LUT4_0 (Input for Counter2 FSM up signal)	29
reg <154:150>	Input for Delay0 or Counter0 reset input	30
reg <159:155>	Input for Delay1 or Counter1 reset input	31
reg <164:160>	Input for Delay 0/1(Counter 0/1) external clock	32
reg <169:165>	Input for Delay3 or Counter3 reset input	33
reg <174:170>	Input for programmable delay (deglitch filter input)	34
reg <179:175>	Power down for osc. (higher priority) (high = power down).	35
reg <184:180>	Pin 6 digital out source	36
reg <189:185>	Pin 7 digital out source	37

Table 18. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <194:190>	Pin 8 digital out source	38
reg <199:195>	Pin 8 output enable	39

9.0 Combinatorial Logic

Combinatorial logic is supported via four Lookup Tables (LUTs) within the SLG46108. There are two 2-bit LUTs and two 3-bit LUTs. The device also includes six Combination Function Macrocells that can be used as LUTs. For more details, please see Section *10.0 Combination Function Macrocells*.

Inputs/Outputs for the four LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The two 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

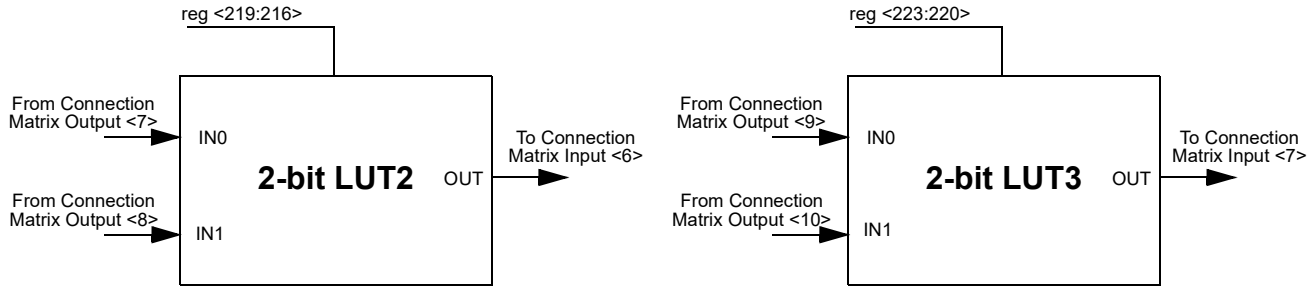


Figure 7. 2-bit LUTs

Table 19. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	reg <216>	LSB
0	1	reg <217>	
1	0	reg <218>	
1	1	reg <219>	MSB

Table 20. 2-bit LUT3 Truth Table

IN1	IN0	OUT	
0	0	reg <220>	LSB
0	1	reg <221>	
1	0	reg <222>	
1	1	reg <223>	MSB

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT2 is defined by reg <219:216>

2-Bit LUT3 is defined by reg <223:220>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 21. 2-bit LUT Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The two 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

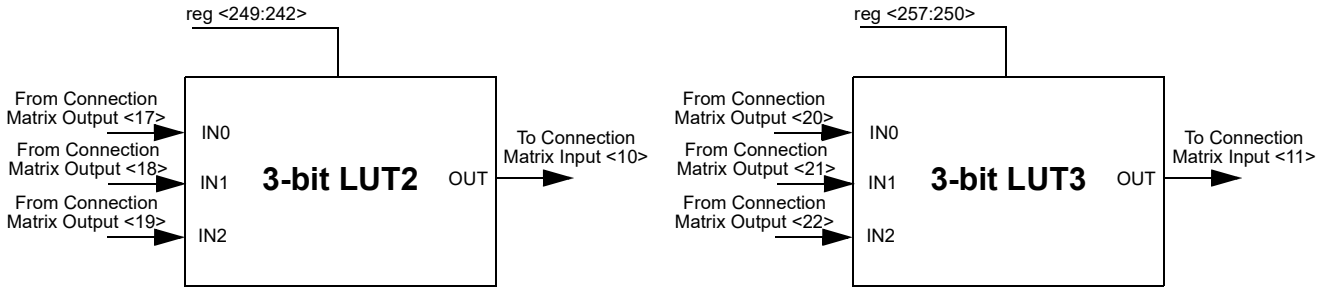


Figure 8. 3-bit LUTs

Table 22. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <242>	LSB
0	0	1	reg <243>	
0	1	0	reg <244>	
0	1	1	reg <245>	
1	0	0	reg <246>	
1	0	1	reg <247>	
1	1	0	reg <248>	
1	1	1	reg <249>	MSB

Table 23. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <250>	LSB
0	0	1	reg <251>	
0	1	0	reg <252>	
0	1	1	reg <253>	
1	0	0	reg <254>	
1	0	1	reg <255>	
1	1	0	reg <256>	
1	1	1	reg <257>	MSB

Each 3-bit LUT uses a 8-bit register signal to define their output functions:

3-Bit LUT2 is defined by reg <249:242>

3-Bit LUT3 is defined by reg <257:250>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 24. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.0 Combination Function Macrocells

The SLG46108 has seven combination function macrocells that can serve more than one logic or timing function. In six of these cases, they can serve as a Look Up Table (LUT), or as another logic or timing function. In the last case, it can serve as either a programmable delay or deglitch filter. See the list below for the functions that can be implemented in these macrocells:

- Two macrocells that can serve as either 2-bit LUTs or as DFF/Latch;
- Two macrocells that can serve as either 3-bit LUTs or as DFF/Latch;
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay;
- One macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter/Delay;
- One macrocell that can serve as either a Programmable Delay or as a Deglitch Filter.

Inputs/Outputs for the seven combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip Flop/Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and nQ outputs to the connection matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 1, then Q latches D value

10.1 2-Bit LUT or D Flip Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip Flop, with the output going back to the connection matrix.

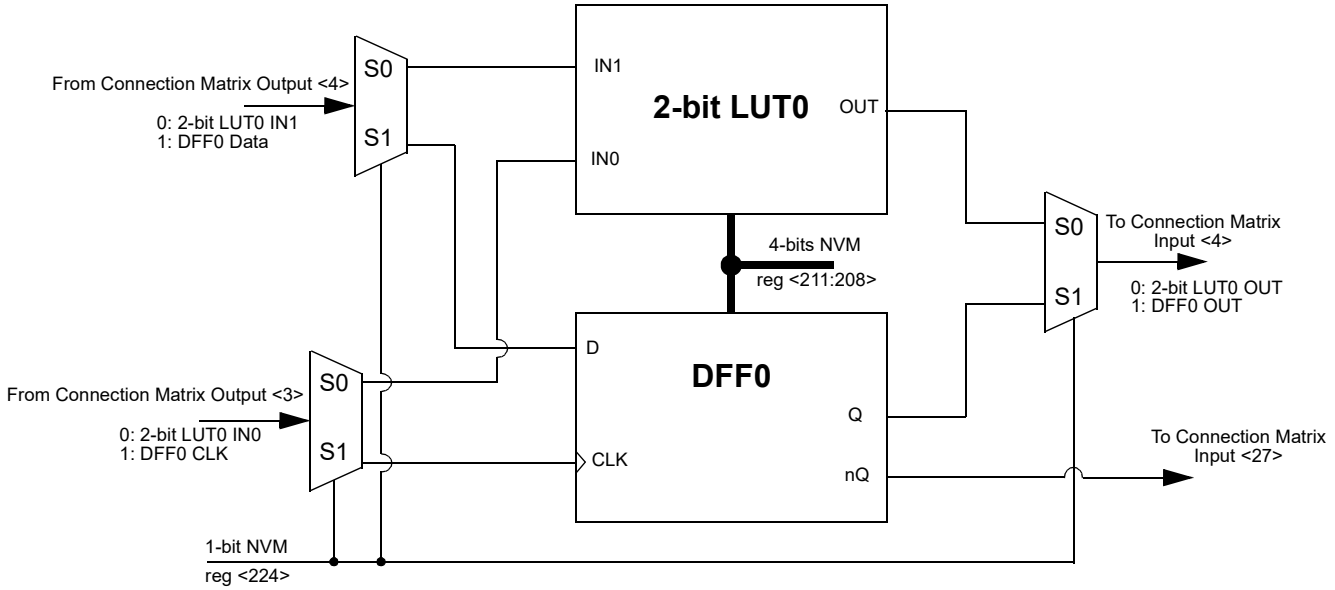


Figure 9. 2-bit LUT0 or DFF0

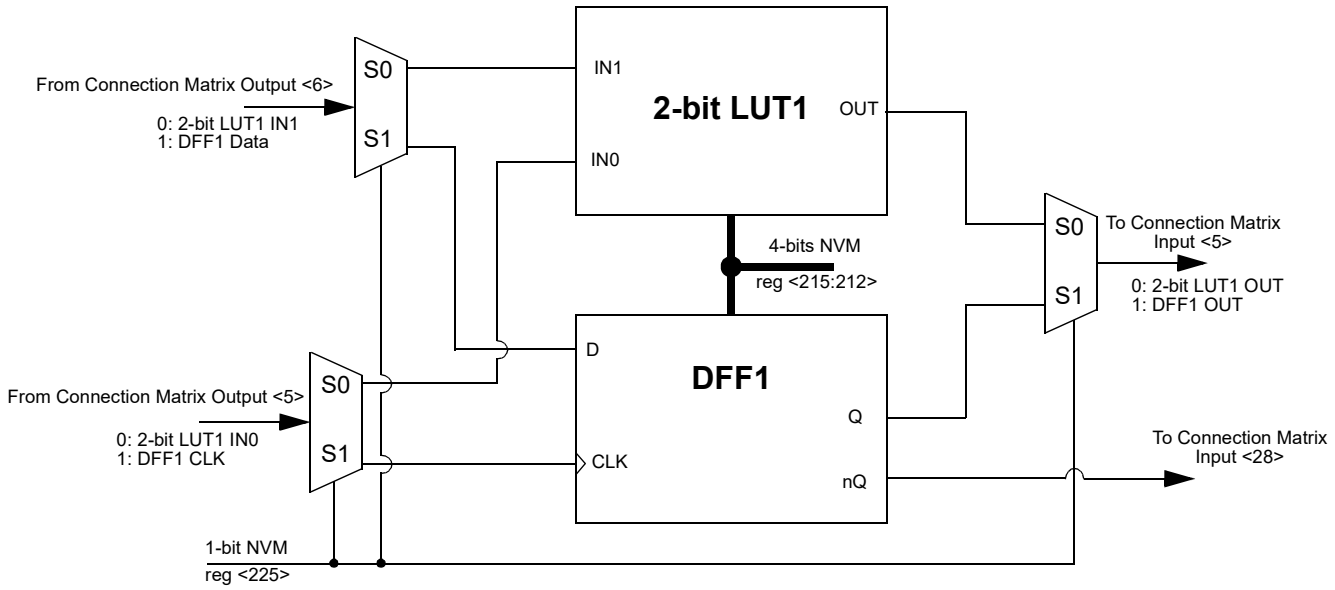


Figure 10. 2-bit LUT1 or DFF1

10.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 25. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	reg <208>	LSB
0	1	reg <209>	
1	0	reg <210>	
1	1	reg <211>	MSB

Table 26. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	reg <212>	LSB
0	1	reg <213>	
1	0	reg <214>	
1	1	reg <215>	MSB

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg <211:208>

2-Bit LUT1 is defined by reg <215:212>

10.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 27. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or Latch select	reg <208>	0: DFF function 1: Latch function
DFF0 initial polarity select	reg <210>	0: Low 1: High
LUT2_0 data	reg <211:208>	LUT2_0 data
LUT2_0 or DFF0 select	reg <224>	0: LUT2_0 1: DFF0

Table 28. DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or Latch select	reg <212>	0: DFF function 1: Latch function
DFF1 initial polarity select	reg <214>	0: Low 1: High
LUT2_1 data	reg <215:212>	LUT2_1 data
LUT2_1 or DFF1 select	reg <225>	0: LUT2_1 1: DFF1

10.2 3-Bit LUT or D Flip Flop with nSet/nReset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

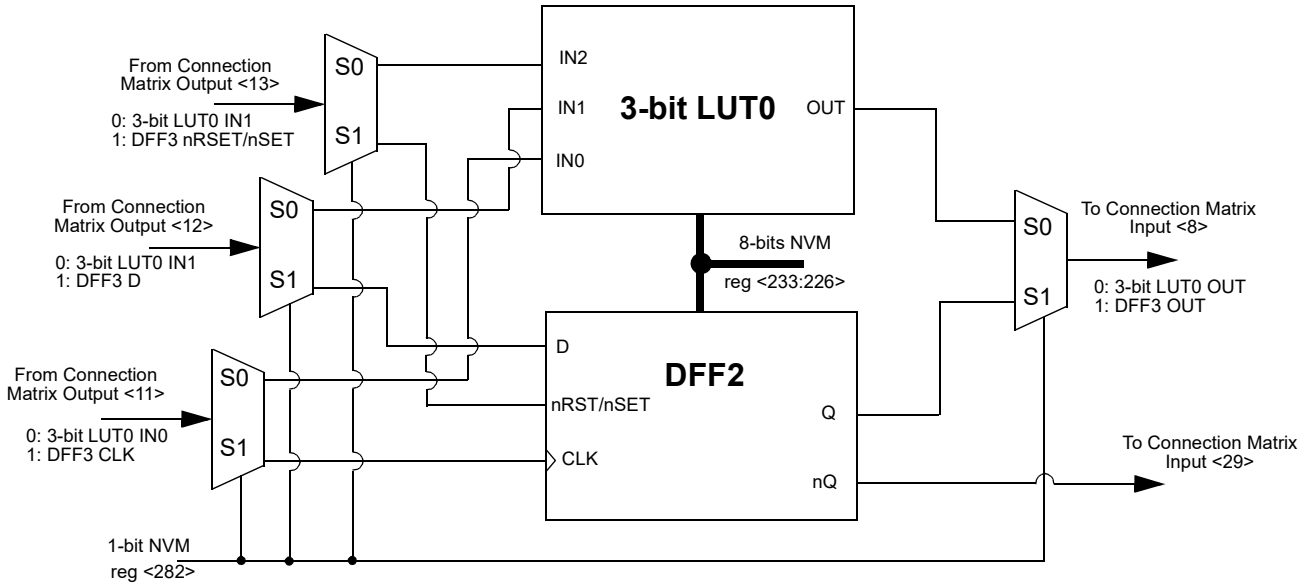


Figure 11. 3-bit LUT0 or DFF2

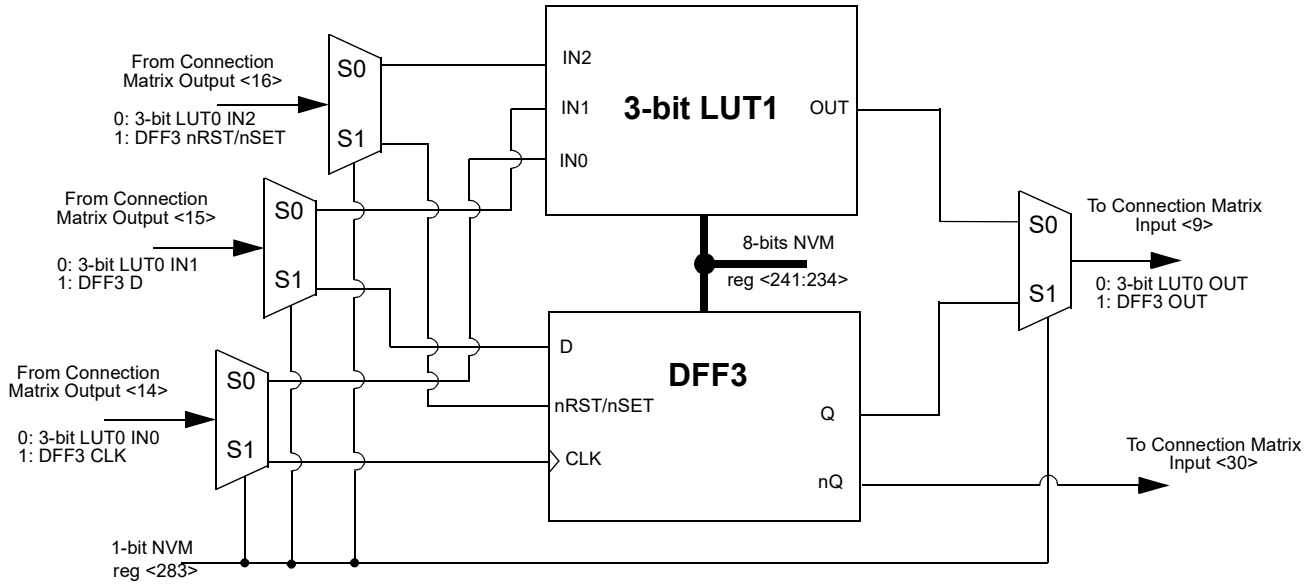


Figure 12. 3-bit LUT1 or DFF3

10.2.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 29. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <226>	LSB
0	0	1	reg <227>	
0	1	0	reg <228>	
0	1	1	reg <229>	
1	0	0	reg <230>	
1	0	1	reg <231>	
1	1	0	reg <232>	
1	1	1	reg <233>	MSB

Table 30. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <234>	LSB
0	0	1	reg <235>	
0	1	0	reg <236>	
0	1	1	reg <237>	
1	0	0	reg <238>	
1	0	1	reg <239>	
1	1	0	reg <240>	
1	1	1	reg <241>	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT2 is defined by reg <233:226>

3-Bit LUT3 is defined by reg <241:234>

10.2.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 31. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or Latch select	reg <226>	0: DFF function 1: Latch function
DFF2 nRST/nSET Select	reg <228>	1: nSET from matrix out 0: nRST from matrix out
DFF2 initial polarity select	reg <229>	0: Low 1: High
LUT3_0 data	reg <233:226>	LUT3_0 data
LUT3_0 or DFF2 select	reg <266>	0: LUT3_0 1: DFF2

Table 32. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or Latch Select	reg <234>	0: DFF function 1: Latch function
DFF3 nRST/nSET Select	reg <236>	1: nSET from matrix out 0: nRST from matrix out
DFF3 initial polarity select	reg <237>	0: Low 1: High
LUT3_1 data	reg <241:234>	LUT3_1 data
LUT3_1 or DFF3 select	reg <267>	0: LUT3_1 1: DFF3

10.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as an 8-stage pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CK) and Reset (nRST). The pipe delay cell is built from D Flip-Flop logic cells that provide the two user selectable output options (OUT0 and OUT1). The DFF cells are tied in series where the output of each delay cell goes to the next DFF cell. There are delay output points for each set of the OUT0 and OUT1 outputs to a 3-input mux that is controlled by reg <260:258> for OUT0 and reg <263:261> for OUT1. The 3-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46108 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46108). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

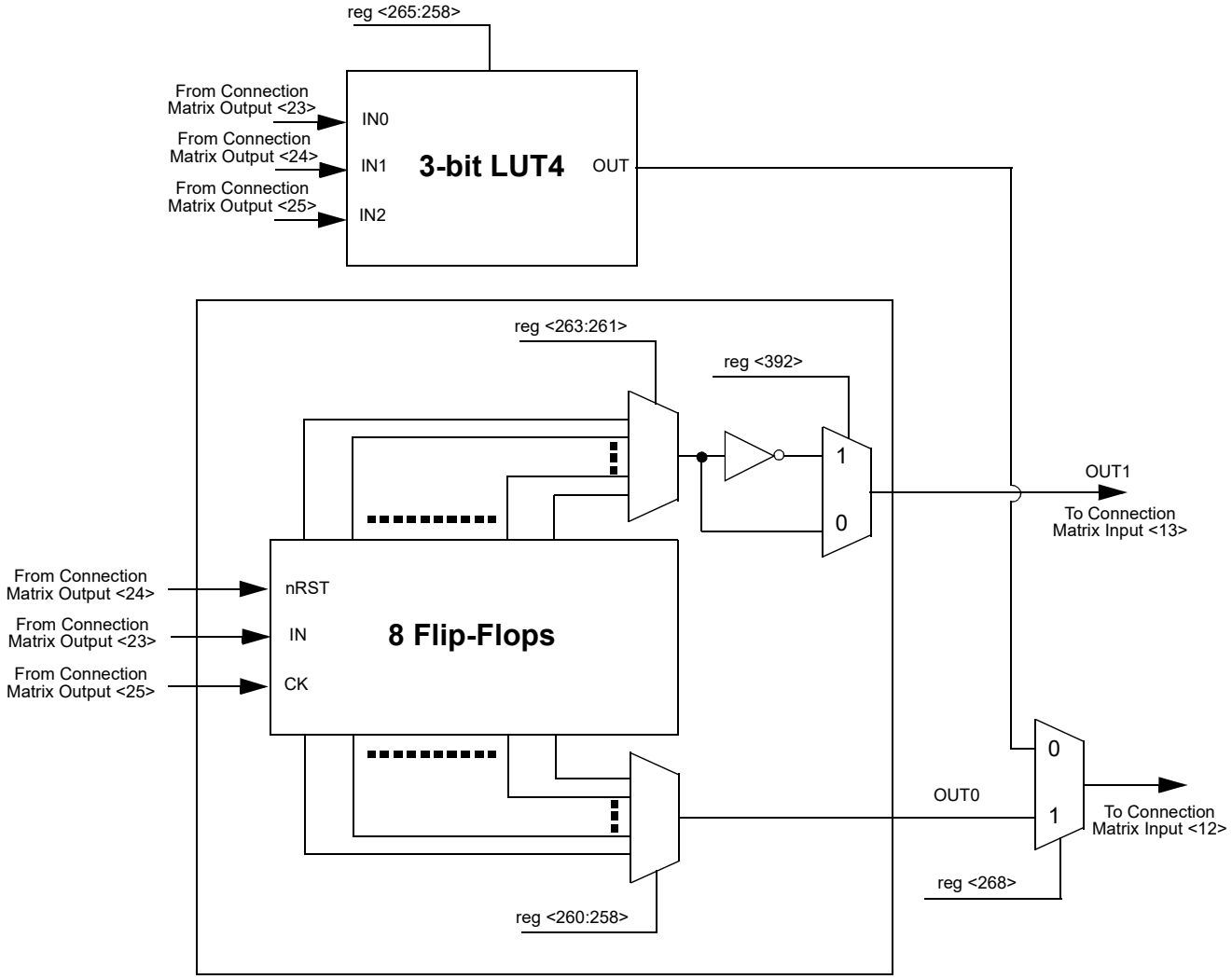


Figure 13. 3-bit LUT4 or Pipe Delay

10.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 33. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <258>	LSB
0	0	1	reg <259>	
0	1	0	reg <260>	
0	1	1	reg <261>	
1	0	0	reg <262>	
1	0	1	reg <263>	
1	1	0	reg <264>	
1	1	1	reg <265>	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT4 is defined by reg <265:258>

10.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 34. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg <260:258>	data (pipe number)
OUT1 select	reg <263:261>	data (pipe number)
LUT3_4 or pipe delay output select	reg <268>	0: LUT3_4 1: pipe delay

10.4 4-Bit LUT or 8-Bit Counter / Delay Macrocells

There is one macrocell that can serve as either a 4-bit LUT or as a Counter / Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the clock (CLK) and reset (DLY_IN/Reset_IN) inputs for the counter/delay, with the output going back to the connection matrix. This macrocell has an optional Finale State Machine (FSM) function. It has two additional matrix inputs for Up and Keep to support FSM functionality. The counter is counting down by default. Logic 1 on input Up reverses counting. Logic 1 on input Keep pauses counting

Note: Counters initialize with counter data after POR.

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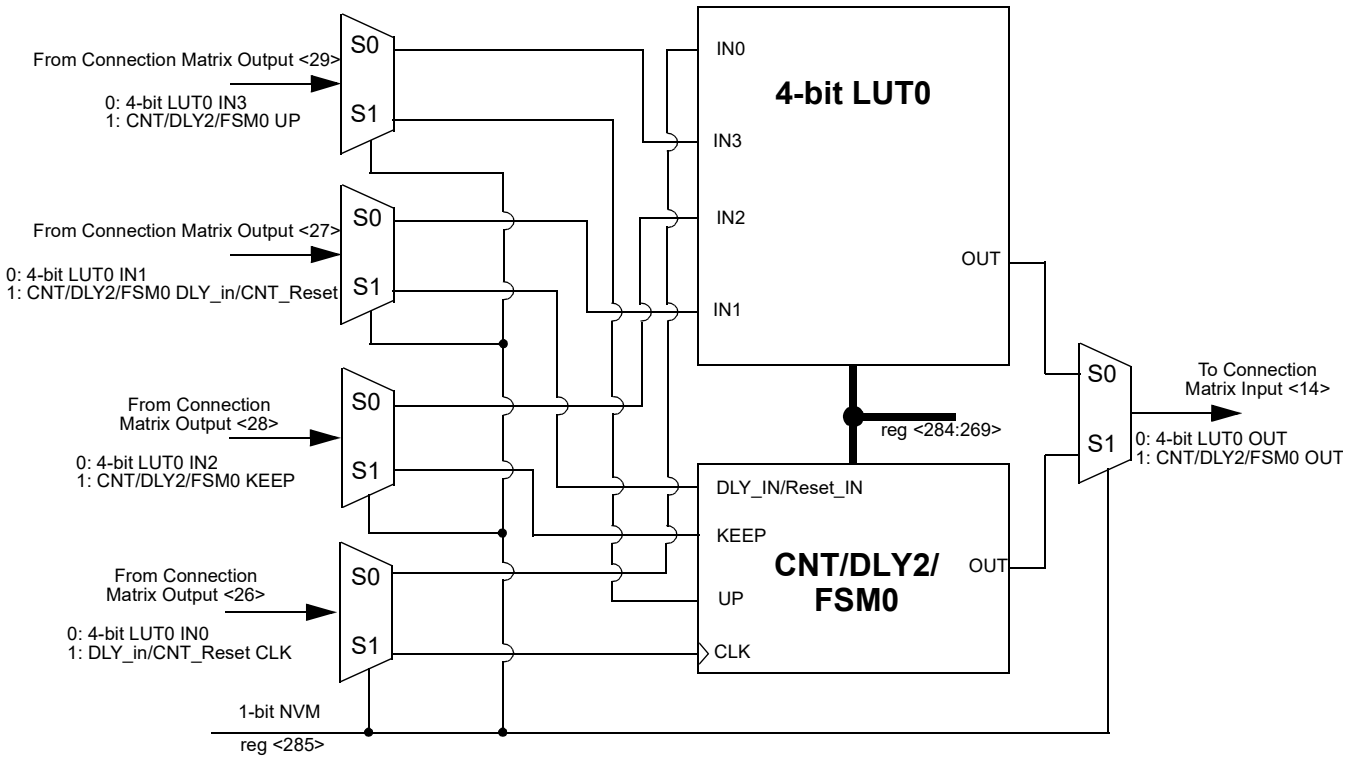


Figure 14. 4-bit LUT1 or CNT/DLY2/FSM0

10.4.1 Counter Mode

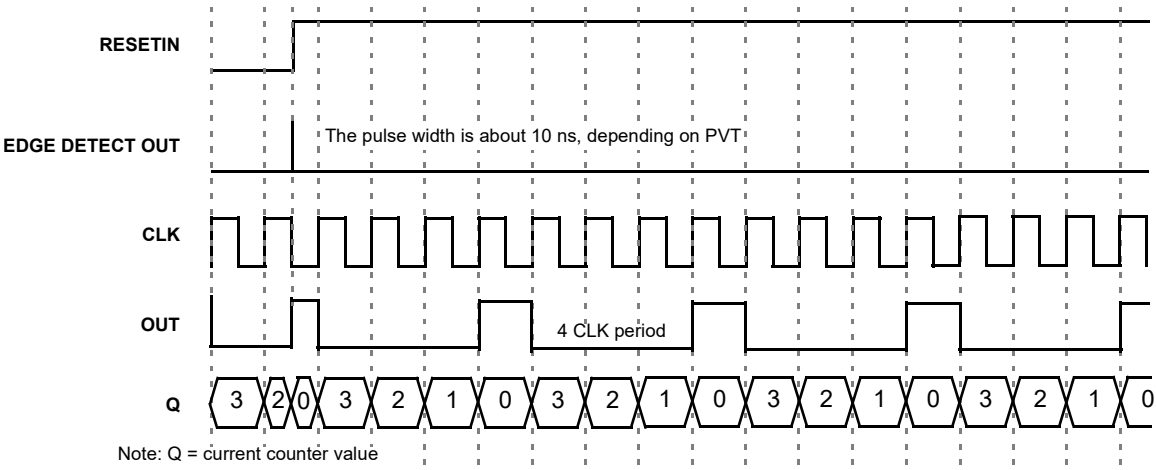


Figure 15. Timing (reset rising edge mode, oscillator is forced on) for count data = 3

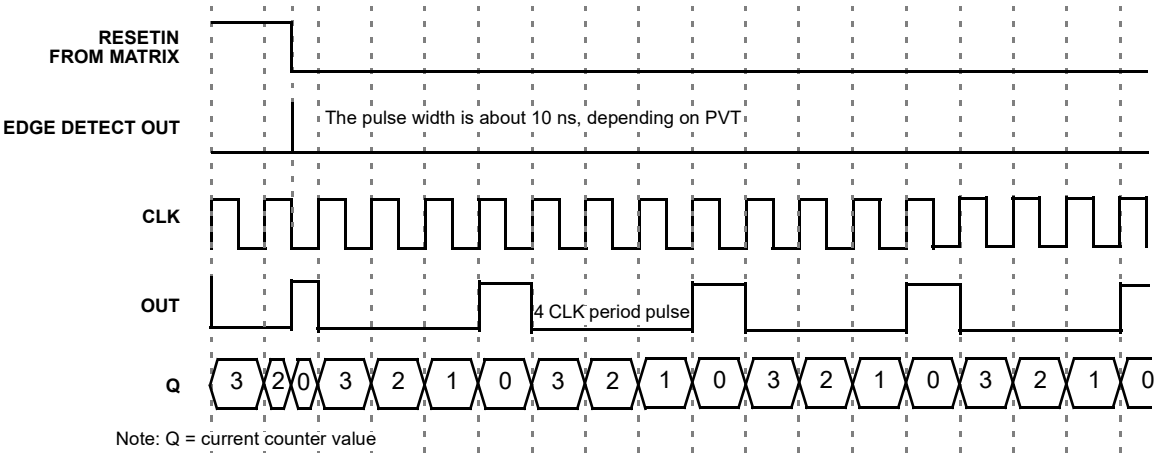


Figure 16. Timing (reset falling edge mode, oscillator is forced on) for count data = 3

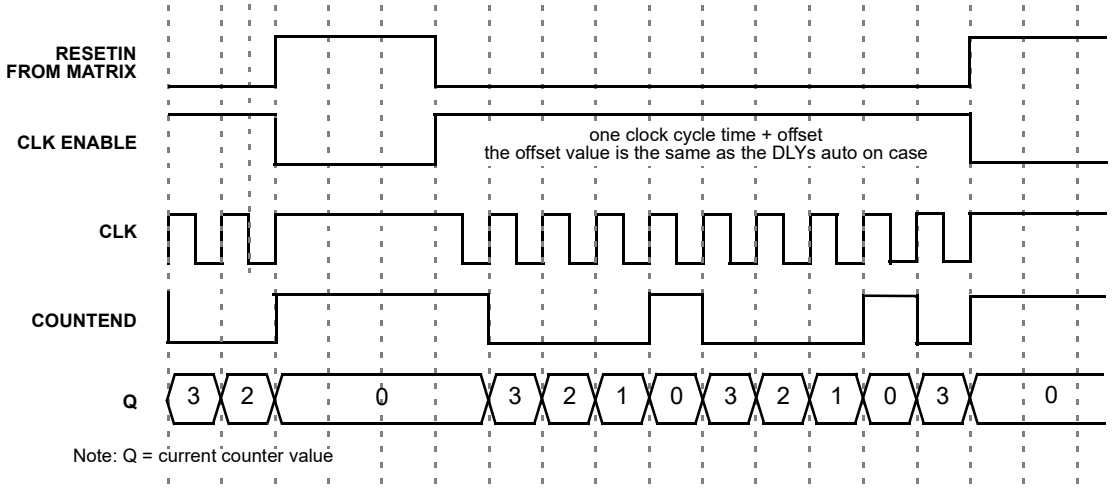


Figure 17. Timing (reset high level mode, oscillator is auto powered on (controlled by reset)) for count data = 3

10.4.2 FSM Mode

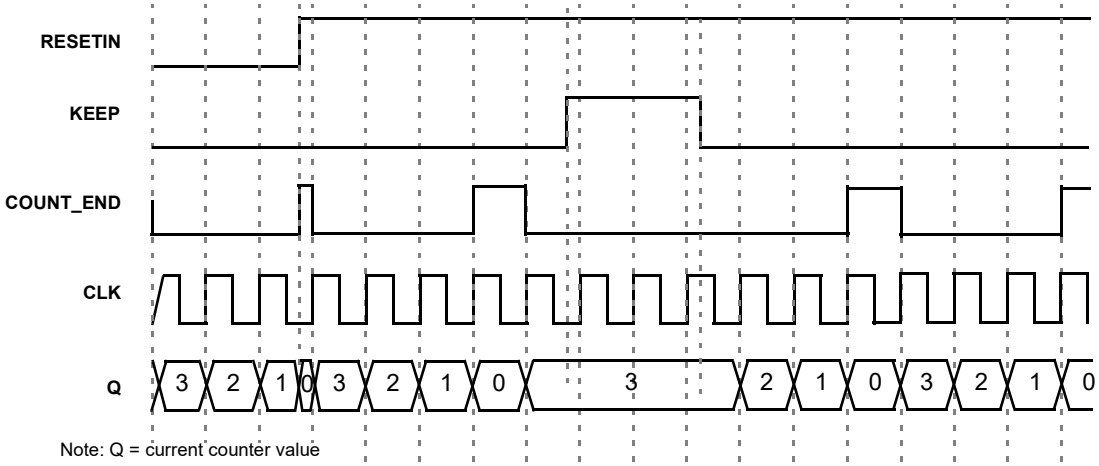


Figure 18. Timing (reset rising edge mode, oscillator is forced on, UP = 0) for count data = 3

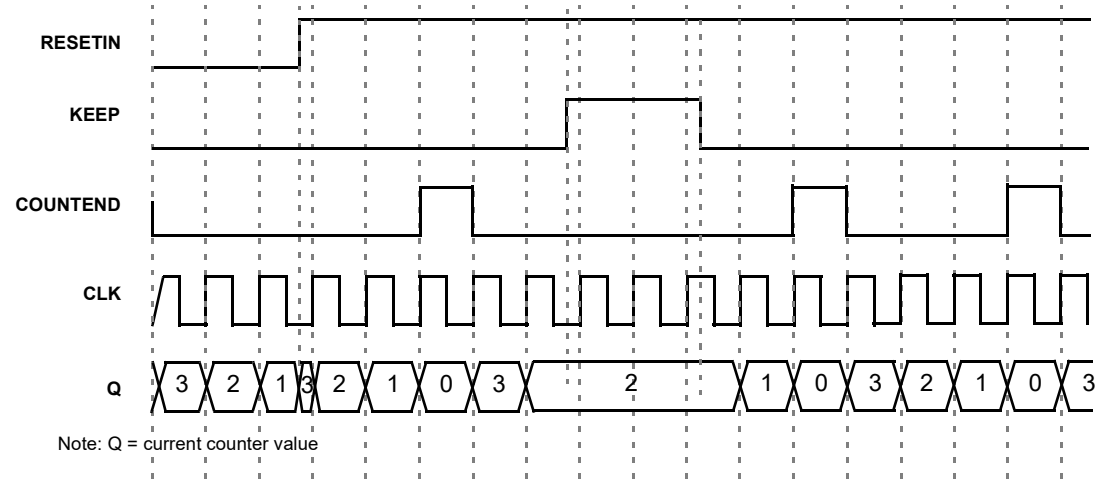


Figure 19. Timing (set rising edge mode, oscillator is forced on, UP = 0) for count data = 3

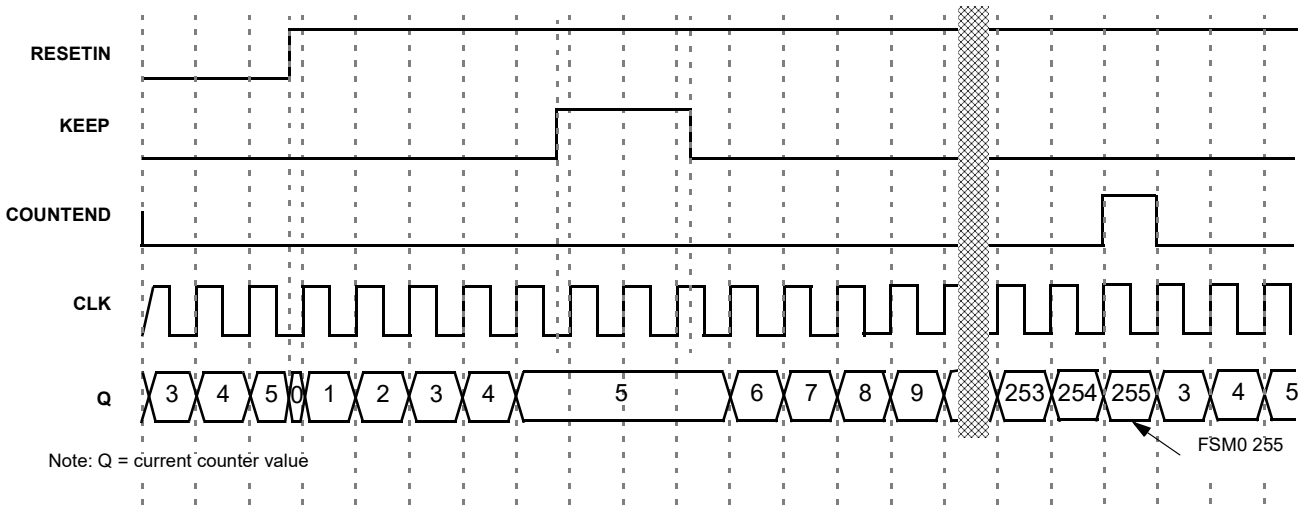


Figure 20. Timing (reset rising edge mode, oscillator is forced on, UP = 1) for count data = 3

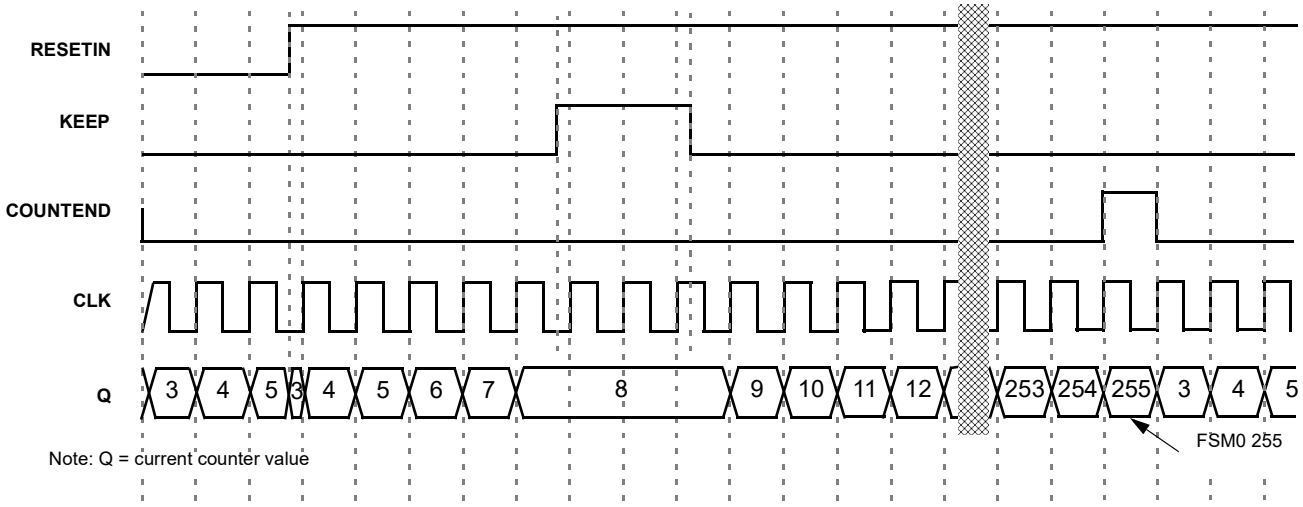


Figure 21. Timing (set rising edge mode, oscillator is forced on, UP = 1) for count data = 3

10.4.3 4-Bit LUT or 8-Bit Counter / Delay Macrocell Used as 4-Bit LUT

Table 35. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	reg <269>	LSB
0	0	0	1	reg <270>	
0	0	1	0	reg <271>	
0	0	1	1	reg <272>	
0	1	0	0	reg <273>	
0	1	0	1	reg <274>	
0	1	1	0	reg <275>	
0	1	1	1	reg <276>	
1	0	0	0	reg <277>	
1	0	0	1	reg <278>	
1	0	1	0	reg <279>	
1	0	1	1	reg <280>	
1	1	0	0	reg <281>	
1	1	0	1	reg <282>	
1	1	1	0	reg <283>	
1	1	1	1	reg <284>	MSB

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg <284:269>

Table 36. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

10.4.4 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 37. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay2 Mode Selection	reg <269>	0: Delay Mode 1: Counter Mode
Counter/delay2 Clock Source Select	reg <272:270>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter1 Overflow
Counter/delay2 Control Data	reg <280:273>	1 – 255 (delay time = (counter control data +1) /freq)
Delay2 Mode Select or asynchronous counter reset	reg <282:281>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
LUT4_0 or Counter2 select	reg <285>	0: LUT4_0 1: Counter2

10.5 Programmable Delay / Edge Detector (PDLY/ Edge Detector)

The SLG46108 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (width/time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

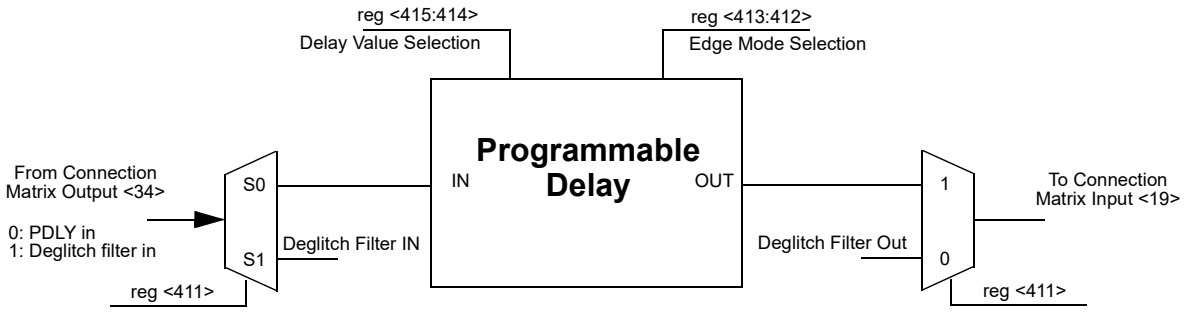


Figure 22. Programmable Delay

10.5.1 Programmable Delay Timing Diagram - Edge Detector Output

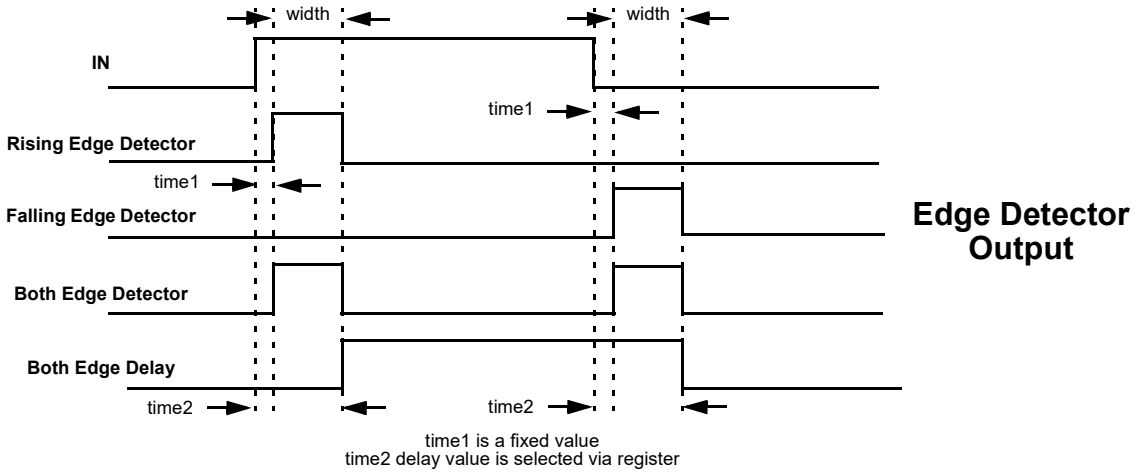


Figure 23. Edge Detector Output

10.5.2 Programmable Delay Register Settings

Table 38. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable delay or filter output select	reg <411>	0: programmable delay output 1: filter output
Select the edge mode of programmable delay & edge detector	reg <413:412>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (VDD = 3.3 V, typical condition)	reg <415:414>	00: 140 ns 01: 280 ns 10: 420 ns 11: 560 ns

10.6 Deglitch Filter

The SLG46108 has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter.The typical filtered pulse width is shown in *Table 5. Typical Pulse Width Performance*.

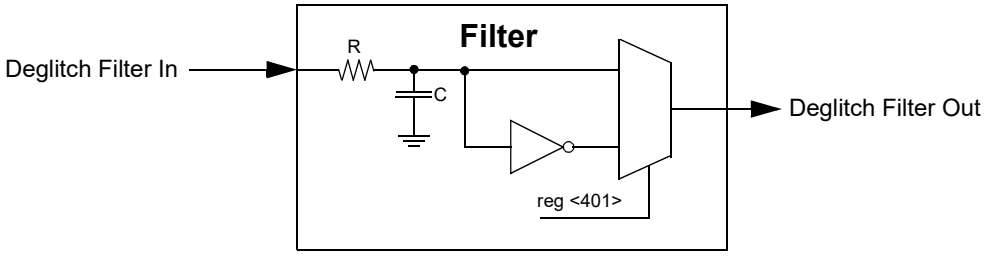


Figure 24. Deglitch Filter

11.0 Counters/Delay Generators (CNT/DLY)

There are three configurable counters/delay generators in the SLG46108. The three counters/delay generators (CNT/DLY 0, 1, 3) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

Two of the counter/delay generator macrocells (CNT/DLY0 and CNT/DLY1) have two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. One of the counter/delay generator macrocells (CNT/DLY3) has one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

Note that there is also one Combination Function Macrocells that can implement either 4-bit LUTs or 8-bit counter / delays. For more information please see Section *10.4 4-Bit LUT or 8-Bit Counter / Delay Macrocells.*

Note: Counters initialize with counter data after POR.

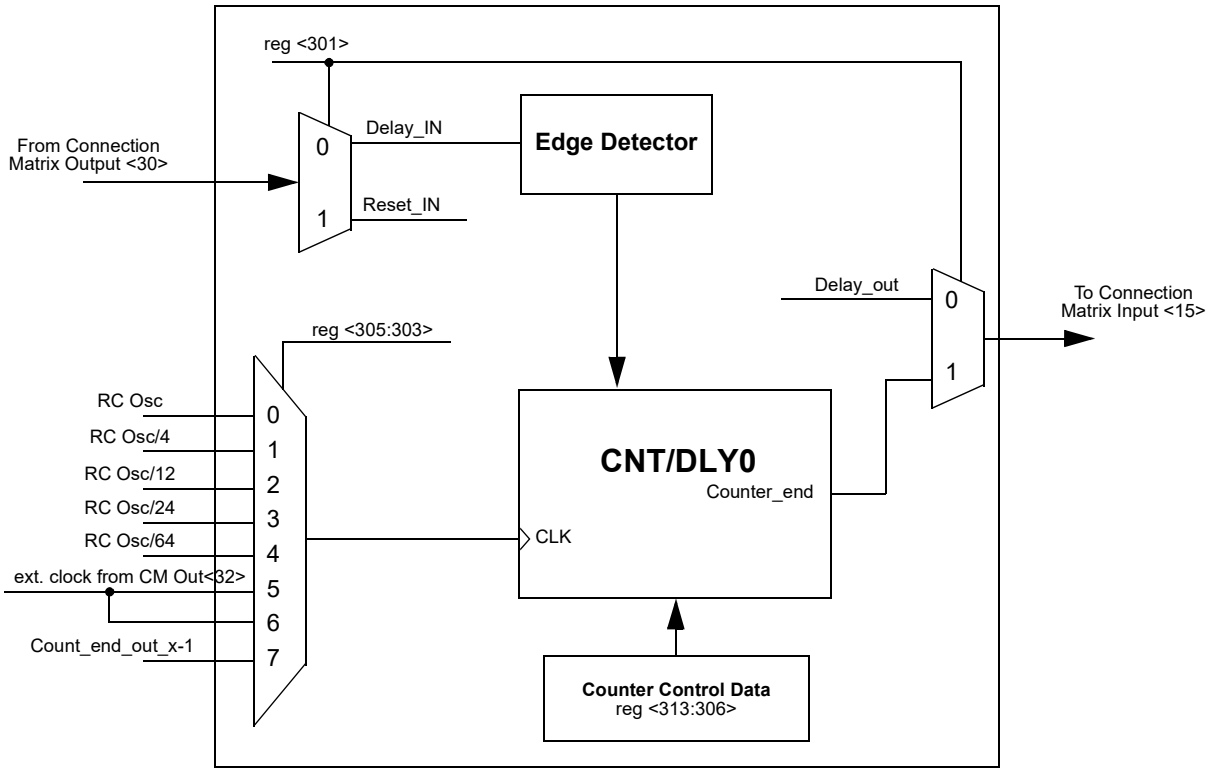


Figure 25. CNT/DLY0

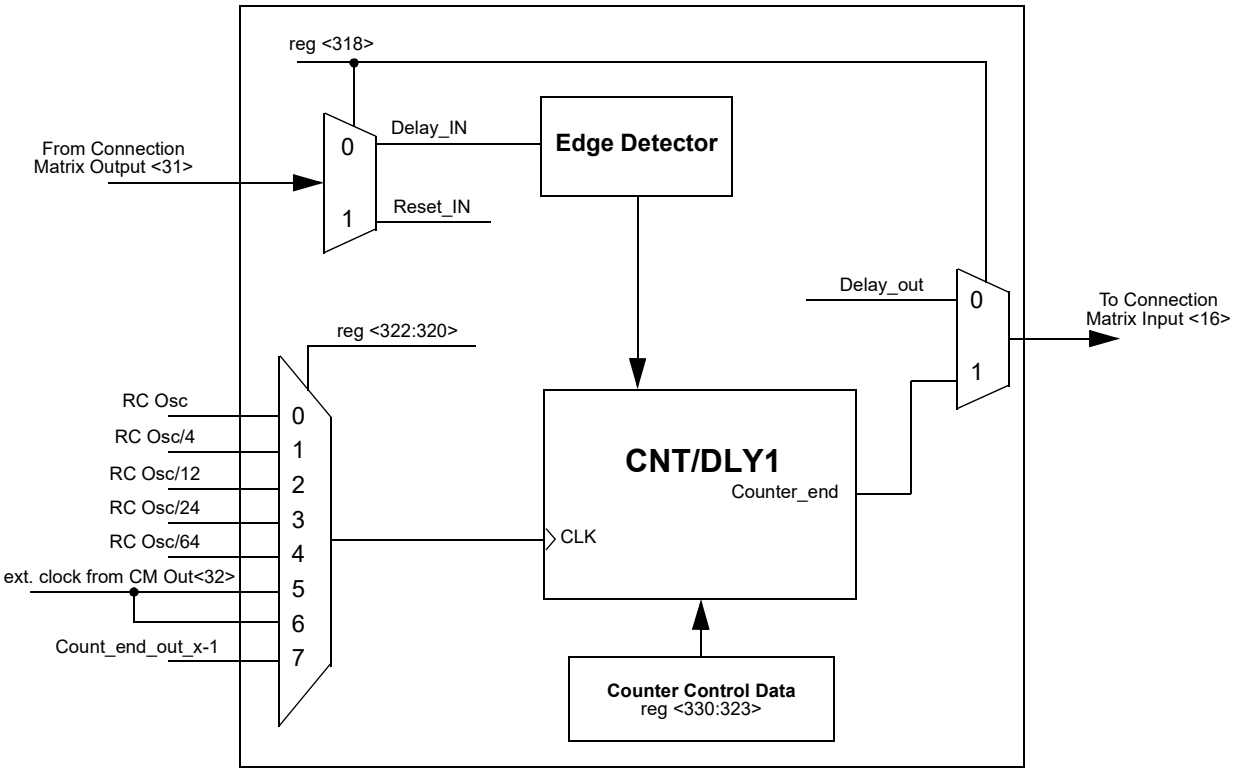


Figure 26. CNT/DLY1

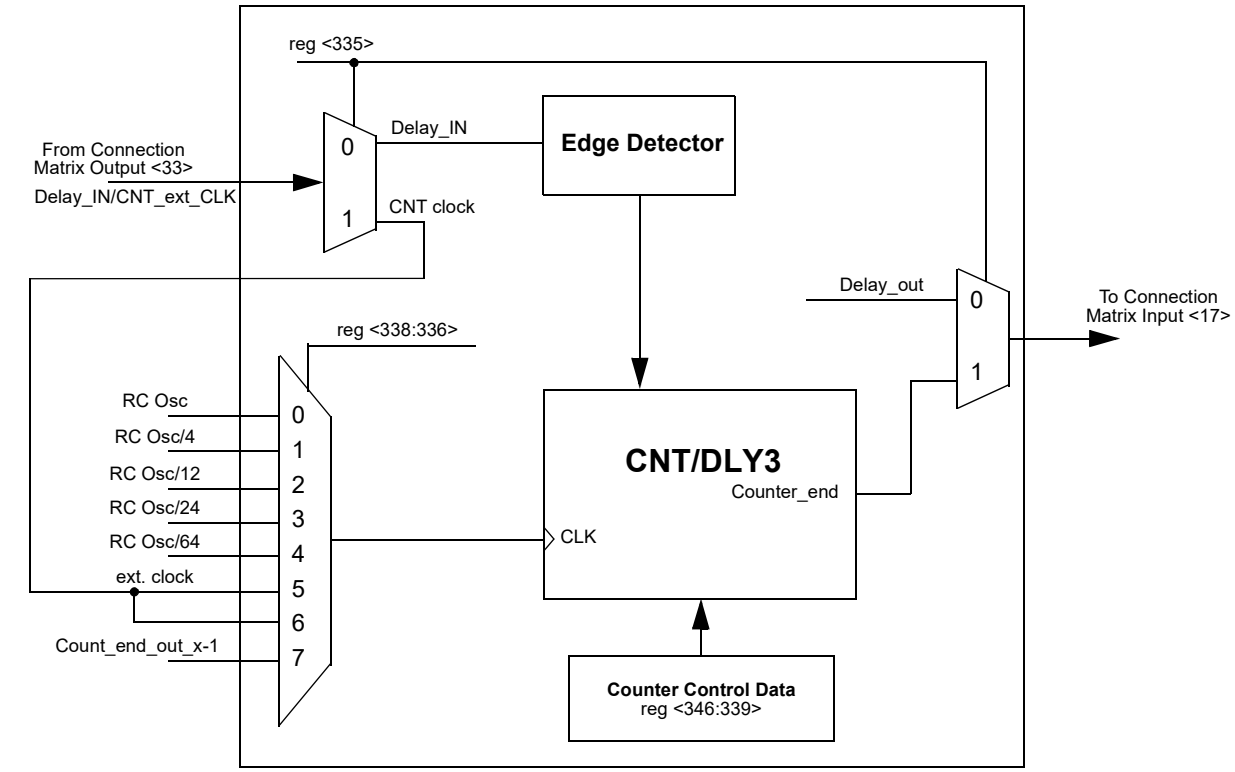


Figure 27. CNT/DLY3

11.1 CNT/DLY0 Register Settings

Table 39. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg <301>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select	reg <305:303>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter3 Overflow
Counter0 Control Data/Delay0 Time Control	reg <313:306>	1-255: (delay time = (counter control data +1) /freq)
Delay0 Mode Select or asynchronous counter reset	reg <315:314>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

11.2 CNT/DLY1 Register Settings

Table 40. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg <318>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source Select (external clock is only for counter mode)	reg <322:320>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
Counter1 Control Data/Delay1 Time Control	reg <330:323>	1-255: (delay time = (counter control data +1) /freq)
Delay1 Mode Select or asynchronous counter reset	reg <332:331>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

11.3 CNT/DLY3 Register Settings

Table 41. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Mode Select	reg <335>	0: Delay Mode 1: Counter Mode
Counter/Delay3 Clock Source Select (external clock is only for counter mode)	reg <338:336>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter2 Overflow
Counter3 Control Data/Delay3 Time Control	reg <346:339>	1-255: (delay time = (counter control data +1) /freq)
Delay3 Mode Select	reg <348:347>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.0 RC Oscillator (RC OSC)

12.1 RC Oscillator Overview

The SLG46108 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. When using the chip internal RC OSC, a choice is available to “Force Power On”, meaning that the RC OSC will always run, or “Auto Power On”, meaning that the RC OSC will have an associated startup and settling time associated with it (offset). *Figure 28* and *Figure 29* show maximum power on delay vs. VDD.

Note: RC OSC power setting: "Auto Power On”.

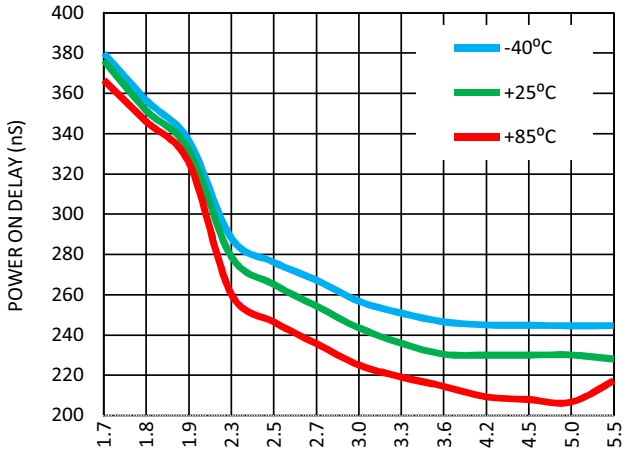


Figure 28. Maximum Power On Delay vs. VDD, RC OSC = 2 MHz.

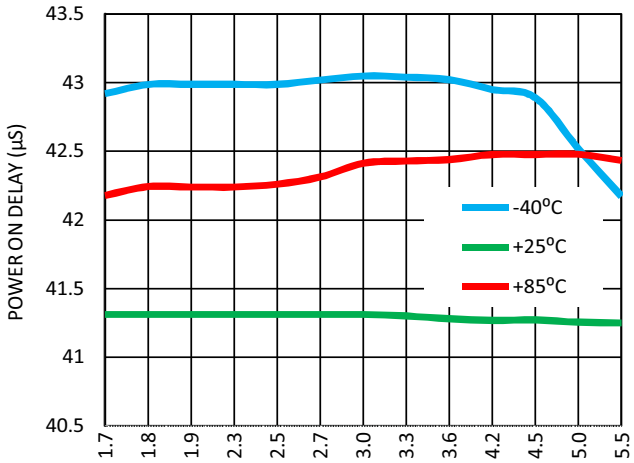


Figure 29. Maximum Power On Delay vs. VDD, RC OSC = 25 kHz.

The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (Pin 8). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider (pre-divider) allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines <20> and <21>. See *Figure 30* below for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

12.2 RC OSC Block Diagram

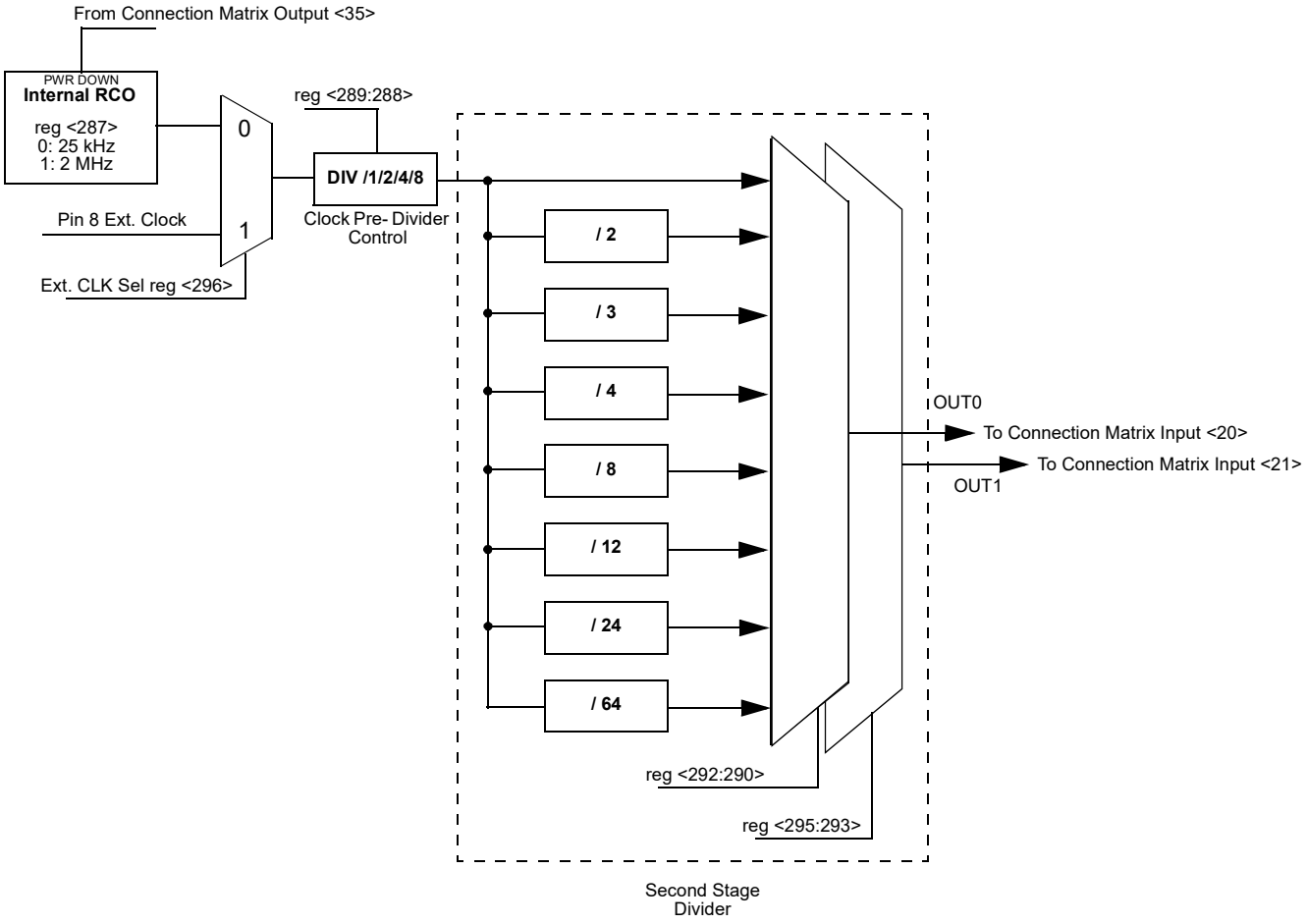


Figure 30. RC OSC Block Diagram

12.3 Oscillator Accuracy

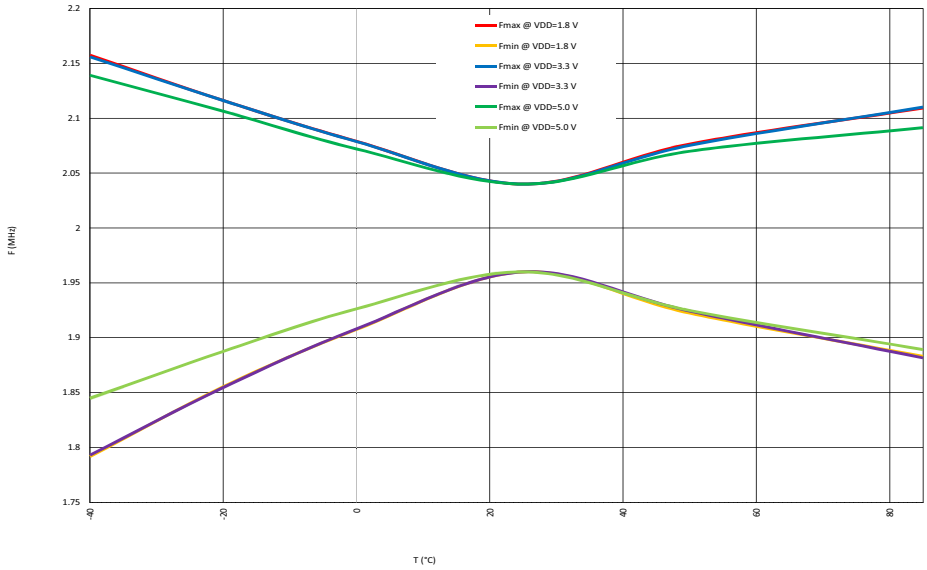


Figure 31. RC Oscillator Frequency vs. Temperature, RC OSC = 2 MHz

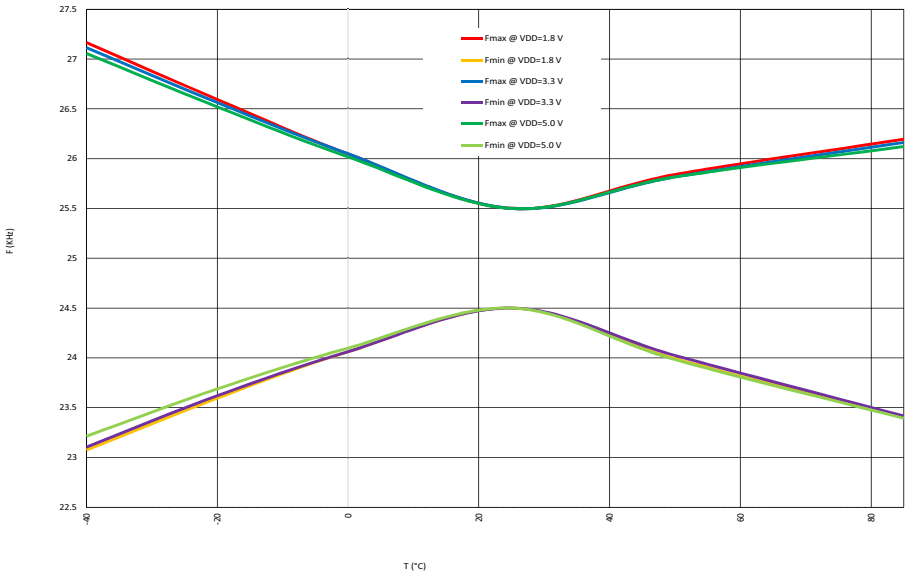


Figure 32. RC Oscillator Frequency vs. Temperature, RC OSC = 25 kHz

13.0 Power On Reset (POR)

The SLG46108 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins.

13.1 General Operation

To start the POR sequence in the SLG46108, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46108 is 1.71 V – 5.5 V (1.8 V ±5% - 5 V±10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46108 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

The SLG46108 is guaranteed to be powered down and non-operational when the VDD voltage (voltage on PIN1) is less than 0.6 V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1. There is a 0.5 V margin due to forward drop voltage of the ESD protection diodes.

Note 2. The Power_ON threshold can vary by PVT, but typically it is 1.6 V.

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the VDD, this rule also applies to the case when the chip is powered on.

13.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 33*.

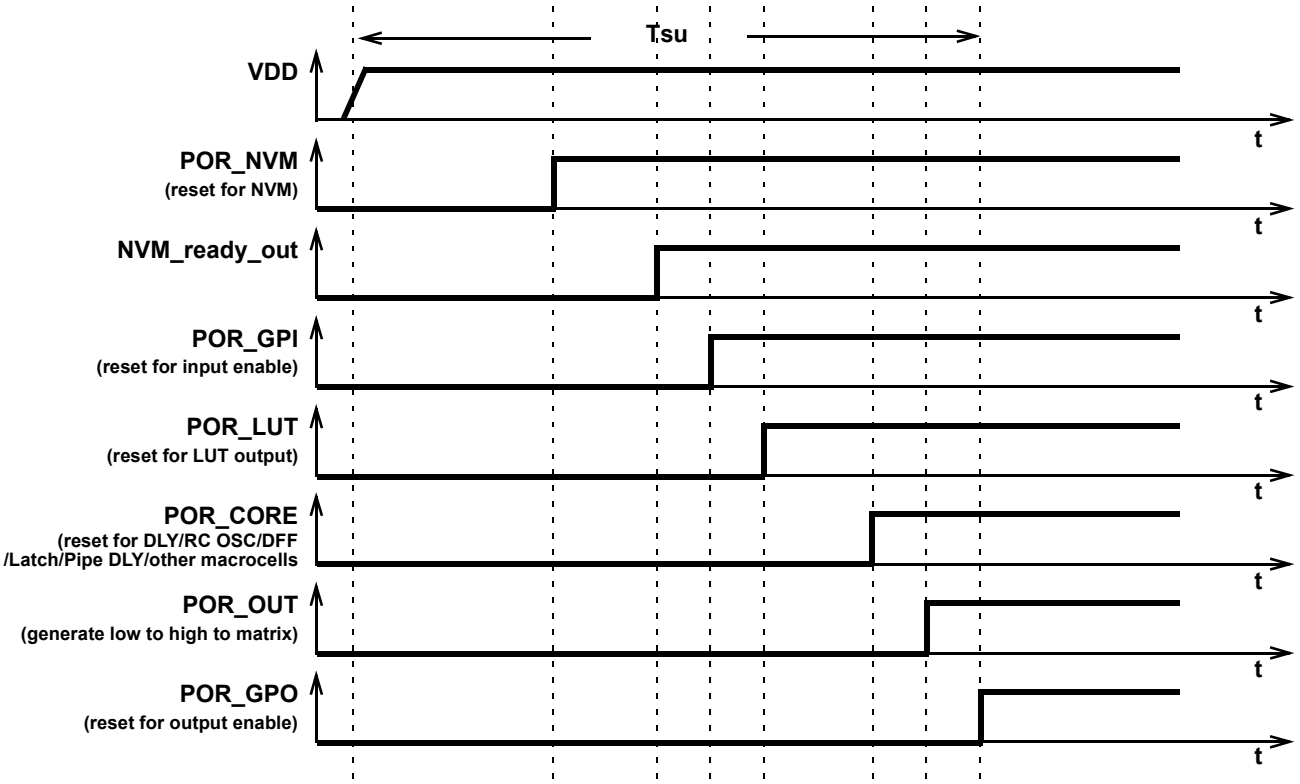


Figure 33. POR sequence

As can be seen from *Figure 33* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

13.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46108 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 34* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

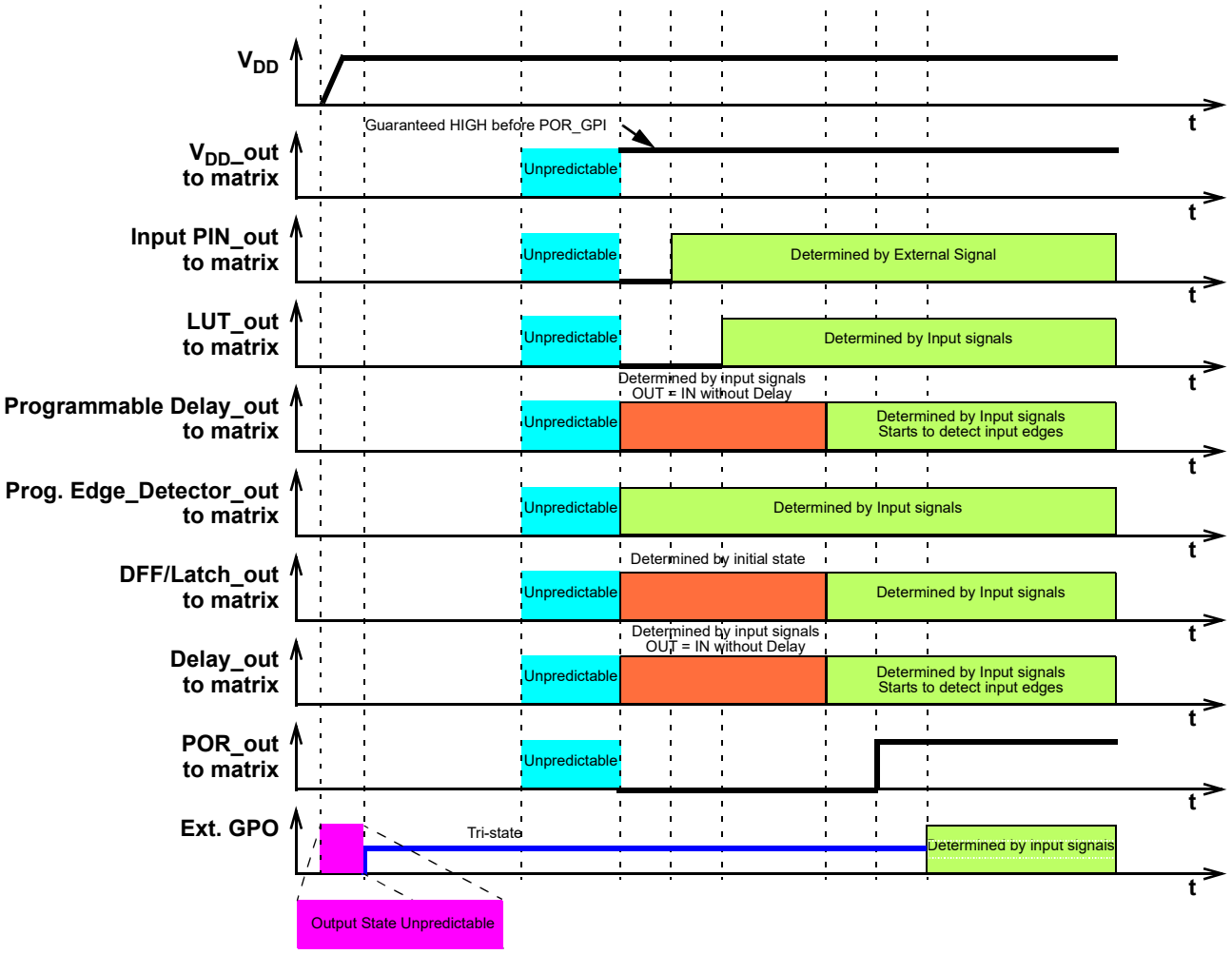


Figure 34. Internal Macrocell States during POR sequence

14.0 Appendix A - SLG46108 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg <4:0>	Pin3 digital out source	
reg <9:5>	Pin4 digital out source	
reg <14:10>	Pin4 output enable	
reg <19:15>	in0 of LUT2_0 (Clock Input of DFF0)	
reg <24:20>	in1 of LUT2_0 (Data Input of DFF0)	
reg <29:25>	in0 of LUT2_1 (Clock Input of DFF1)	
reg <34:30>	in1 of LUT2_1 (Data Input of DFF1)	
reg <39:35>	in0 of LUT2_2	
reg <44:40>	in1 of LUT2_2	
reg <49:45>	in0 of LUT2_3	
reg <54:50>	in1 of LUT2_3	
reg <59:55>	in0 of LUT3_0 (Clock Input of DFF2 with nReset/nSet)	
reg <64:60>	in1 of LUT3_0 (Data input of DFF2 with nReset/nSet)	
reg <69:65>	in2 of LUT3_0 (Resetb or Setb of DFF2 with nReset/nSet)	
reg <74:70>	in0 of LUT3_1 (Clock Input of DFF3 with nReset/nSet)	
reg <79:75>	in1 of LUT3_1 (Data input of DFF3 with nReset/nSet)	
reg <84:80>	in2 of LUT3_1 (Resetb or Setb of DFF3 with nReset/nSet)	
reg <89:85>	in0 of LUT3_2	
reg <94:90>	in1 of LUT3_2	
reg <99:95>	in2 of LUT3_2	
reg <104:100>	in0 of LUT3_3	
reg <109:105>	in1 of LUT3_3	
reg <114:110>	in2 of LUT3_3	
reg <119:115>	in0 of LUT3_4 (Input of pipe delay)	
reg <124:120>	in1 of LUT3_4 (Resetb of pipe delay)	
reg <129:125>	in2 of LUT3_4 (Clock of pipe delay)	
reg <134:130>	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 external Clock)	
reg <139:135>	in1 of LUT4_0 (Input for delay2 or counter2 reset input)	
reg <144:140>	in2 of LUT4_0 (Input for counter2 FSM keep signal)	
reg <149:145>	in3 of LUT4_0 (Input for counter2 FSM up signal)	
reg <154:150>	Input for delay0 or counter0 reset input	
reg <159:155>	Input for delay1 or counter1 reset input	
reg <164:160>	Input for Delay 0/1(Counter 0/1) external clock	
reg <169:165>	Input for delay3 or counter3 reset input	
reg <174:170>	Input for programmable delay (deglitch filter input)	
reg <179:175>	Power down for osc. (higher priority) (high = power down).	
reg <184:180>	Pin6 digital out source	
reg <189:185>	Pin7 digital out source	

Register Bit Address	Signal Function	Register Bit Definition
reg <194:190>	Pin8 digital out source	
reg <199:195>	Pin8 output enable	
reg <207:200>	Reserved	
LUT2		
reg <208>	DFF0 or Latch select / LUT 2_0 <0>	0: DFF function 1: Latch function
reg <209>	LUT 2_0 <1>	
reg <210>	DFF0 initial polarity select / LUT 2_0 <2>	0: Low 1: High
reg <211>	LUT 2_0 <3>	
reg <212>	DFF1 or Latch select / LUT 2_1 <0>	0: DFF function 1: Latch function
reg <213>	LUT 2_1 <1>	
reg <214>	DFF1 initial polarity select / LUT 2_1 <2>	0: Low 1: High
reg <215>	LUT 2_1 <3>	
reg <219:216>	LUT2_2 data	
reg <223:220>	LUT2_3 data	
reg <224>	LUT2_0 or DFF/Latch_0 select	0: LUT2_0 1: DFF4
reg <225>	LUT2_1 or DFF/Latch_1 select	0: LUT2_1 1: DFF5
LUT3		
reg <226>	DFF2 or Latch select / LUT 3_0 <1>	0: DFF function 1: Latch function
reg <227>	LUT 3_0 <2>	
reg <228>	DFF2 rstb/setb select / LUT 3_0 <3>	0:resetb from matrix output 1:setb from matrix output
reg <229>	DFF2 initial polarity select / LUT 3_0 <4>	0: Low 1: High
reg <233:230>	LUT 3_0 <7:5>	
reg <234>	DFF3 or Latch select / LUT 3_1 <1>	0: DFF function 1: Latch function
reg <235>	LUT 3_1 <2>	
reg <236>	DFF3 rstb/setb select / LUT 3_1 <3>	0: resetb from matrix output 1: setb from matrix output
reg <237>	DFF3 initial polarity select / LUT 3_1 <4>	0: Low 1: High
reg <241:238>	LUT 3_1 <7:5>	
reg <249:242>	LUT3_2 data	
reg <257:250>	LUT3_3 data	
reg <265:258>	LUT3_4 data or pipe number select	reg<260:258>: OUT0 select reg<263:261>: OUT1 select
reg <266>	LUT3_0 or DFF/Latch_2 (with nReset/nSet) select	0:LUT3_0 1:DFF2
reg <267>	LUT3_1 or DFF/Latch_3 (with nReset/nSet) select	0: LUT3_1 1: DFF3

Register Bit Address	Signal Function	Register Bit Definition
reg <268>	LUT3_4 or Pipe delay select	0: LUT3_4 1: Pipe delay
LUT4		
reg <284:269>	LUT4_0 data or:	
reg <269>	Counter/delay2 mode selection	0: Delay Mode 1: Counter Mode
reg <272:270>	Counter/delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter1 Overflow
reg <280:273>	Counter/delay2 Control Data	1 – 255 (delay time = (counter control data +1) /freq)
reg <282:281>	Delay2 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg <283>	Counter2/FSM2's Q are set to Data or Reset to 0s selection	0: reset to 0 1: set to data
reg <285>	LUT4_0 or counter_2 select	0: LUT4_0 1: Counter2
OSC		
reg <286>	Force oscillator on	0: Auto Power on 1: Force Power on
reg <287>	Oscillator frequency control	0: 25 k 1: 2 M
reg <289:288>	Osc clock pre-divider	00: div1 01: div2 10: div4 11: div8
reg <292:290>	internal oscillator divider frequency control 1	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <295:293>	internal oscillator divider frequency control 2	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <296>	External Clock Source Select	0: Internal Oscillator 1: External Clock from Pin8
reg <297>	Reserved	

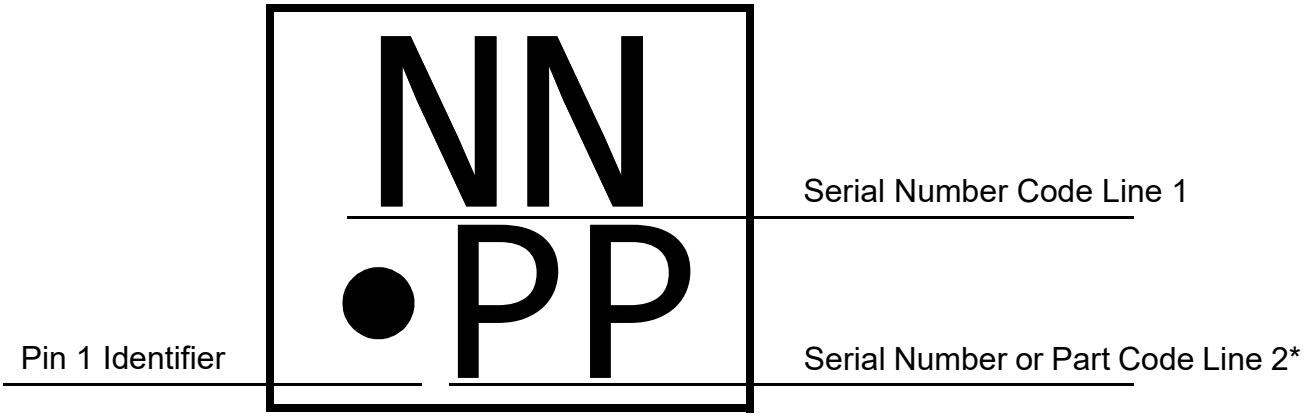
Register Bit Address	Signal Function	Register Bit Definition
reg <298>	OSC Clock 25KHz/2MHz to matrix input <20> enable	
reg <299>	OSC Clock 25KHz/2MHz to matrix input <21> enable	
reg <300>	OSC Fast Start-Up Enable for 25KHz/2MHz	
CNT/DLY		
reg <301>	Counter/Delay0 (8bits) mode select	0: Delay mode 1: Counter mode
reg <302>	Reserved	
reg <305:303>	Counter/delay0 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter3 Overflow
reg <313:306>	Counter0 Control Data/Delay0 Time Control	1-255: (delay time = (counter control data +1) /freq)
reg <315:314>	Delay0 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg <317:316>	Reserved	
reg <318>	Counter/Delay1 (8bits) mode select	0: Delay mode 1: Counter mode
reg <319>	Reserved	
reg <322:320>	Counter/delay1 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
reg <330:323>	Counter1 Control Data/Delay1 Time Control	1-255: (delay time = (counter control data +1) /freq)
reg <332:331>	Delay1 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg <334:333>	Reserved	
reg <335>	Counter/Delay3 (8bits) mode select	0: Delay mode 1: Counter mode
reg <338:336>	Counter/delay3 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter2 Overflow
reg <346:339>	Counter3 Control Data/Delay3 Time Control	1-255: (delay time = (counter control data +1) /freq)

Register Bit Address	Signal Function	Register Bit Definition
reg <348:347>	Delay3 Mode Select	00: Delay on both falling and rising edges 01: delay on falling edge only 10: delay on rising edge only 11: no delay on either falling or rising edges
PIN 2		
reg <350:349>	Pin2 Mode control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
reg <352:351>	Pin2 Pull down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
PIN 3		
reg <355:353>	Pin3 Mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
reg <357:356>	Pin3 Pull up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg <358>	Pin3 Pull up/down resistor enable.	0: Pull down resistor enable 1: Pull up resistor enable
reg <359>	Pin3 Driver strength selection	0: 1X 1: 2X
PIN 4		
reg <361:360>	Pin4 Mode control (sig_pin4_oe = 0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
reg <363:362>	Pin4 Mode control (sig_pin4_oe = 1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg <365:364>	Pin4 Pull up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg <366>	Pin4 Pull up/down resistor enable.	0: Pull down resistor enable 1: Pull up resistor enable
reg <367>	Reserved	

Register Bit Address	Signal Function	Register Bit Definition
PIN 6		
reg <370:368>	Pin6 Mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
reg <372:371>	Pin6 Pull up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg <373>	Pin6 Pull up/down resistor enable.	0: Pull down resistor enable 1: Pull up resistor enable
reg <374>	Pin6 Driver strength selection	0: 1X 1: 2X
PIN 7		
reg <377:375>	Pin7 Mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
reg <379:378>	Pin7 Pull up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg <380>	Pin7 Pull up/down resistor enable.	0: Pull down resistor enable 1: Pull up resistor enable
reg <381>	Pin7 Driver strength selection	0: 1X 1: 2X
PIN 8		
reg <383:382>	Pin8 Mode control (sig_pin8_oe = 0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
reg <385:384>	Pin8 Mode control (sig_pin8_oe = 1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg <387:386>	Pin8 Pull up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg <388>	Pin8 Pull up/down resistor enable.	0: Pull down resistor enable 1: Pull up resistor enable
reg <390:389>	Reserved	
Quick Charge		
reg <391>	GPIO quick charge enable	0: Disable 1: Enable

Register Bit Address	Signal Function	Register Bit Definition
Pipe Delay		
reg <392>	Pipe delay OUT1 polarity select bit	0: Non-inverted 1: Inverted
Pattern ID		
reg <400:393>	8-bit pattern id	
Deglitch Filter		
reg <401>	Deglitch filter out polarity selection	0: Non-inverted 1: Inverted
Misc.		
reg <402>	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
reg <403>	NVM power down (or NVM data programming disable)	0: None (or programming enable) 1: Power Down (or programming disable)
reg <405:404>	Reserved	
reg <406>	Reserved	
reg <407>	Reserved	
PGM Delay and Edge Detector		
reg <408>	Pin2 Edge Detect Mode	0: Rising edge 1: Falling edge
reg <409>	Pin2 Bypass the pin2	0: PIN2 edge active 1: PIN2 high active
reg <410>	PIN2 Reset enable	0: Disable 1: Enable
reg <411>	Programmable delay or filter output select	0: Programmable delay output 1: Filter output
reg <413:412>	Select the edge mode of programmable delay with edge detector	00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
reg <415:414>	Delay value select for programmable delay & edge detector (VDD = 3.3 V, typical condition)	00: 135 ns 01: 270 ns 10: 405 ns 11: 540 ns
reg <423:416>	Reserved	
reg <431:424>	Reserved	
reg <437:432>	Reserved	
reg <439:438>	Reserved	
reg <445:440>	Reserved	
reg <447:446>	Reserved	
reg <448>	Reserved	
reg <449>	Reserved	
reg <450>	Reserved	
reg <451>	Reserved	
reg <455:452>	Reserved	
reg <463:456>	Reserved	

15.0 Package Top Marking System Definition

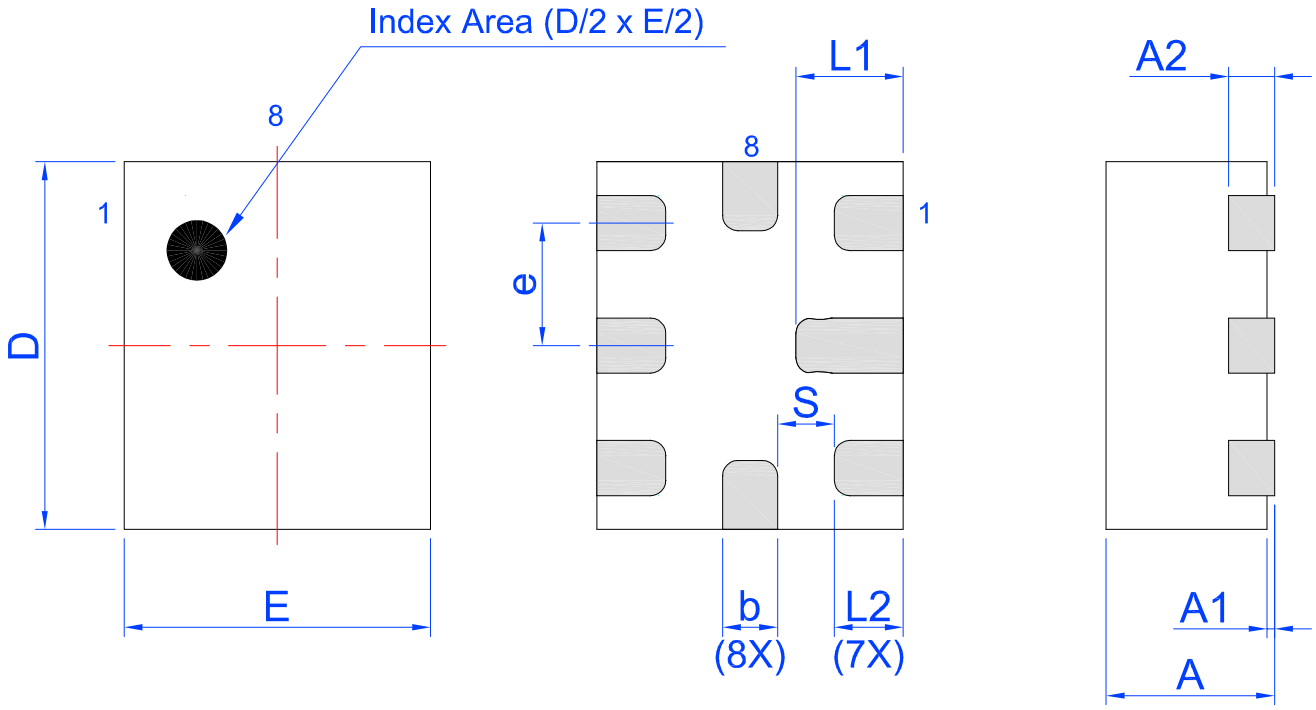


* PP may consist of the special characters +, -, and = for a total of 9 different combinations, or may consist of two character alphanumeric Part Code (A-Z and 0-9), depending on time of marking.

Note: The SN Code (Line 1 and Line 2) is generated during production, and encodes information including part number, programming code number, date code and lot code. This same information is provided in plain text form on a label placed on the reel. If you need assistance in decoding the SN Code, please contact Dialog Semiconductor.

16.0 Package Drawing and Dimensions

8 Lead STQFN Package 1.0 x 1.2 mm
IC net weight: 0.0017 g



TOP View **BTM View** **SIDE View**

Unit: mm

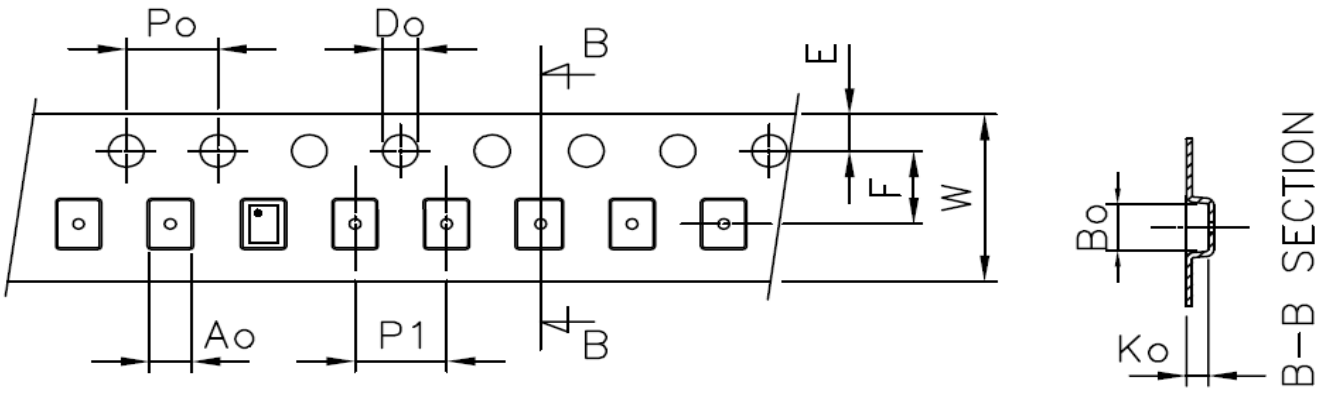
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.15	1.20	1.25
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.30	0.35	0.40
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.185 REF		

17.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 8L 0.4P FC Green	8	1.0x1.2x0.55	3000	3000	178/60	100	400	100	400	8	4

17.1 Carrier Tape Drawing and Dimensions

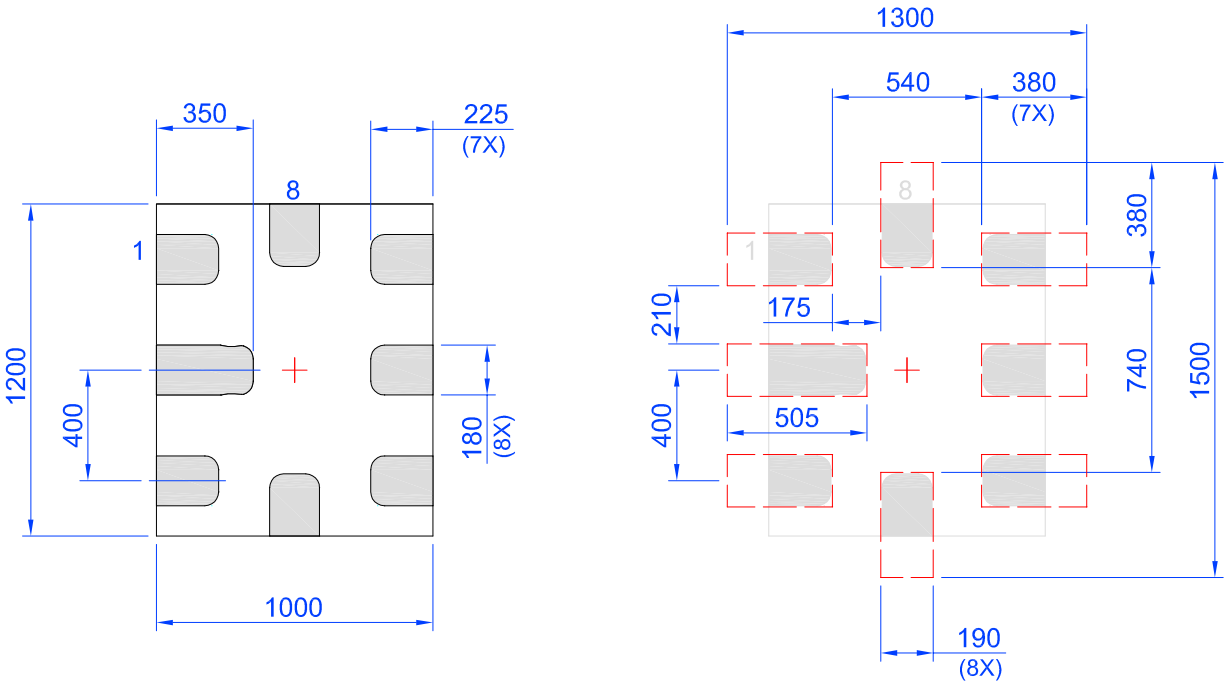
Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 8L 0.4P FC Green	1.16	1.38	0.71	4	4	1.5	1.75	3.5	8



18.0 Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Landing Pattern
(PKG face down)



Unit: um

19.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

20.0 Revision History

Date	Version	Change
8/25/2020	1.12	Updated figure Internal Macrocell States during POR sequence Added note for CNTs Corrected registers [346:336], [330:320], [313:303], [280:270]
7/11/2019	1.11	Corrected Absolute Maximum Conditions Corrected Appendix A Fixed typos
11/13/2018	1.10	Updated to Dialog style Updated Marking Spec Fixed typos
5/10/2018	1.09	Fixed typos
10/27/2017	1.08	Updated OSC Electrical Spec
10/9/2017	1.07	Updated Electrical Spec Fixed typos
8/10/2017	1.06	Fixed typos
7/28/2017	1.05	Corrected Pin Structure Diagrams Fixed typos
7/5/2017	1.04	Fixed typos Updated Silego Website & Support Updated Section Programmable Delay / Edge Detector Updated Landing Pattern Updated Electrical Spec
8/31/2016	1.03	Updated OSC Specifications
7/27/2016	1.02	Updated Programmable Delay for clarification Clarified Electrical Characteristics Table conditions Simplified IDD Estimator table Fixed RC Oscillator descriptions Added Note to Package Marking
7/1/2016	1.01	Final clean up
6/15/2016	1.00	Production Release
5/19/2016	0.50	Preliminary Release

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