

## P-Channel Enhancement Mode Power MOSFET

### Description

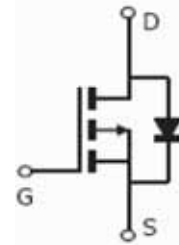
The RM70P30LD uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

### General Features

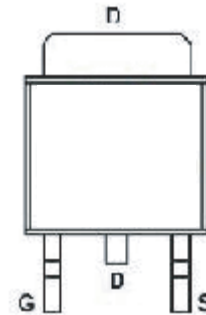
- $V_{DS} = -30V, I_D = -70A$   
 $R_{DS(ON)} < 7.2m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 12m\Omega @ V_{GS} = -4.5V$
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low on-resistance

### Application

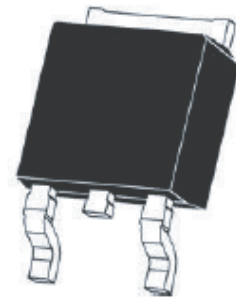
- Power switch
- DC/DC converters
- Halogen-free
- P/N suffix V means AEC-Q101 qualified, e.g: RM70P30LDV



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

**100% UIS TESTED!**

**100%  $\Delta V_{ds}$  TESTED!**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
70P30	RM70P30LD	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-70	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	-50	A
Pulsed Drain Current	$I_{DM}$	-200	A
Maximum Power Dissipation	$P_D$	90	W
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	80	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta jc}$	1.6	$^{\circ}\text{C}/\text{W}$
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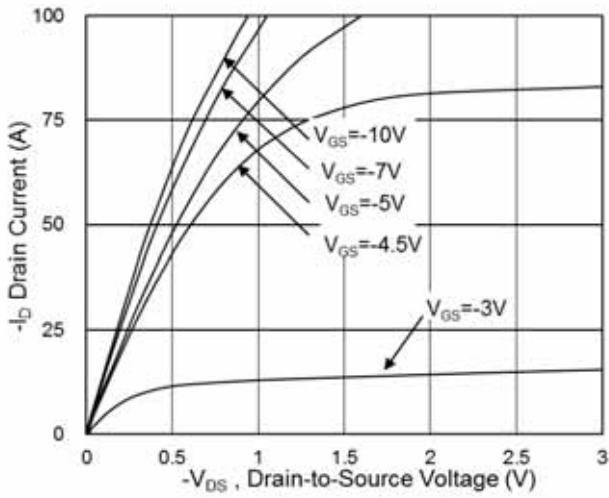
## Electrical Characteristics ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-	-2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$	-	6	7.2	m $\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	-	9.5	12	
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	3450	-	PF
Output Capacitance	$C_{oss}$		-	255	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	140	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-10A$ $V_{GS}=-20V, R_{GEN}=3.3\Omega$	-	17	-	nS
Turn-on Rise Time	$t_r$		-	40	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	$t_f$		-	13	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_D=-18A,$ $V_{GS}=-10V$	-	60	-	nC
Gate-Source Charge	$Q_{gs}$		-	9	-	nC
Gate-Drain Charge	$Q_{gd}$		-	15	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-1A$	-	-	-1.2	V
Diode Forward Current (Note 2)	$I_S$	-	-	-	-70	A
Reverse Recovery Time	$t_{rr}$	$T_J=25^{\circ}\text{C}, I_F=-20A$ $di/dt=100A/\mu s$ (Note 3)	-	22	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	72	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

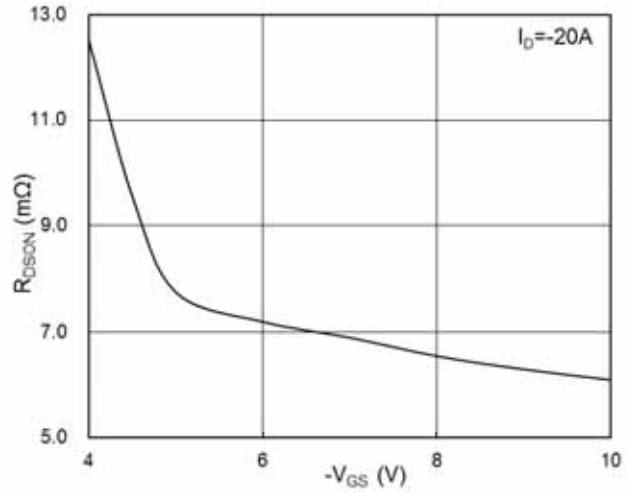
## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, L=0.5\text{mH}, R_g=25\Omega$

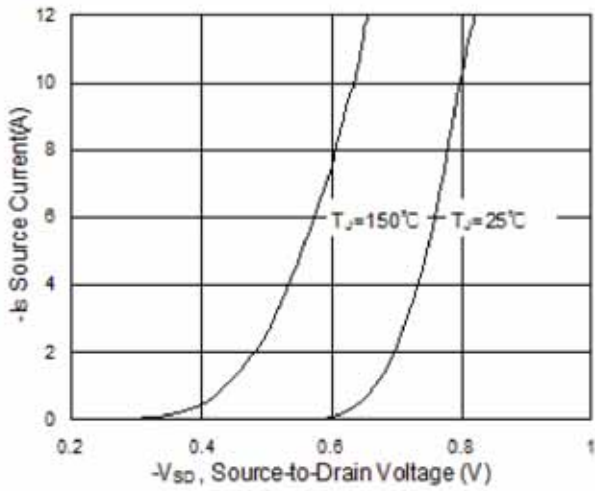
## RATING AND CHARACTERISTICS CURVES (RM70P30LD)



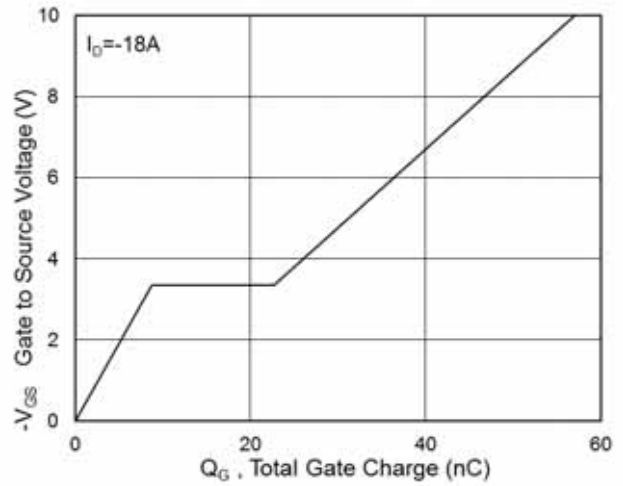
**Fig.1 Typical Output Characteristics**



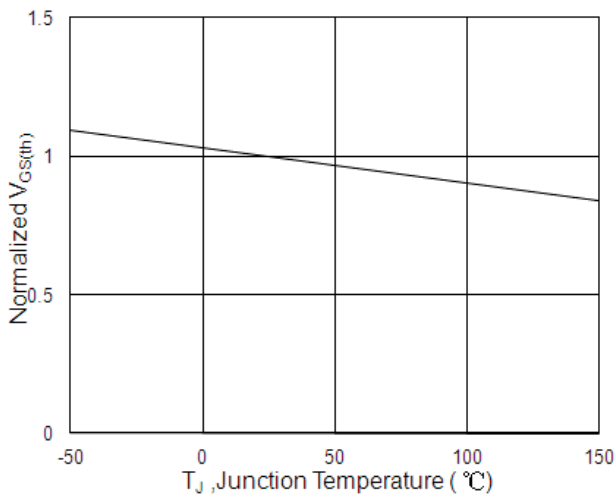
**Fig.2 On-Resistance vs. Gate-Source Voltage**



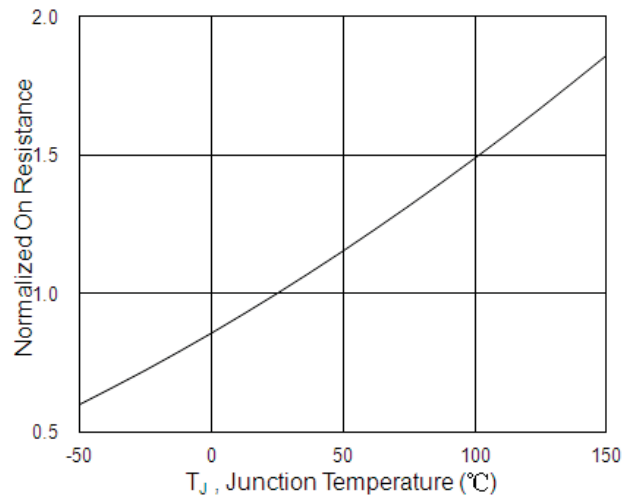
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

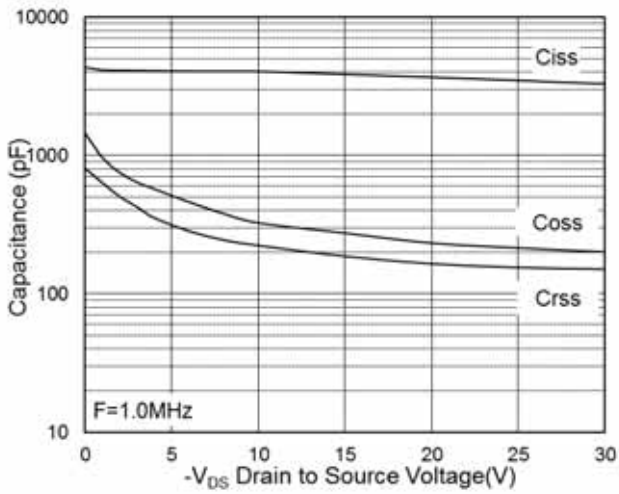


**Fig.5 Normalized  $-V_{GS(th)}$  vs.  $T_J$**

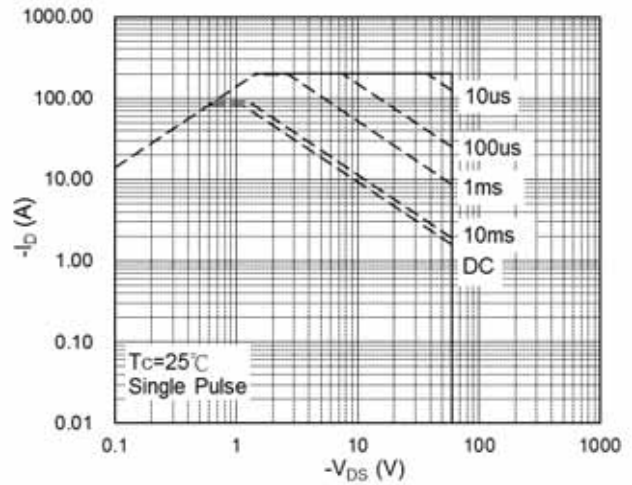


**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

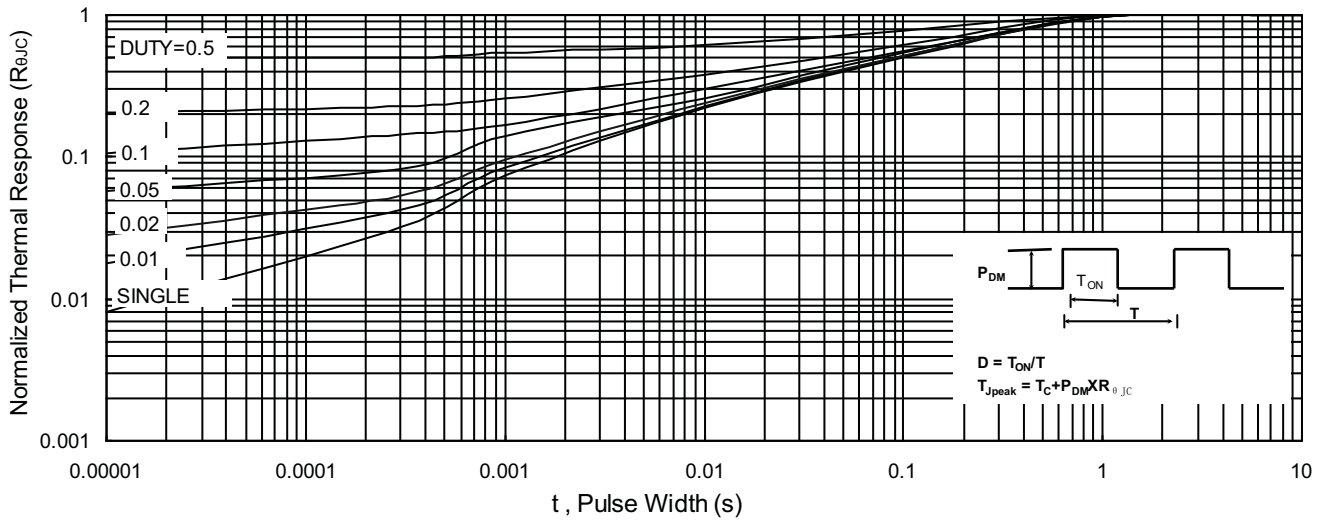
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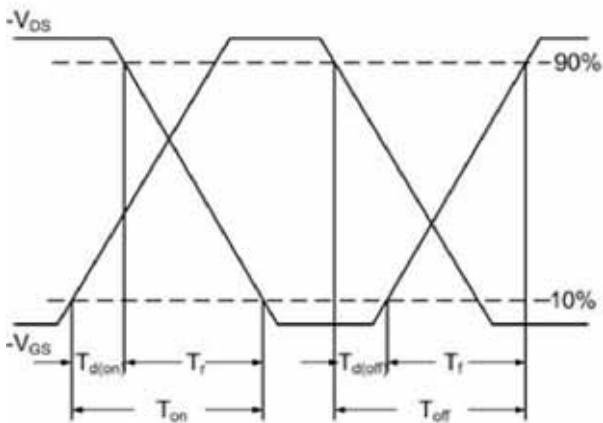
**Fig.7 Capacitance**



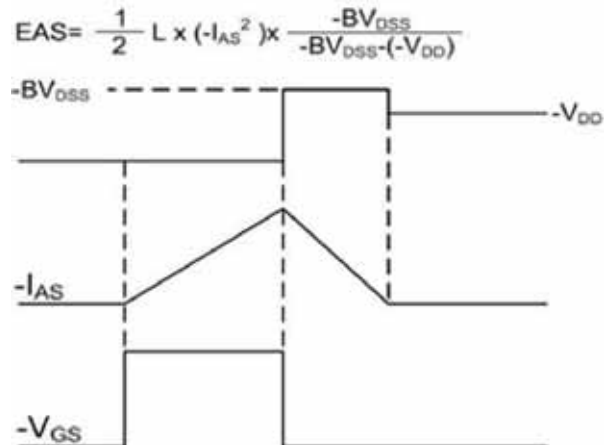
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

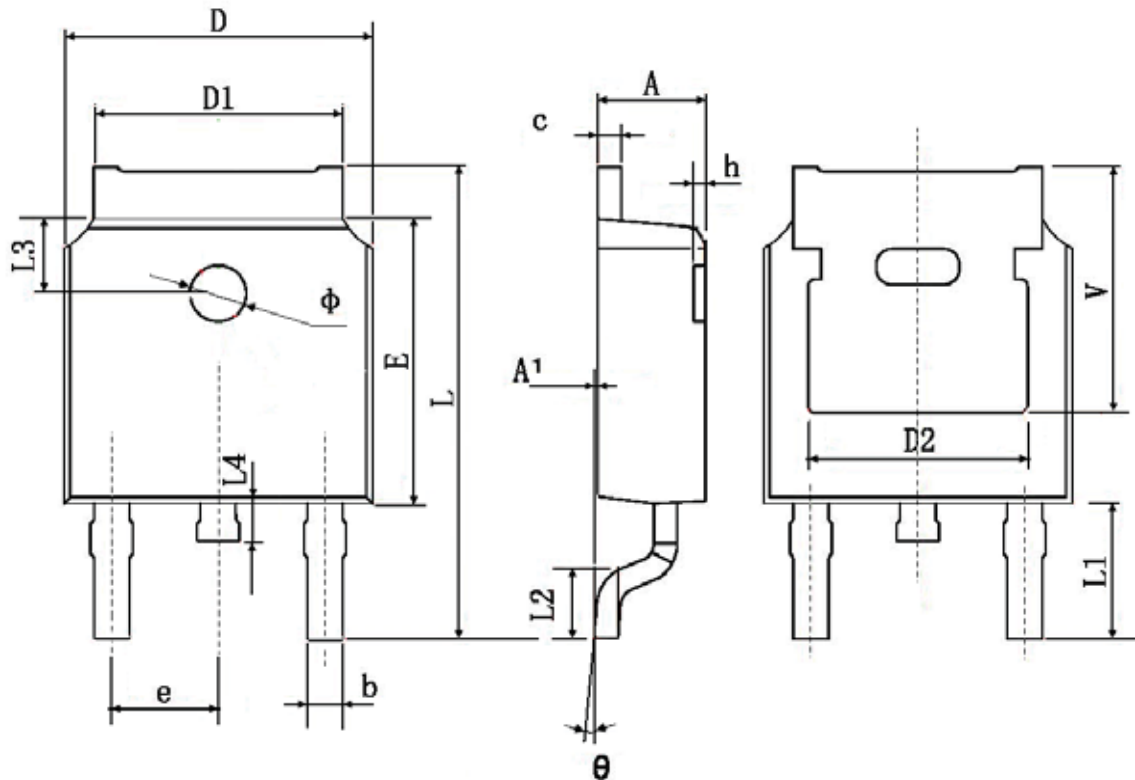


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
phi	1.100	1.300	0.043	0.051
theta	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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