IS61/64WV102416EDALL
IS61/64WV102416EDBLL

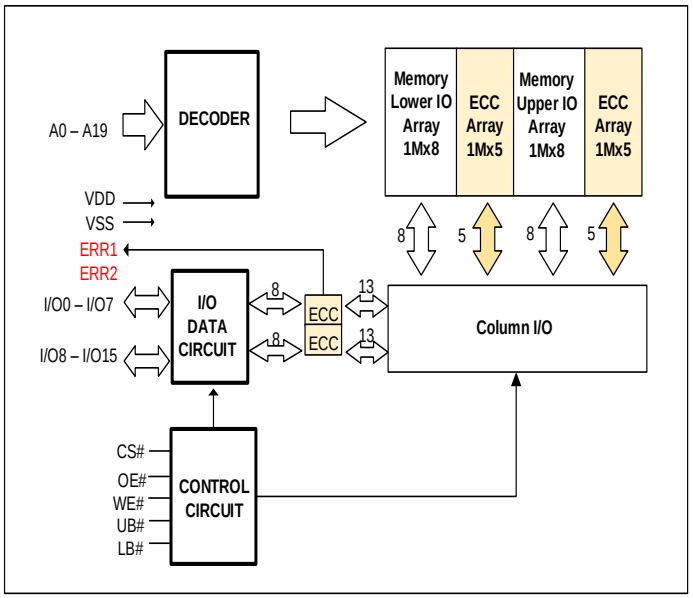
AUGUST 2019

1Mx16 HIGH SPEED AYNCHRONOUS CMOS STATIC RAM with ECC

KEY FEATURES

- High-speed access time: 10ns, 12ns
- Single power supply
  - 1.65V-2.2V VDD(IS61/64WV102416EDALL)
  - 2.4V-3.6V VDD (IS61/64WV102416EDBLL)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
  - ERR1 pin indicates 1-bit error detection and correction.
  - ERR2 pin indicates 2-bit error detection
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The *ISSI* IS61/64WV102416EDALL/EDBLL are high-speed, low power, 16M bit static RAMs organized as 1M words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yield high-performance and highly reliable devices.

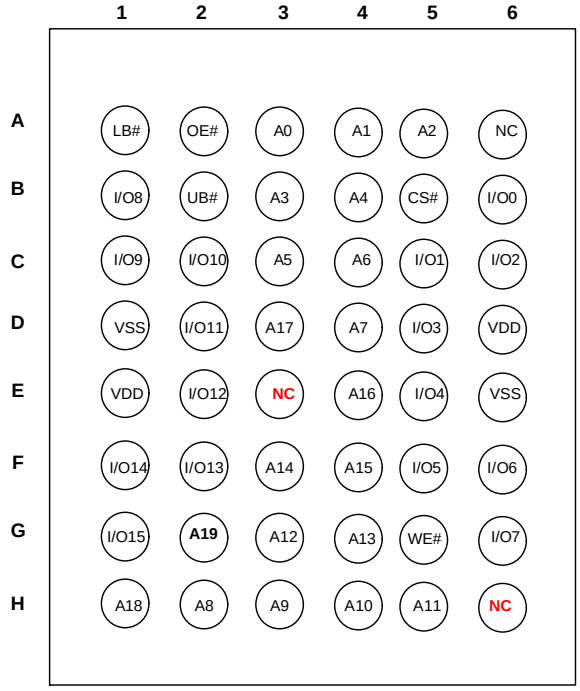
When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Easy memory expansion is provided by using Chip Enable and Output Enable inputs.

The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

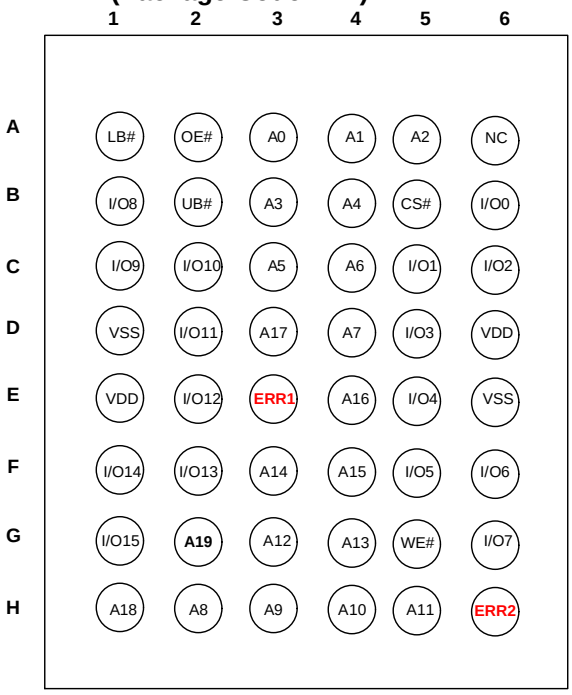
The IS61/64WV102416EDALL/EDBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 48-pin TSOP (TYPE I)

PIN CONFIGURATIONS

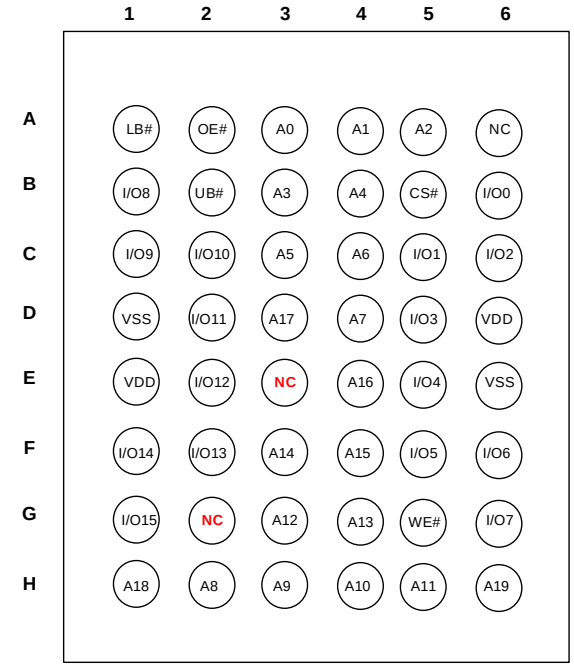
48-Pin mini BGA(6mm x 8mm), A19 on G2 (Package Code : B)



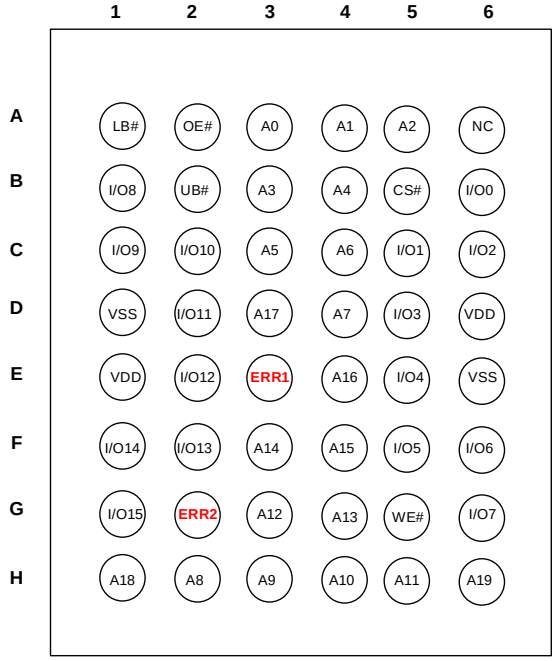
48-Pin mini BGA (6mm x 8mm) , A19 on G2, ERR1/2 (Package Code : B2)



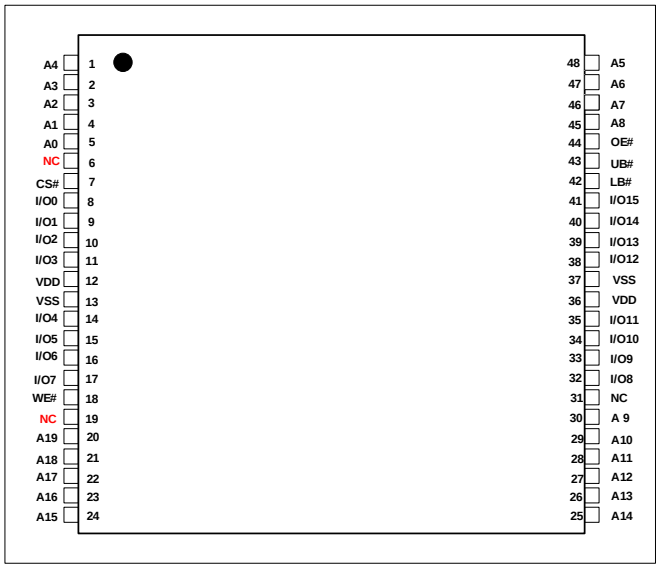
48-Pin mini BGA(6mm x 8mm), A19 on H6 (Package Code : B3)



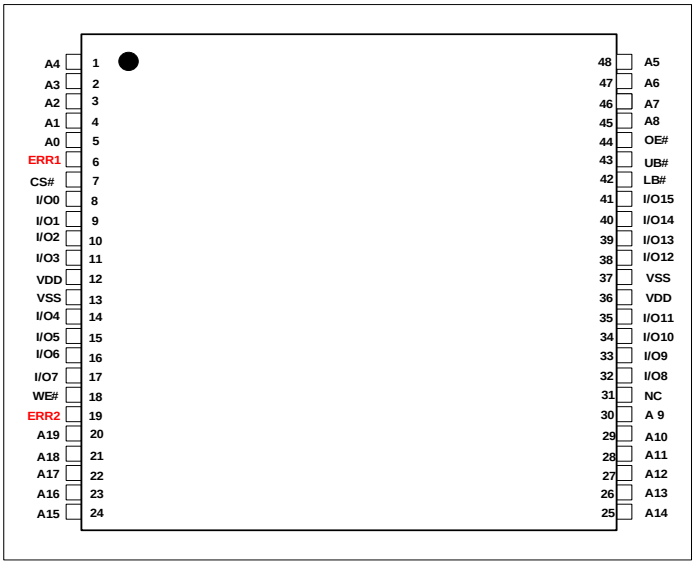
48-Pin mini BGA (6mm x 8mm) , A19 on H6, ERR1/2 (Package Code : B4)



48-Pin TSOP-I



48-Pin TSOP-I with ERR1/ERR2



PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
ERR1	1-bit Error Detection and Correction Signal
ERR2	2-bit ERR Detection Signal
NC	No Connection
V_{DD}	Power
VSS	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS#) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct one bit error per byte or detect 2-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates 2-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

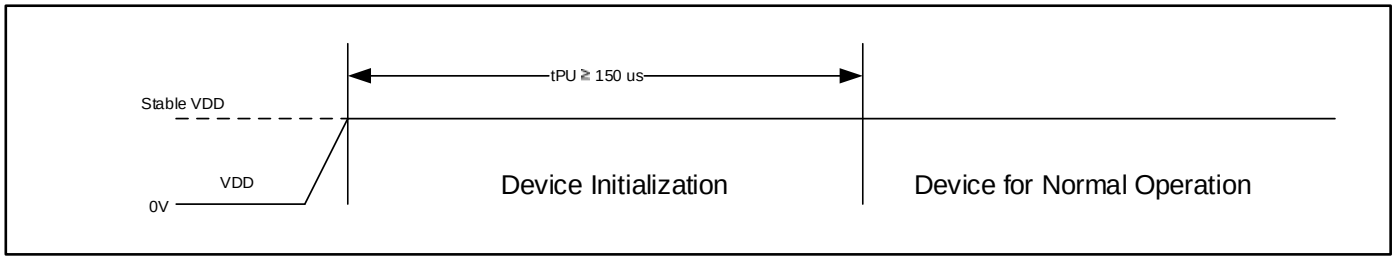
ERR1	ERR2	DQ pin	Status	Remark
0	0	Valid Q	No Error	
1	0	Valid Q	1-Bit Error only	1-bit error per byte detected and corrected
0	1	In-Valid Q	2-Bit Error only	No 1-bit error. 2-bit error per byte detected (out of 2 bytes)
1	1	In-Valid Q	1-bit & 2-bit error	1-bit error detected and corrected at one byte, and 2-bit error detected at another byte.
High-Z	High-Z	Valid D	Non-Read	Write operation or Output Disabled

TRUTH TABLE

Mode	CS#	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	L	H	H	L	L	High-Z	High-Z	ICC
	L	H	H	H	L	High-Z	High-Z	
Read	L	H	L	L	H	DOUT	High-Z	ICC
	L	H	L	H	L	High-Z	DOUT	
	L	H	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	ICC
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

POWER UP INITIALIZATION

The device includes on-chip voltage sensor used to launch POWER-UP initialization process.
When VDD reaches stable level, the device requires 150us of tPU (Power-Up Time) to complete its self-initialization process.
When initialization is complete, the device is ready for normal operation.



ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	VDD	SPEED (MAX)
Commercial	0°C to +70°C	IS61WV102416EDALL	1.65V – 2.2V	12 ns(1)
		IS61WV102416EDBLL	2.4V – 3.6V	10ns
Industrial	-40°C to +85°C	IS61WV102416EDALL	1.65V – 2.2V	12 ns(1)
		IS61WV102416EDBLL	2.4V – 3.6V	10ns
Automotive (A3)	-40°C to +125°C	IS64WV102416EDALL	1.65V – 2.2V	12 ns
		IS64WV102416EDBLL	2.4V – 3.6V	

Note:
1. Contact ISSI MKT for 1.8V 10ns device.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.4V~3.6V)
Input Pulse Level	0V to V_{DD}	0V to V_{DD}
Input Rise and Fall Time	1.5 ns	1.5 ns
Output Timing Reference Level	½ V_{DD}	½ V_{DD}
R1 (ohm)	13500	319
R2 (ohm)	10800	353
V_{TM} (V)	1.8V	3.3V
Output Load Conditions	Refer to Figure 1 and 2	

AC TEST LOADS

FIGURE 1

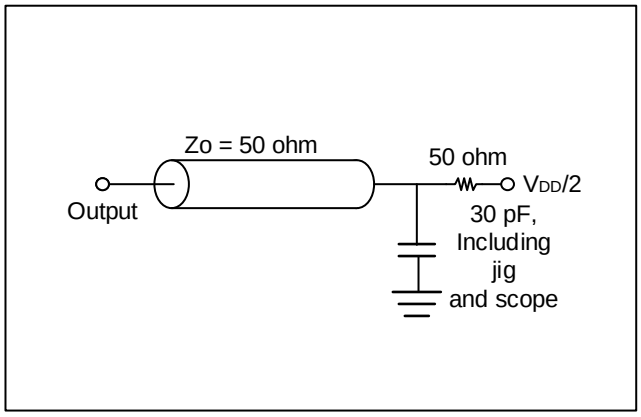
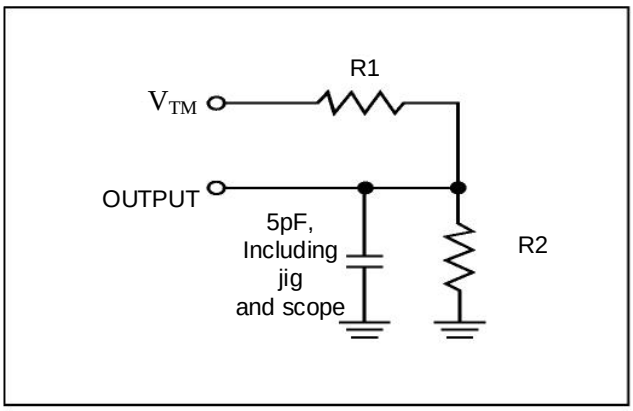


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (OVER THE OPERATING RANGE)

VDD = 1.65V – 2.2V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Note:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

VDD = 2.4V – 3.6V

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OH} = -1.0 mA	2.0	—	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OH} = -4.0 mA	2.2		
V_{OL}	Output LOW Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OL} = 2.0 mA	—	0.4	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	
V_{IH}(1)	Input HIGH Voltage	2.4V ~ 2.7V		2.0	V_{DD} + 0.3	V
		2.7V ~ 3.6V		2.0		
V_{IL}(1)	Input LOW Voltage	2.4V ~ 2.7V		–0.3	0.6	V
		2.7V ~ 3.6V		–0.3	0.8	
I_{LI}	Input Leakage		VSS < V_{IN} < V_{DD}	–2	2	µA
I_{LO}	Output Leakage		VSS < V_{IN} < V_{DD}, Output Disabled	–2	2	µA

Note:
1. VIL(min) = -0.3V DC ; VIL(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
   VIH (max) = VDD + 0.3V DC ; VIH(max) = VDD + 2.0V AC (pulse width 2.0ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-10 Max.	-12 Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = f_{MAX}	Com.	90	85	mA
			Ind.	100	95	
			Auto.	140	135	
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	80	80	mA
			Ind.	90	90	
			Auto.	110	110	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL} CS# ≥ V_{IH}, f = 0	Com.	60	60	mA
			Ind.	70	70	
			Auto.	110	110	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	50	50	mA
			Ind.	60	60	
			Auto.	100	100	
			Typ. (2)	10		

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V_{DD} = 3.0V/1.8V, T_A = 25 °C and not 100% tested.

AC CHARACTERISTICS (OVER OPERATING RANGE)

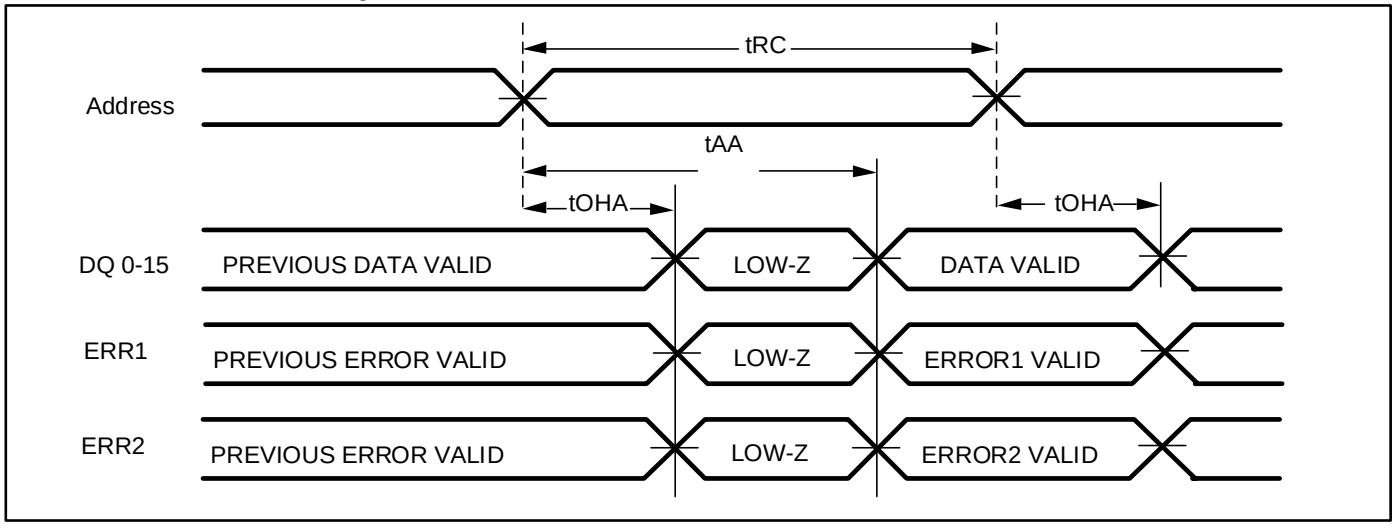
READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	-10[1]		-12[1]		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	10	-	12	-	ns	
Address Access Time	tAA	-	10	-	12	ns	
Output Hold Time	tOHA	2.5	-	2.5	-	ns	
CS# Access Time	tACE	-	10	-	12	ns	
OE# Access Time	tDOE	-	6	-	7	ns	
OE# to High-Z Output	tHZOE	0	5	0	6	ns	2
OE# to Low-Z Output	tLZOE	0	-	0	-	ns	2
CS# to High-Z Output	tHZCE	0	5	0	6	ns	2
CS# to Low-Z Output	tLZCE	3	-	3	-	ns	2
UB#, LB# Access Time	tBA	-	6	-	7	ns	
UB#, LB# to High-Z Output	tHZB	0	5	0	6	ns	2
UB#, LB# to Low-Z Output	tLZB	0	-	0	-	ns	2

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0V to V_{DD} and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

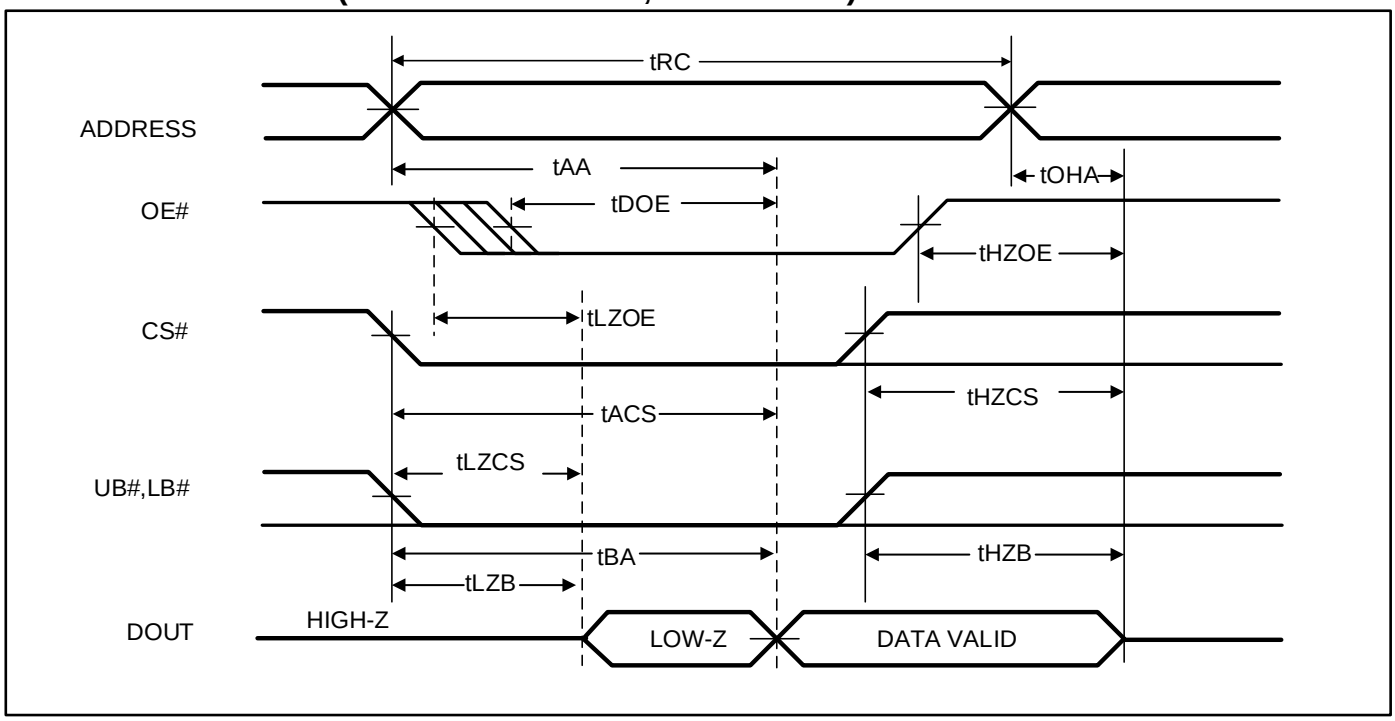
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED, CS# = OE# = UB# = LB# = LOW, WE# = HIGH)



Notes:
1. The device is continuously selected.
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

READ CYCLE NO. 2[1] (OE# CONTROLLED, WE# = HIGH)



Note:
1. Address is valid prior to or coincident with CS# LOW transition.

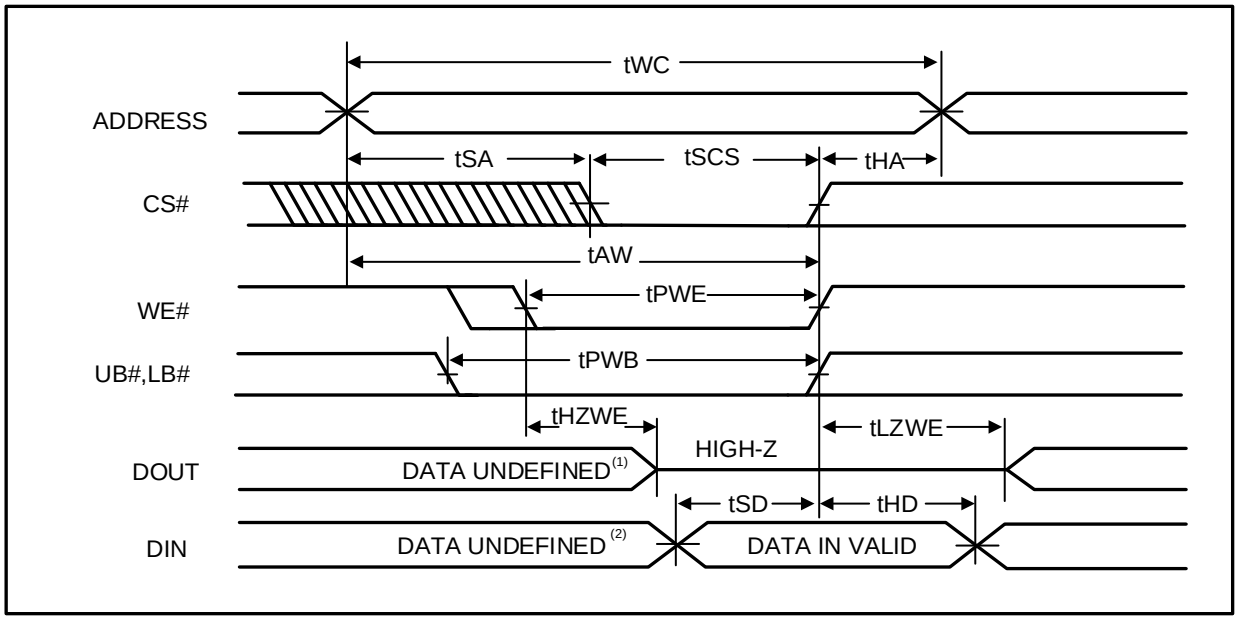
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-10(1)		-12(1)		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	10	-	12	-	ns	
CS# to Write End	tSCS	8	-	9	-	ns	
Address Setup Time to Write End	tAW	8	-	9	-	ns	
UB#,LB# to Write End	tPWB	8	-	9	-	ns	
Address Hold from Write End	tHA	0	-	0	-	ns	
Address Setup Time	tSA	0	-	0	-	ns	
WE# Pulse Width	tPWE1	8	-	9	-	ns	
WE# Pulse Width (OE# = LOW)	tPWE2	10	-	12	-	ns	2
Data Setup to Write End	tSD	6	-	7	-	ns	
Data Hold from Write End	tHD	0	-	0	-	ns	
WE# LOW to High-Z Output	tHZWE	-	4	-	5	ns	
WE# HIGH to Low-Z Output	tLZWE	2	-	2	-	ns	

Notes:
1 The internal write time is defined by the overlap of CS# = LOW, UB# or LB# = LOW, and WE# = LOW. All conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2 tPWE > tHZWE + tSD when OE# is LOW.

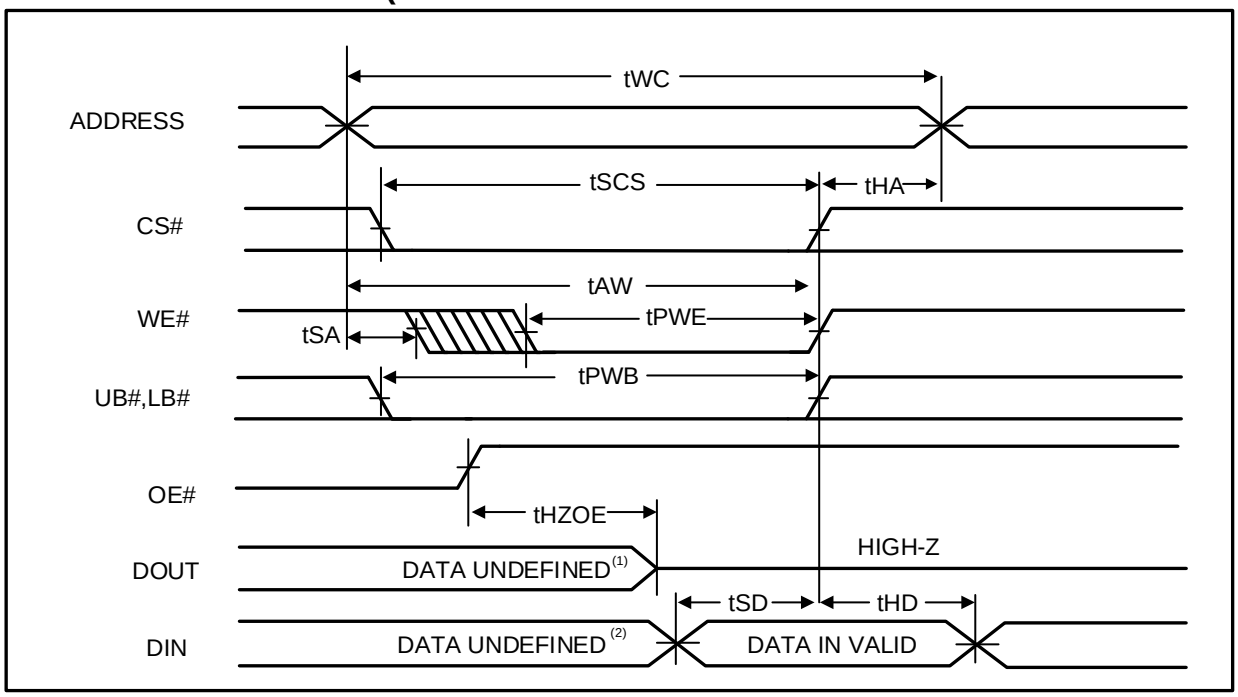
AC WAVEFORMS

WRITE CYCLE NO. 1 (CS# CONTROLLED, OE# = HIGH OR LOW)



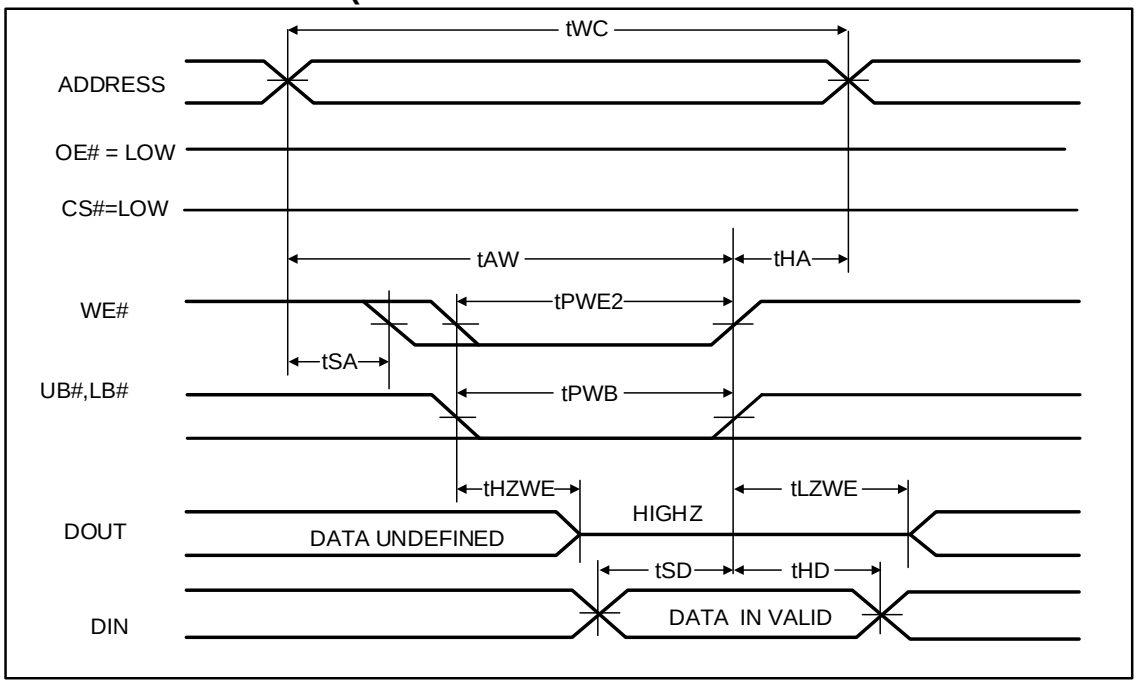
Note:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle.

WRITE CYCLE NO. 2[1,2] (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



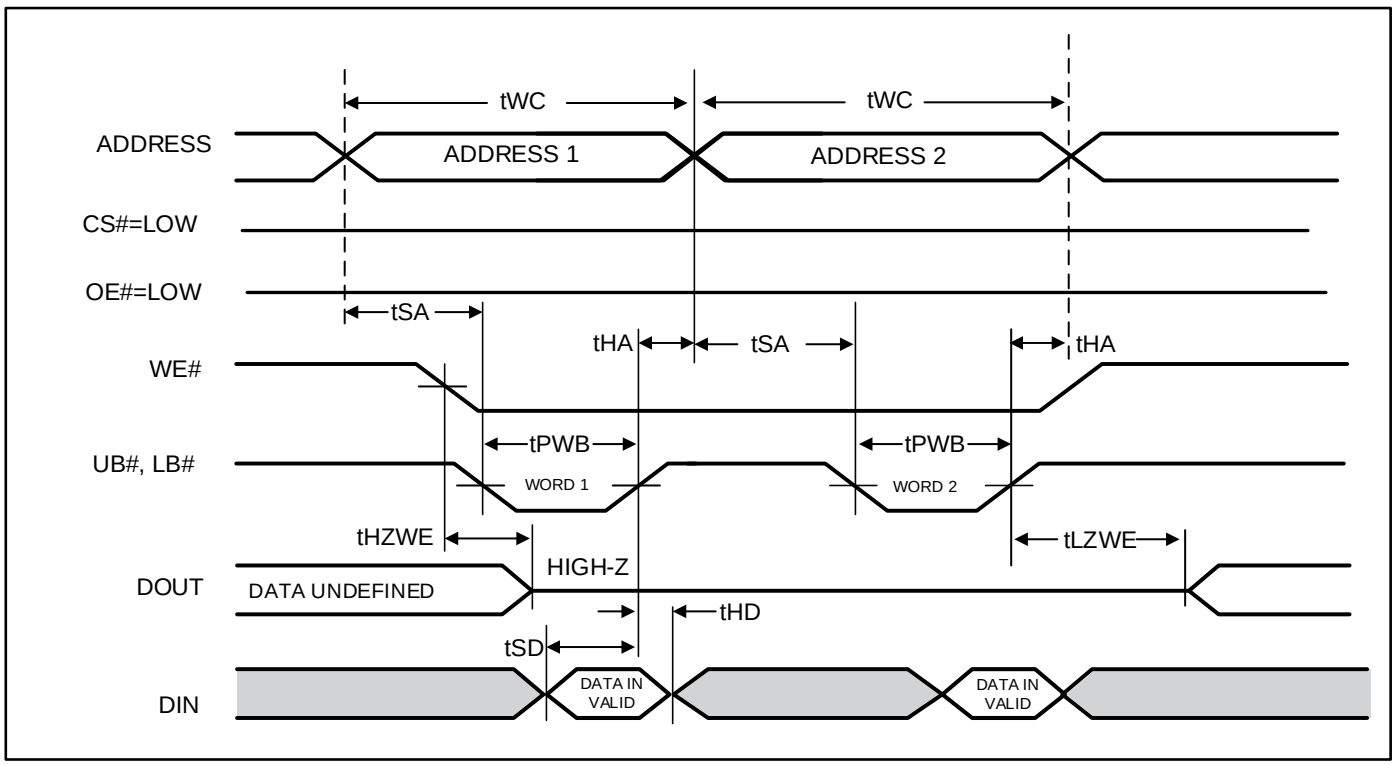
Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:
3. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4[1, 2, 3] (UB# & LB# Controlled, CS# = OE# = LOW)



Notes:

1 If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

2 Due to the restriction of note1, OE# is recommended to be HIGH during write period.

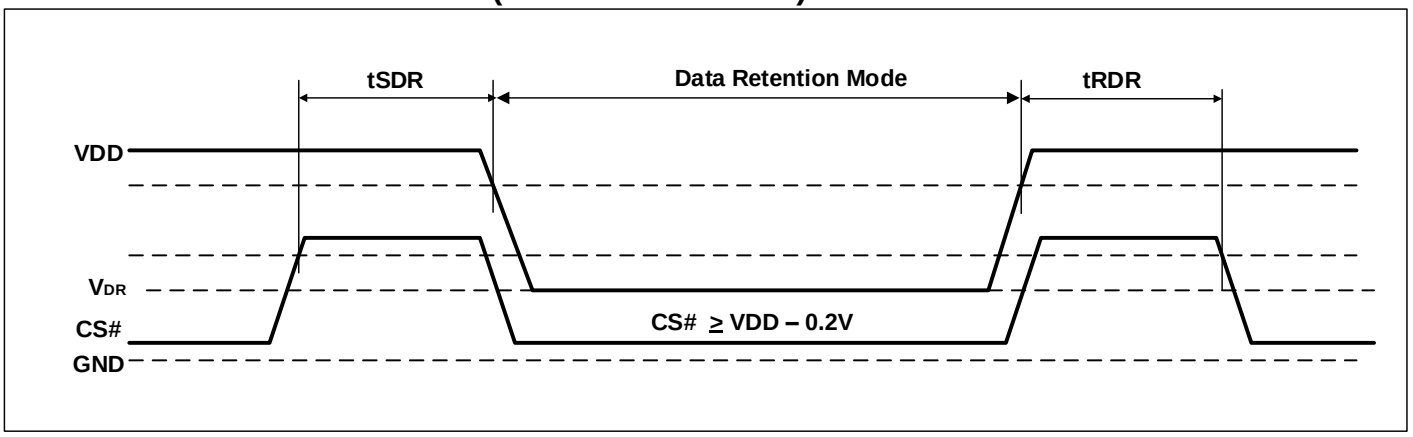
3 WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	V_{DD} = 2.4V to 3.6V	2.0		3.6	V
			V_{DD} = 1.65V to 2.2V	1.2		3.6	
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), CS# ≥ V_{DD} – 0.2V	Com.	-	10	50	mA
			Ind.	-	-	60	
			Auto	-	-	100	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. If CS# ≥ VDD–0.2V, all other inputs including UB# and LB# must meet this condition.
2. Typical values are measured at V_{DD} = V_{DR} (Min), T_A = 25 °C and not 100% tested.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

IS61/64WV1024EDALL (1.65V – 2.2V)

Industrial Range: -40°C to +85°C, Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
10	**Contact ISSI MKT for 10ns**	
12	IS61WV102416EDALL-12BI	mini BGA (6mm x 8mm)
12	IS61WV102416EDALL-12BLI	mini BGA (6mm x 8mm), Lead-free
12	IS61WV102416EDALL-12B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS61WV102416EDALL-12B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS61WV102416EDALL-12TLI	TSOP (Type I) , Lead-free
12	IS61WV102416EDALL-12T2LI	TSOP (Type I), ERR1/ERR2 Pins , Lead-free

Automotive (A3) Range: –40°C to +125°C, Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
12	IS64WV102416EDALL-12BA3	mini BGA (6mm x 8mm)
12	IS64WV102416EDALL-12BLA3	mini BGA (6mm x 8mm), Lead-free
12	IS64WV102416EDALL-12B2A3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV102416EDALL-12B2LA3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV102416EDALL-12CTLA3	TSOP (Type I), Copper Leadframe, Lead-free
12	IS64WV102416EDALL-12CT2LA3	TSOP (Type I), ERR1/ERR2 Pins, Copper Leadframe, Lead-free

IS61/64WV1024EDALL (2.2V - 3.6V)

Commercial Range: 0°C to +70°C, Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS61WV102416EDBLL-10B	mini BGA (6mm x 8mm)
10	IS61WV102416EDBLL-10BL	mini BGA (6mm x 8mm), Lead-free
10	IS61WV102416EDBLL-10B2	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS61WV102416EDBLL-10B2L	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS61WV102416EDBLL-10TL	TSOP (Type I) , Lead-free
10	IS61WV102416EDBLL-10T2L	TSOP (Type I), ERR1/ERR2 Pins , Lead-free

Industrial Range: -40°C to +85°C, Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS61WV102416EDBLL-10BI	mini BGA (6mm x 8mm)
10	IS61WV102416EDBLL-10BLI	mini BGA (6mm x 8mm), Lead-free
10	IS61WV102416EDBLL-10B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS61WV102416EDBLL-10B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS61WV102416EDBLL-10TLI	TSOP (Type I) , Lead-free
10	IS61WV102416EDBLL-10T2LI	TSOP (Type I), ERR1/ERR2 Pins , Lead-free

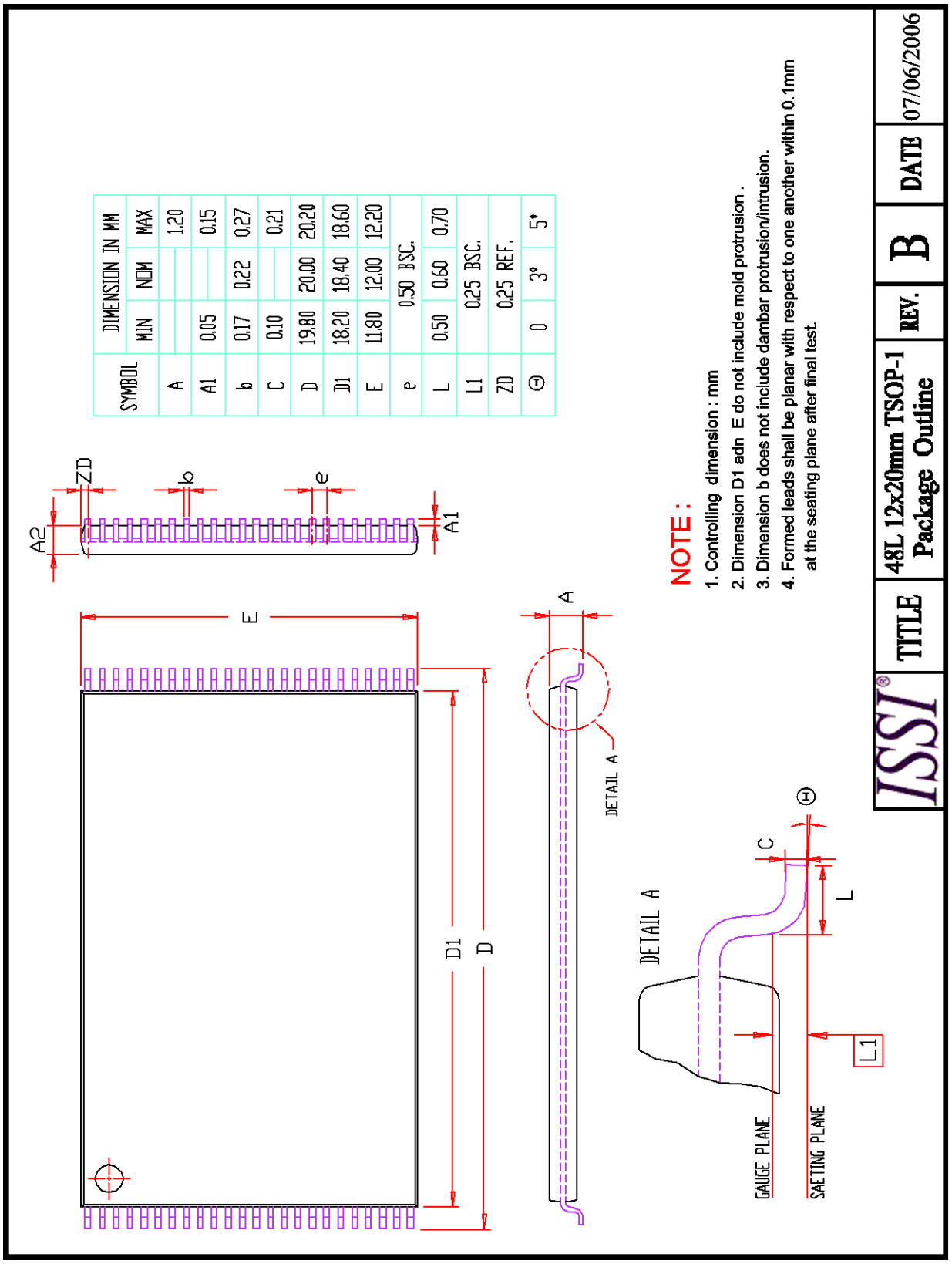
*Contact ISSI MKT for B3/B4 (A19 on H6) BGA Packages.

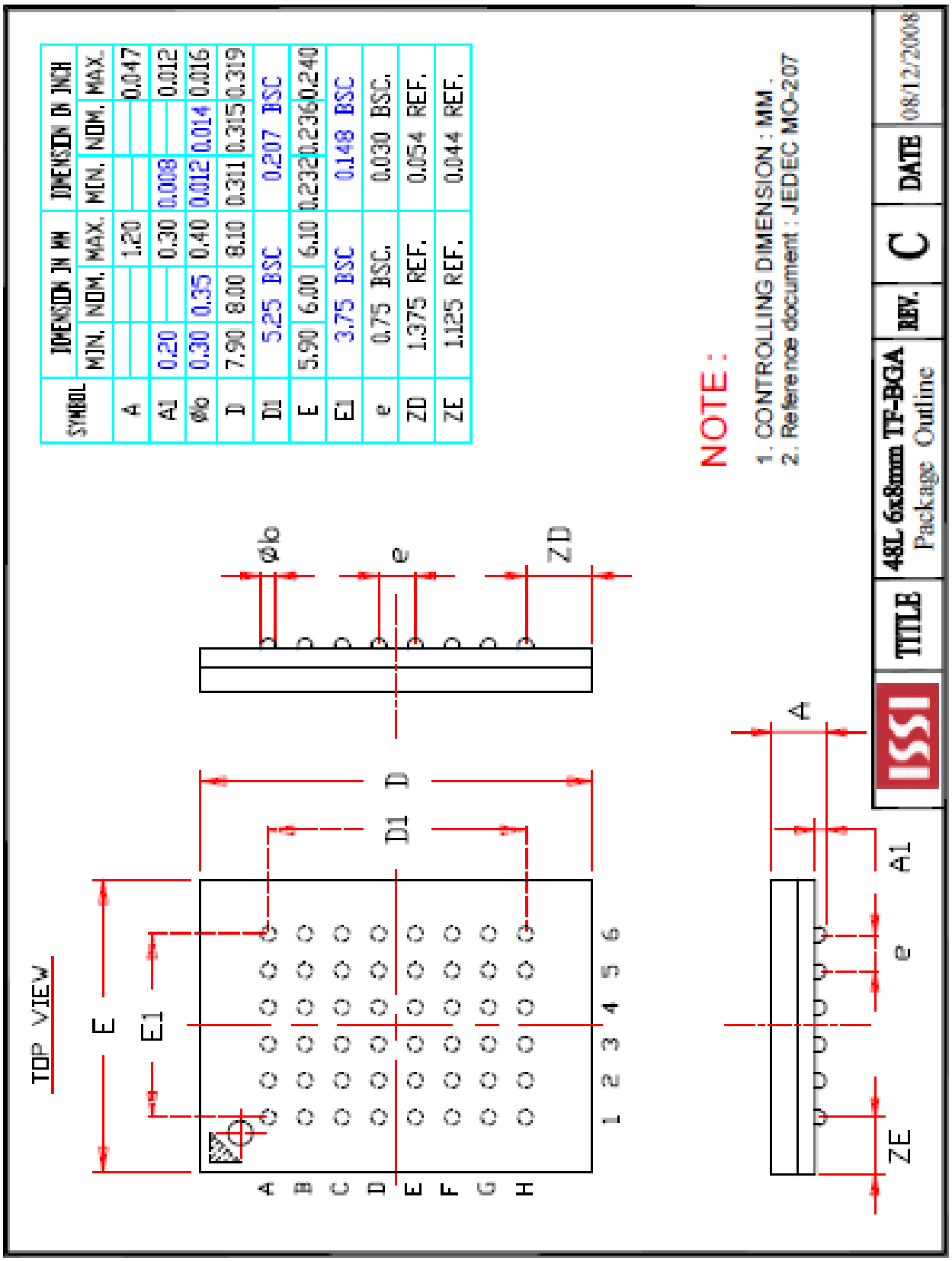
Automotive (A3) Range: –40°C to +125°C, Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
12	IS64WV102416EDBLL-12BA3	mini BGA (6mm x 8mm)
12	IS64WV102416EDBLL-12BLA3	mini BGA (6mm x 8mm), Lead-free
12	IS64WV102416EDBLL-12B2A3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV102416EDBLL-12B2LA3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV102416EDBLL-12CTLA3	TSOP (Type I), Copper Leadframe, Lead-free
12	IS64WV102416EDBLL-12CT2LA3	TSOP (Type I), ERR1/ERR2 Pins, Copper Leadframe, Lead-free

*Contact ISSI MKT for B3/B4 (A19 on H6) BGA Packages.

PACKAGE INFORMATION




SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
ϕb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008
TOP VIEW
ϕb
e
ZD
D
D1
E
E1
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H