12MHz and 60/72MHz output Clock Generator
AK8153A

Features

- **Input Frequency:**
  60.0MHz（SEL= L）
  72.0MHz（SEL= H）
- **Output Frequency:**
  12M:12MHz
  REF: 60.0MHz （SEL= L）
  72.0MHz （SEL= H）
- **Low Jitter Performance:**
  Longterm jitter（p-p）:125 ps
  （1000cycles delay, 10σ）
- **Low Current Consumption:**
  6.4 mW max.
- **Output Load:**
  12M: 12pF Max
  REF: 25pF Max
- **Supply Voltage:**
  VDD : 1.8V±0.1V
- **Operating Temperature Range:**
  -30 to +80℃
- **Package:**
  6-pin USON (1.4mm x 1.4mm)

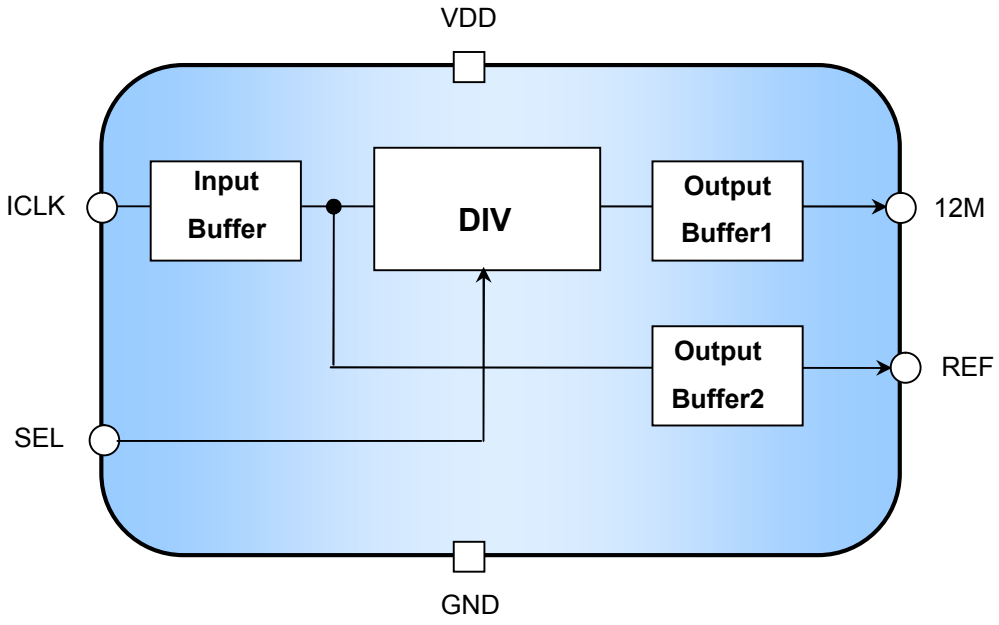
Description

The AK8153A is a high performance clock generator IC with two outputs. It generates 12MHz clock by dividing 60M or 72MHz input clock. And also outputs REF clock which is to be ICLK.
AK8153A provides very low jitter and highly accurate clock output without an external crystal.

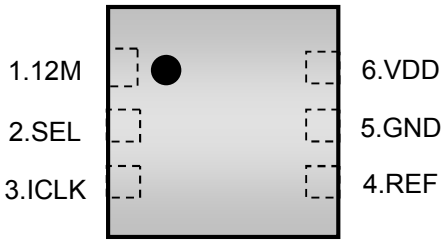
Applications

- Digital Still Camera
- Digital Video Camera

Block Diagram



PIN DESCRIPTION



Package: 6-Pin USON (Top View)
***lead-free**

Pin No.	Pin Name	Pin Type	Description
1	12M	OUT	12MHz output.
2	SEL	IN	Input Clock frequency select. "L": 60.0MHz, "H": 72.0MHz
3	ICLK	IN	60 MHz or 72 MHz input. 1.8V available. Input frequency is selected by SEL pin setting.
4	REF	OUT	Reference clock output. The signal input to the ICLK pin is output.
5	GND	--	Ground.
6	VDD	--	Power supply.

Input frequency Setting

SEL	ICLK Frequency	Output pin	Output Frequency
L	60.00 MHz	12M	12.00MHz
		REF	60.00MHz
H	72.00 MHz	12M	12.00MHz
		REF	72.00MHz

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8153A	53A	Tape and Reel	6-pin USON	-30 to 80 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	Vin	VSS-0.3 to 3.6	V
Input Current (any pins except supplies)	I_{IN}	±10	mA
Storage Temperature	Tstg	-55 to 130	°C

Note:

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature	Ta		-30		80	°C
Supply Voltage	VDD		1.7	1.8	1.9	V
Input Clock Frequency	Fin	SEL=L		60.0		MHz
		SELH		72.0		
Input Clock Duty Cycle		At 1/2 level of ICLK amplitude		50		%
Output Load Capacitance	Cp	Pin: 12M			12	pF
		Pin: REF			25	

DC Characteristics

All specifications at VDD: 1.7 to 1.9V, Ta: -30 to +80℃, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}	Pin: ICLK, SEL	0.8*VDD			V
Low level input voltage	V_{IL}				0.2*VDD	V
Input leakage current	I_L	Pin: ICLK, SEL	-10		+10	μA
High level output voltage	V_{OH}	12M IOH= -3mA	0.8*VDD1			V
		REF IOH= -7mA	0.9*VDD2			
Low level output voltage	V_{OL}	12M IOH= +3mA			0.2*VDD1	V
		REF IOH= +7mA			0.1*VDD2	
Power Consumption	W	No load VDD=1.8V			6.4	mW

AC Characteristics

All specifications at VDD: 1.7 to 1.9V,Ta: -30 to +80℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Frequency 1	fo1	Pin: 12M		12.00		MHz
Output Clock Frequency 2	fo2	Pin: REF SEL=L		60.00		MHz
		Pin: REF SEL=H		72.00		MHz
Output Clock Duty Cycle 1(1) (2)		Pin: 12M Cp=12pF	45	50	55	%
Output Clock Duty Cycle 2(1) (2)		Pin: REF Cp=25pF	40	50	60	%
Output Clock Rise Time(1)	t_{rise}	Pin: 12M 0.2VDD to 0.8VDD, Cp=12pF			4.0	ns
		Pin: REF 0.1VDD to 0.9VDD, Cp=25pF			1.9	
Output Clock Fall Time(1)	t_{fall}	Pin: 12M 0.2VDD to 0.8VDD, Cp=12pF			4.0	ns
		Pin: REF 0.1VDD to 0.9VDD, Cp=25pF			1.9	
Period Jitter (1)	Jit	Pin: 12M 1σ,Cp=12pF		25		ps
Cycle to Cycle Jitter(1)	Jit	Pin: 12M 1σ,Cp=12pF		50		ps
Longterm Jitter(1)	Jit	Pin: REF 1000 cycles delay, 10σ in 10000 sampling, Cp=25pF			125	ps
Output Stable Time(3)	t_{lock}	Pin:12M, REF no load			0.2	ms

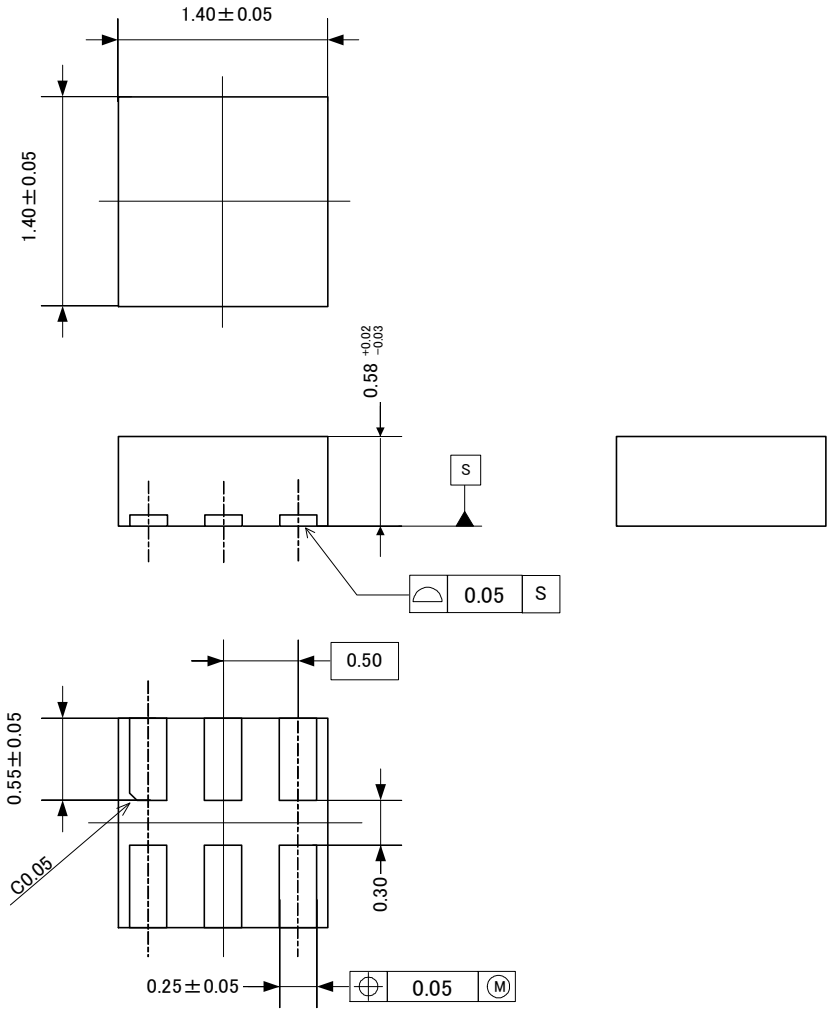
(1) Design value

(2) When the Input clock duty cycle is 50% at 1/2 level of ICLK amplitude

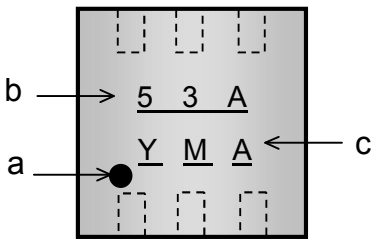
(3) The time that output reaches the target frequency within accuracy of ±0.1% from the point that the ICLK signal starts to be input

Package Information

- **Mechanical data (Units:mm)**



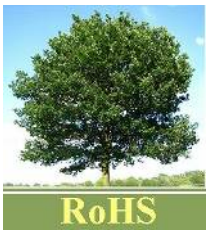
- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (3 digits)

AKM and the logo - - are the brand of AKM's IC's and identify that AKM continues to offer the best choice for high performance mixed-signal solution under this brand.

RoHS Compliance



All integrated circuits form Asahi Kasei Microdevices (AKM) assembled in "lead-free" packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.