

E3M0045065K

Silicon Carbide Power MOSFET
E-Series Automotive
N-Channel Enhancement Mode



Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

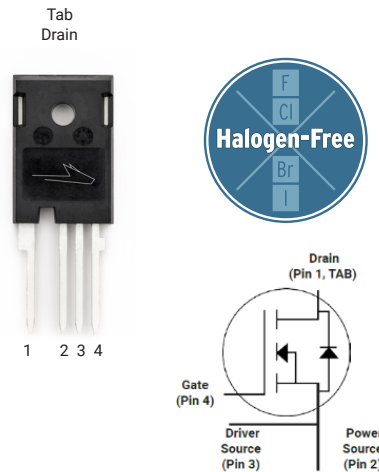
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

Package



| Part Number | Package | Marking |
|-------------|-----------|-------------|
| E3M0045065K | TO-247-4L | E3M0045065K |

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Value | Unit | Note | |
|----------------|---|---------------------------|------------------|--------------------|--------------------|
| V_{DSmax} | Drain - Source Voltage | 650 | V | | |
| V_{GSmax} | Gate - Source Voltage | -8/+19 | V | Note: 1 | |
| I_D | Continuous Drain Current, $V_{GS} = 15\text{ V}$ | $T_c = 25^\circ\text{C}$ | 46 | A | Fig. 19 Note: 2 |
| | | $T_c = 100^\circ\text{C}$ | 33 | | |
| $I_{D(pulse)}$ | Pulsed Drain Current, Pulse width t_p limited by T_{jmax} | 132 | A | Fig. 22 | |
| P_D | Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 175^\circ\text{C}$ | 150 | W | Fig. 20 Note: 2 | |
| T_j, T_{stg} | Operating Junction and Storage Temperature | -40 to +175 | $^\circ\text{C}$ | | |
| T_L | Solder Temperature, 1.6mm (0.063") from case for 10s | 260 | $^\circ\text{C}$ | | |
| M_d | Mounting Torque , M3 or 6-32 screw | 1 | Nm lbf-in | | |
| | | 8.8 | | | |

Note (1): Recommended turn off / turn on gate voltage $V_{GS} = -4V...0V / +15V$

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---------------|---|------|------|------|---------------|--|--------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 650 | | | V | $V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$ | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.8 | 2.8 | 3.6 | V | $V_{DS} = V_{GS}, I_D = 4.84\ \text{mA}$ | Fig. 11 |
| | | | 2.2 | | V | $V_{DS} = V_{GS}, I_D = 4.84\ \text{mA}, T_J = 175^\circ\text{C}$ | |
| I_{DSS} | Zero Gate Voltage Drain Current | | 1 | 50 | μA | $V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$ | |
| I_{GSS} | Gate-Source Leakage Current | | 10 | 250 | nA | $V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$ | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | | 45 | 60 | m Ω | $V_{GS} = 15\ \text{V}, I_D = 17.6\ \text{A}$ | Fig. 4, 5, 6 |
| | | | 63 | | | $V_{GS} = 15\ \text{V}, I_D = 17.6\ \text{A}, T_J = 175^\circ\text{C}$ | |
| g_{fs} | Transconductance | | 25 | | S | $V_{DS} = 20\ \text{V}, I_{DS} = 17.6\ \text{A}$ | Fig. 7 |
| | | | 24 | | | $V_{DS} = 20\ \text{V}, I_{DS} = 17.6\ \text{A}, T_J = 175^\circ\text{C}$ | |
| C_{iss} | Input Capacitance | | 1593 | | pF | $V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$ $F = 1\ \text{MHz}$ $V_{AC} = 25\ \text{mV}$ | Fig. 17, 18 |
| C_{oss} | Output Capacitance | | 99 | | | | |
| C_{rss} | Reverse Transfer Capacitance | | 7 | | | | |
| E_{oss} | C_{oss} Stored Energy | | 10 | | μJ | | Fig. 16 |
| $C_{o(er)}$ | Effective Output Capacitance (Energy Related) | | 122 | | pF | $V_{GS} = 0\ \text{V}, V_{DS} = 0... 400\ \text{V}$ | Note: 3 |
| $C_{o(tr)}$ | Effective Output Capacitance (Time Related) | | 179 | | pF | | |
| E_{oN} | Turn-On Switching Energy (External Diode) | | 51 | | μJ | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 17.6\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 99\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE | Fig. 26, 28 |
| E_{oOFF} | Turn Off Switching Energy (External Diode) | | 18 | | | | |
| E_{oN} | Turn-On Switching Energy (Body Diode FWD) | | 68 | | μJ | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 17.6\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 99\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode | Fig. 26, 28 |
| E_{oOFF} | Turn-Off Switching Energy (Body Diode FWD) | | 13 | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | | 9 | | ns | $V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 17.6\ \text{A}, R_{G(ext)} = 2.5\ \Omega,$ Timing relative to V_{DS} Inductive load | Fig. 27, 28 |
| t_r | Rise Time | | 12 | | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | 19 | | | | |
| t_f | Fall Time | | 7 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 3 | | Ω | $f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$ | |
| Q_{gs} | Gate to Source Charge | | 20 | | nC | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 17.6\ \text{A}$ Per IEC60747-8-4 pg 21 | Fig. 12 |
| Q_{gd} | Gate to Drain Charge | | 19 | | | | |
| Q_g | Total Gate Charge | | 64 | | | | |

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V


Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|----------------|----------------------------------|------|------|------|---|---------------|
| V_{SD} | Diode Forward Voltage | 4.7 | | V | $V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 25^\circ\text{C}$ | Fig. 8, 9, 10 |
| | | 4.2 | | V | $V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 175^\circ\text{C}$ | |
| I_S | Continuous Diode Forward Current | | 26 | A | $V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$ | |
| $I_{S, pulse}$ | Diode pulse Current | | 132 | A | $V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax} | |
| t_{rr} | Reverse Recover time | 12 | | ns | $V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $dif/dt = 4590\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$ | |
| Q_{rr} | Reverse Recovery Charge | 210 | | nC | | |
| I_{rrm} | Peak Reverse Recovery Current | 34 | | A | | |
| t_{rr} | Reverse Recover time | 14 | | ns | $V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2140\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$ | |
| Q_{rr} | Reverse Recovery Charge | 142 | | nC | | |
| I_{rrm} | Peak Reverse Recovery Current | 16 | | A | | |

Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|-----------------|--|------|------|---------------------------|-----------------|---------|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 0.79 | 1 | $^\circ\text{C}/\text{W}$ | | Fig. 21 |



Typical Performance

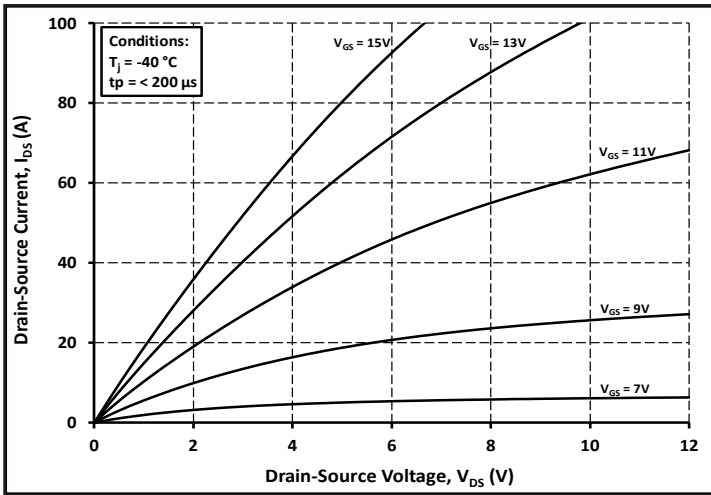


Figure 1. Output Characteristics $T_j = -40\text{ }^\circ\text{C}$

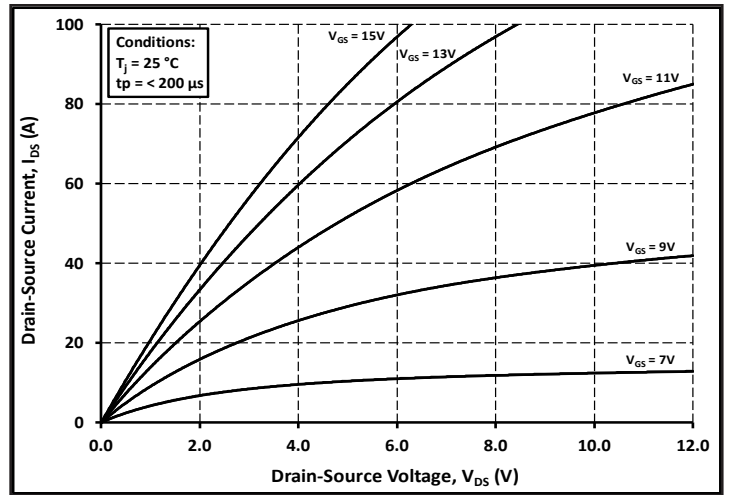


Figure 2. Output Characteristics $T_j = 25\text{ }^\circ\text{C}$

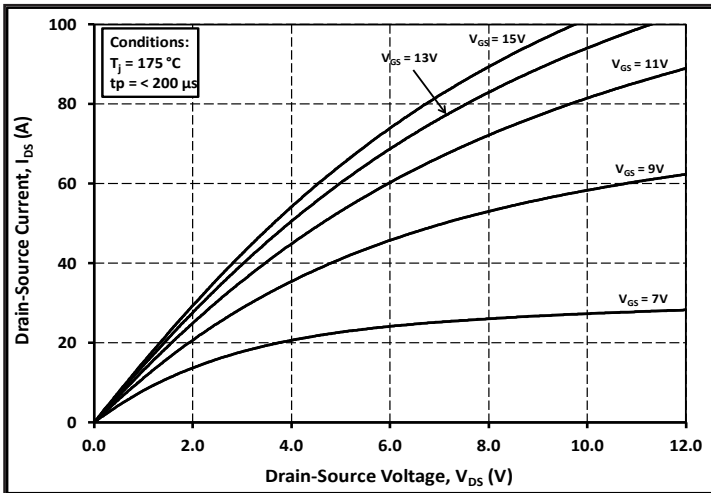


Figure 3. Output Characteristics $T_j = 175\text{ }^\circ\text{C}$

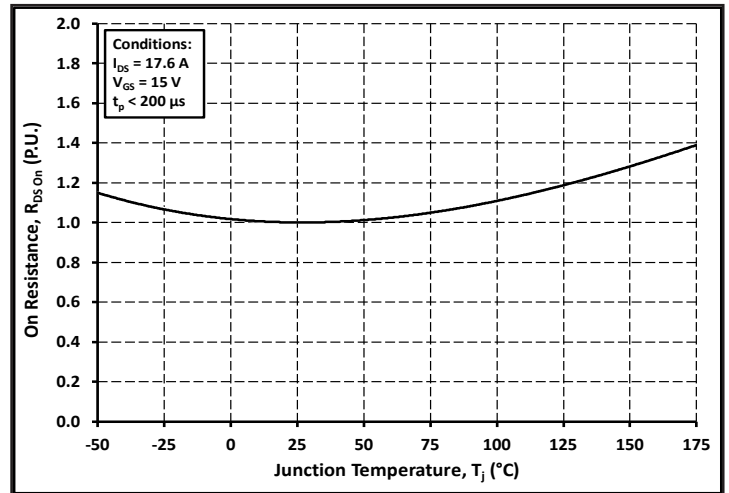


Figure 4. Normalized On-Resistance vs. Temperature

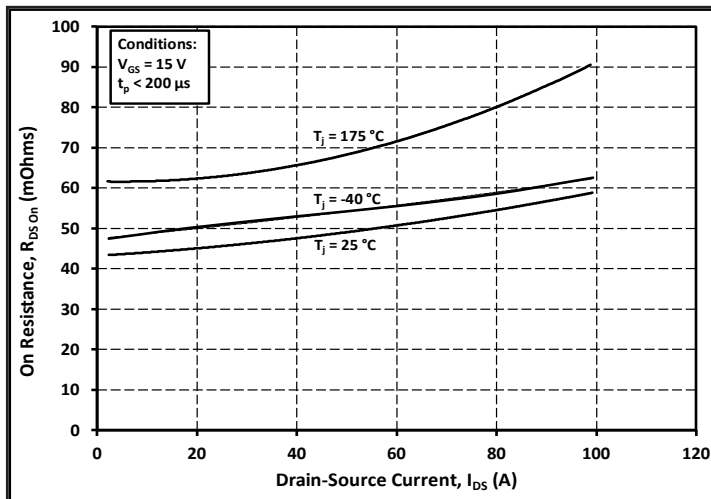


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

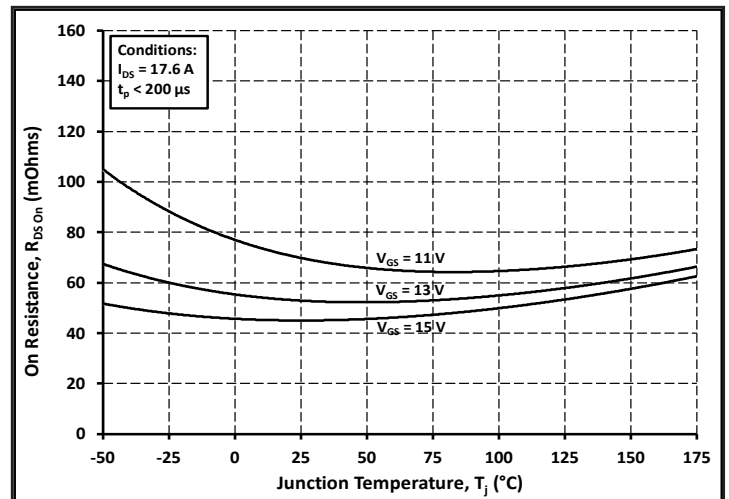


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

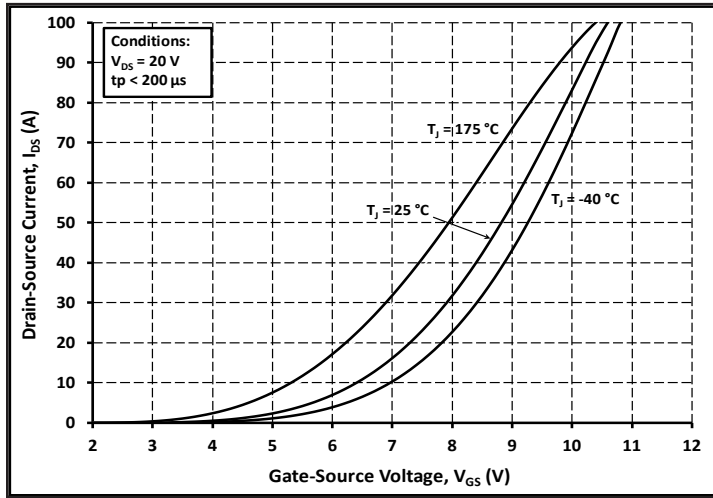


Figure 7. Transfer Characteristic for Various Junction Temperatures

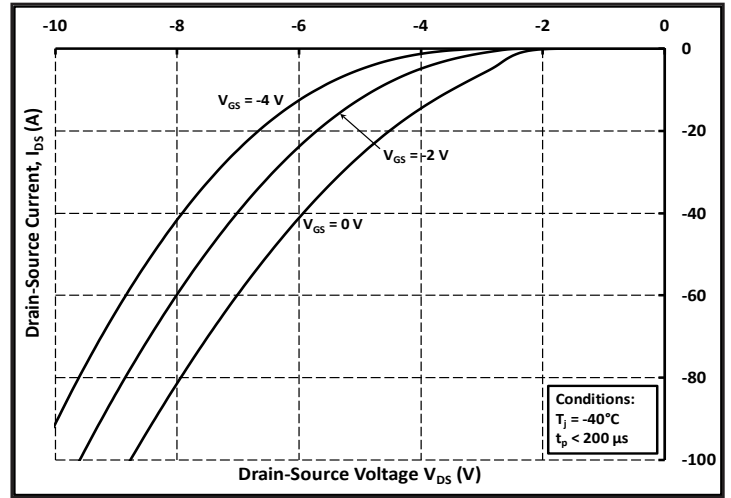


Figure 8. Body Diode Characteristic at -40 °C

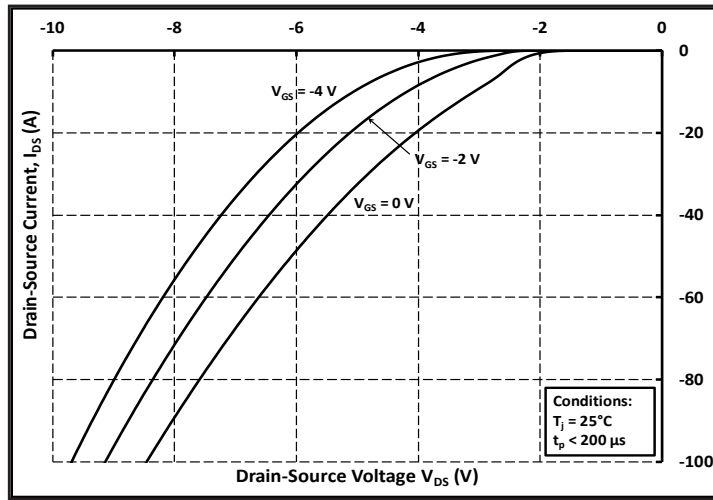


Figure 9. Body Diode Characteristic at 25 °C

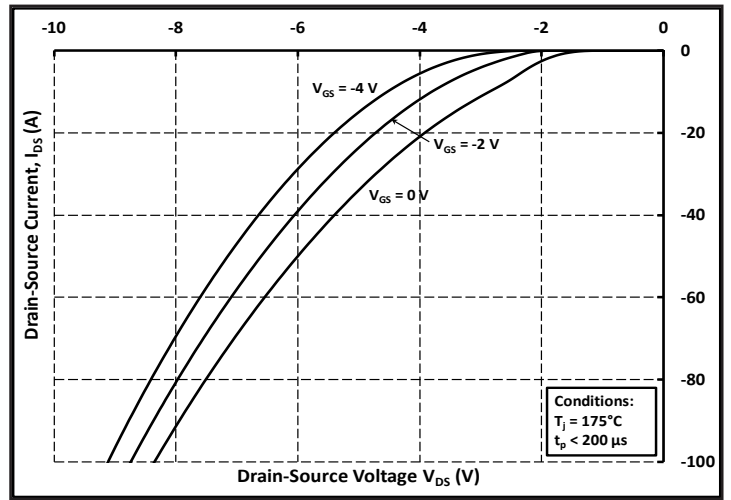


Figure 10. Body Diode Characteristic at 175 °C

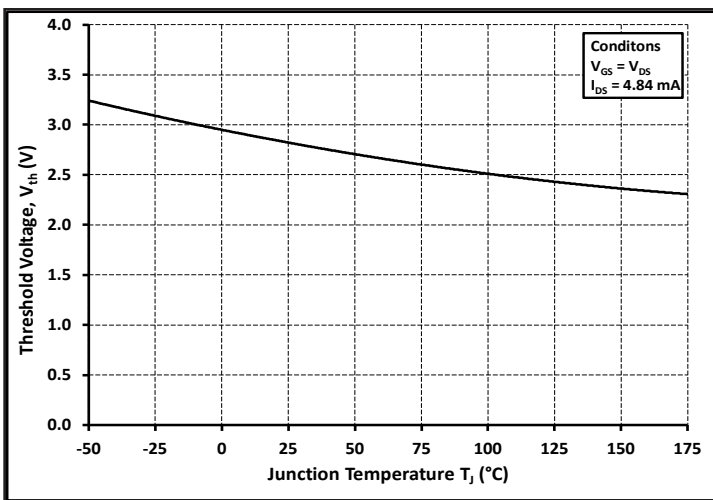


Figure 11. Threshold Voltage vs. Temperature

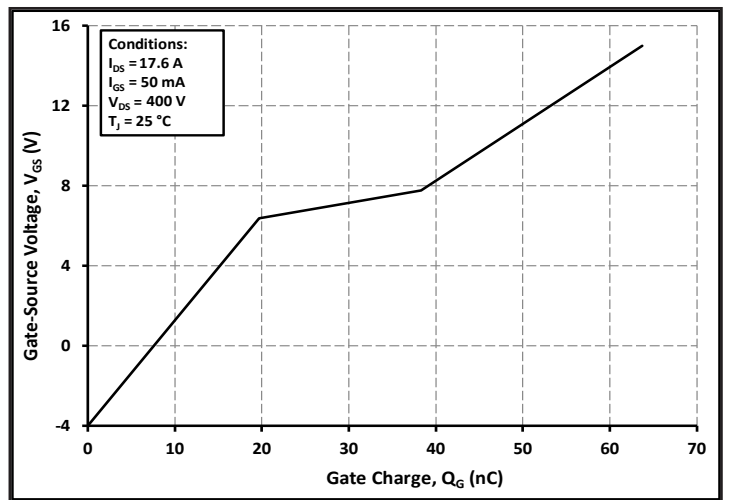


Figure 12. Gate Charge Characteristics



Typical Performance

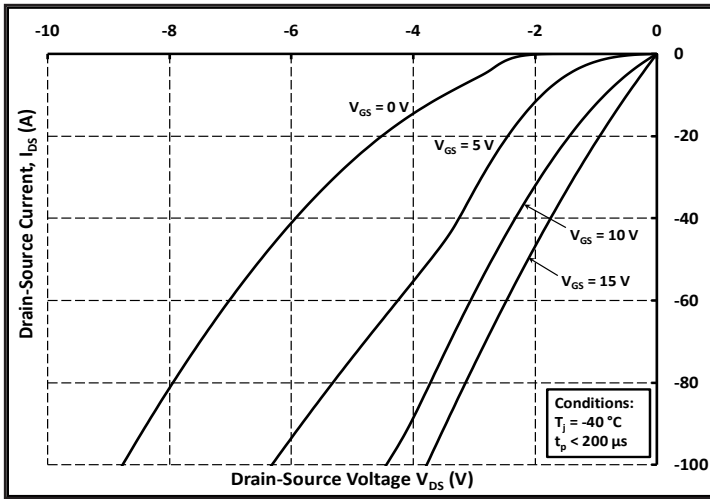


Figure 13. 3rd Quadrant Characteristic at -40 °C

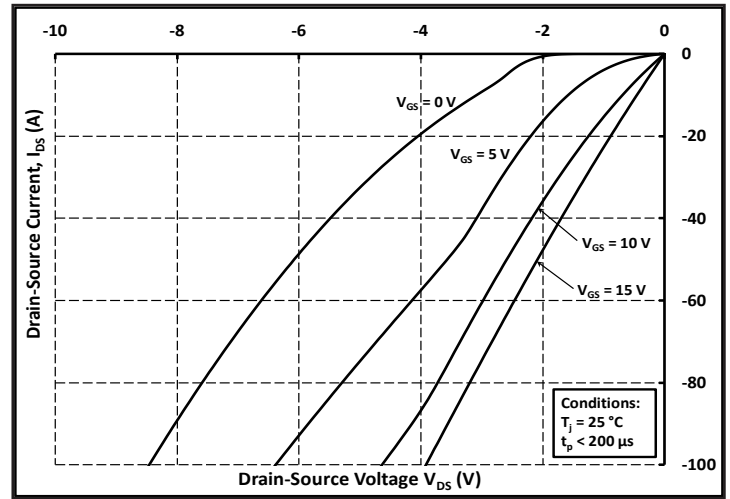


Figure 14. 3rd Quadrant Characteristic at 25 °C

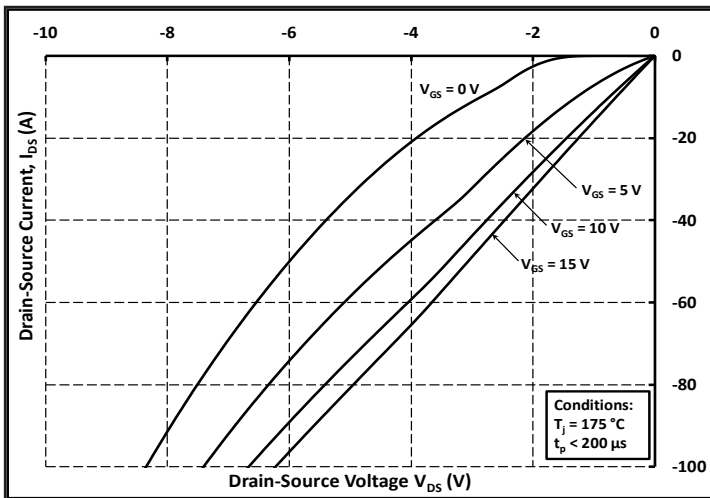


Figure 15. 3rd Quadrant Characteristic at 175 °C

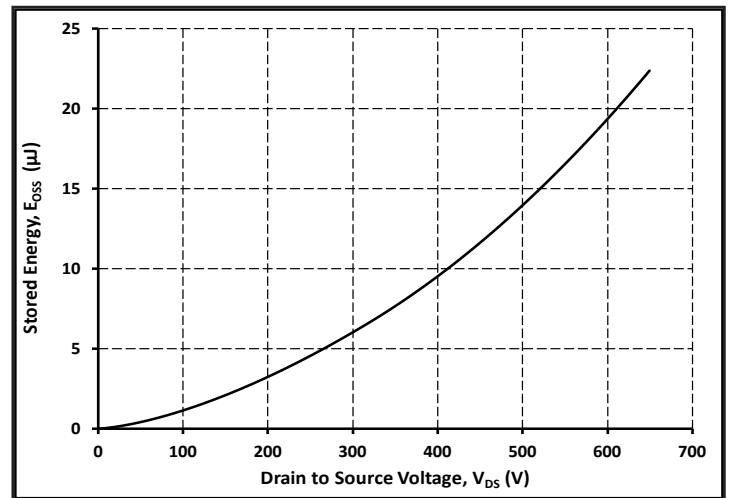


Figure 16. Output Capacitor Stored Energy

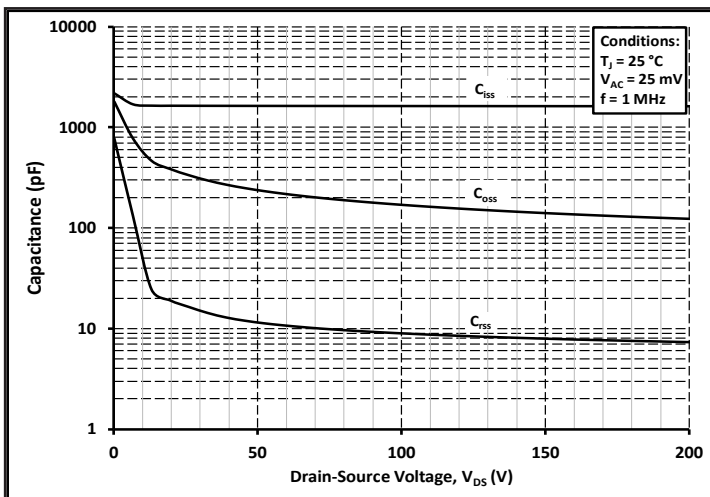


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

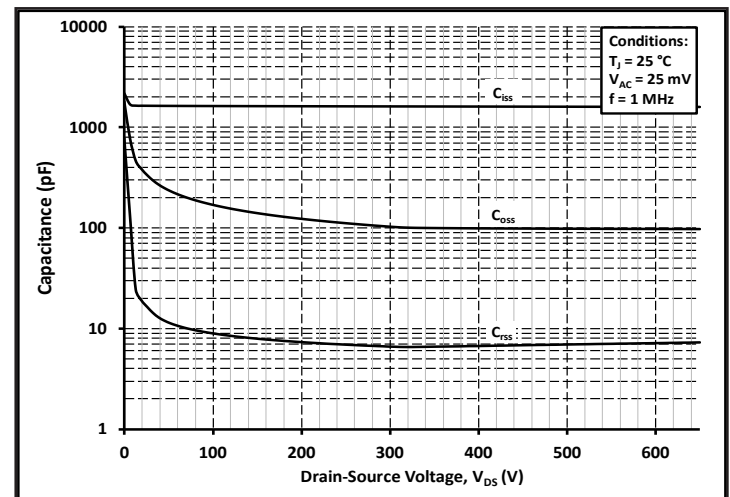


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)



Typical Performance

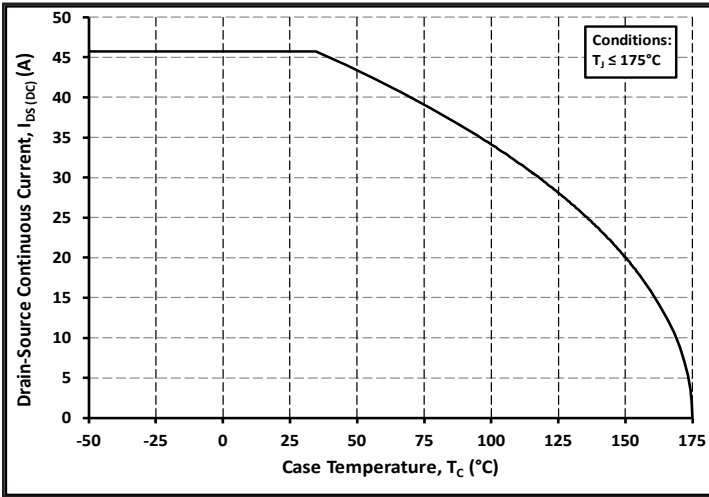


Figure 19. Continuous Drain Current Derating vs. Case Temperature

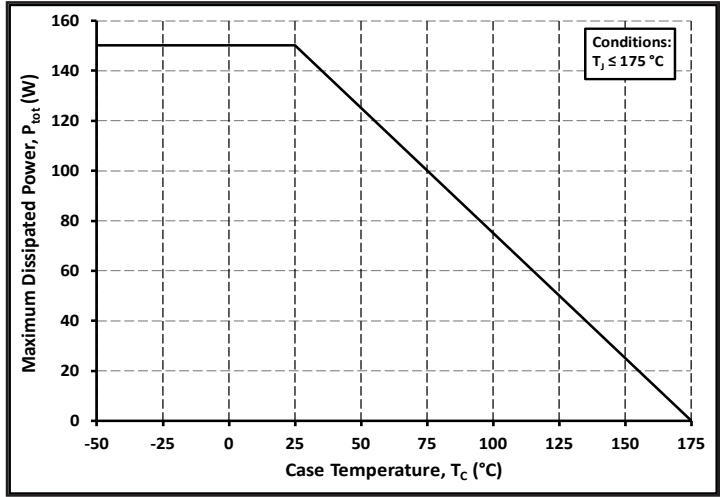


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

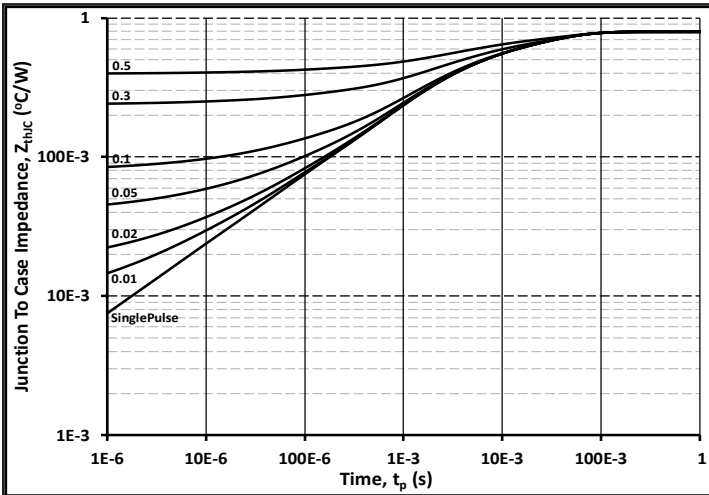


Figure 21. Transient Thermal Impedance (Junction - Case)

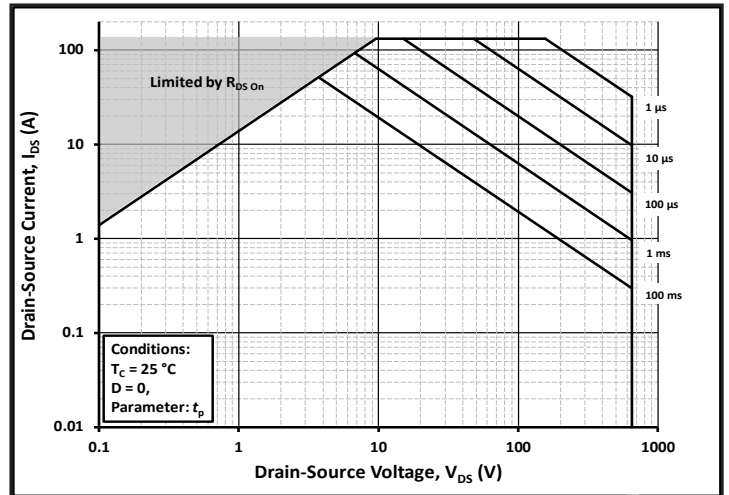


Figure 22. Safe Operating Area

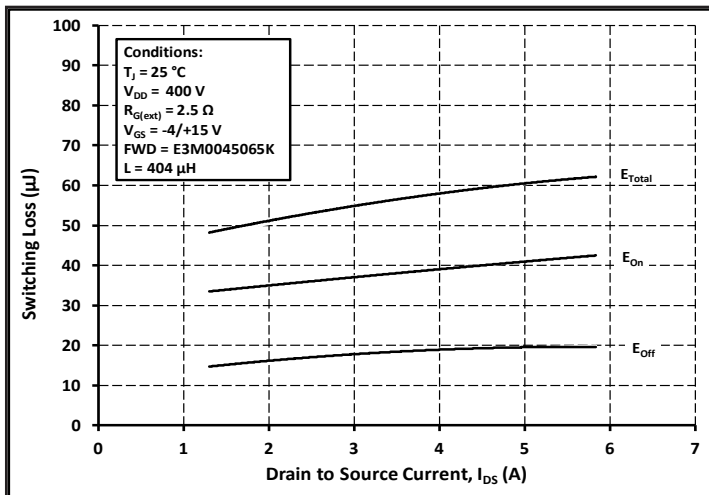


Figure 23. Clamped Inductive Switching Energy vs. Low Drain Current ($V_{DD} = 400V$)

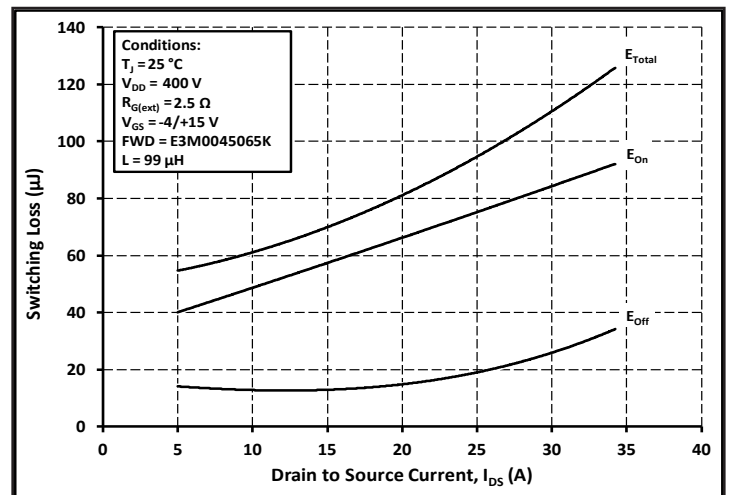


Figure 24. Clamped Inductive Switching Energy vs. High Drain Current ($V_{DD} = 400V$)

Typical Performance

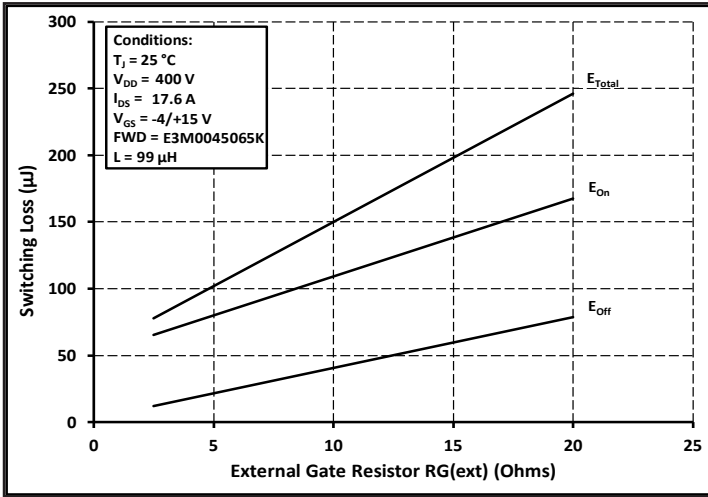


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

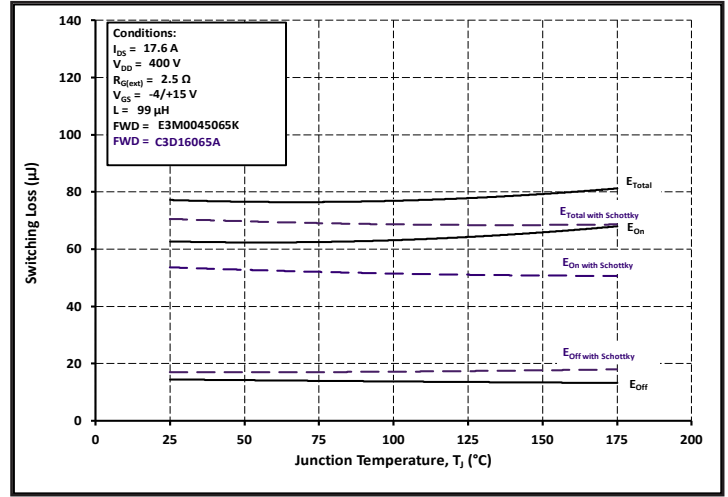


Figure 26. Clamped Inductive Switching Energy vs. Temperature

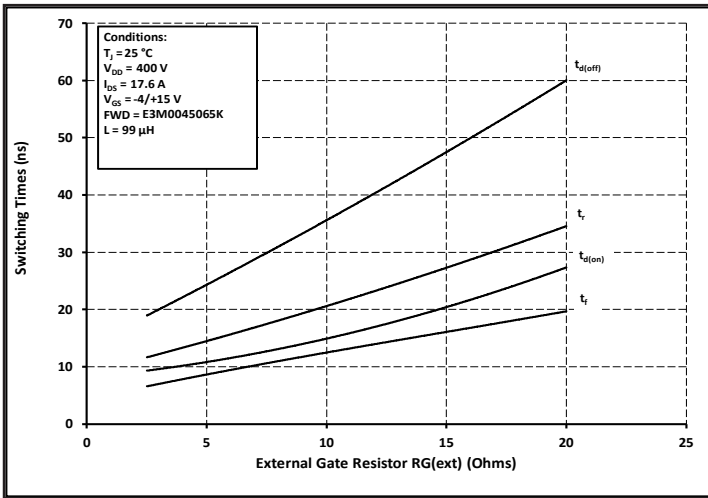


Figure 27. Switching Times vs. $R_{G(ext)}$

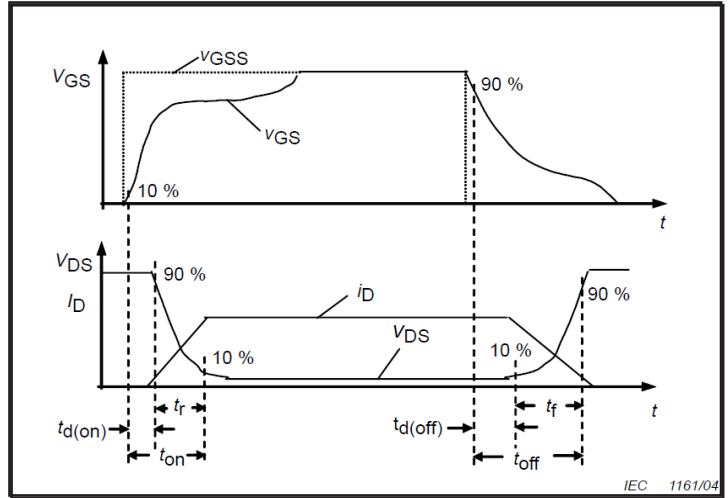


Figure 28. Switching Times Definition

Test Circuit Schematic

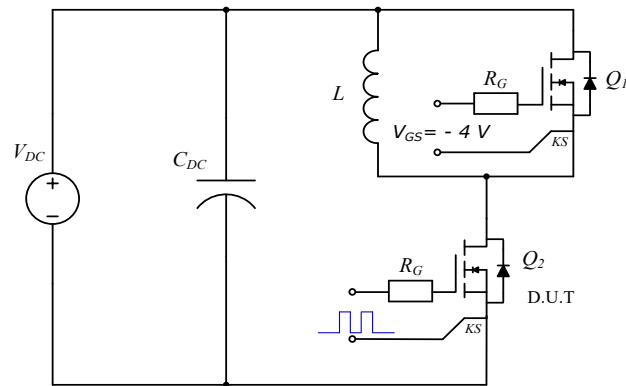
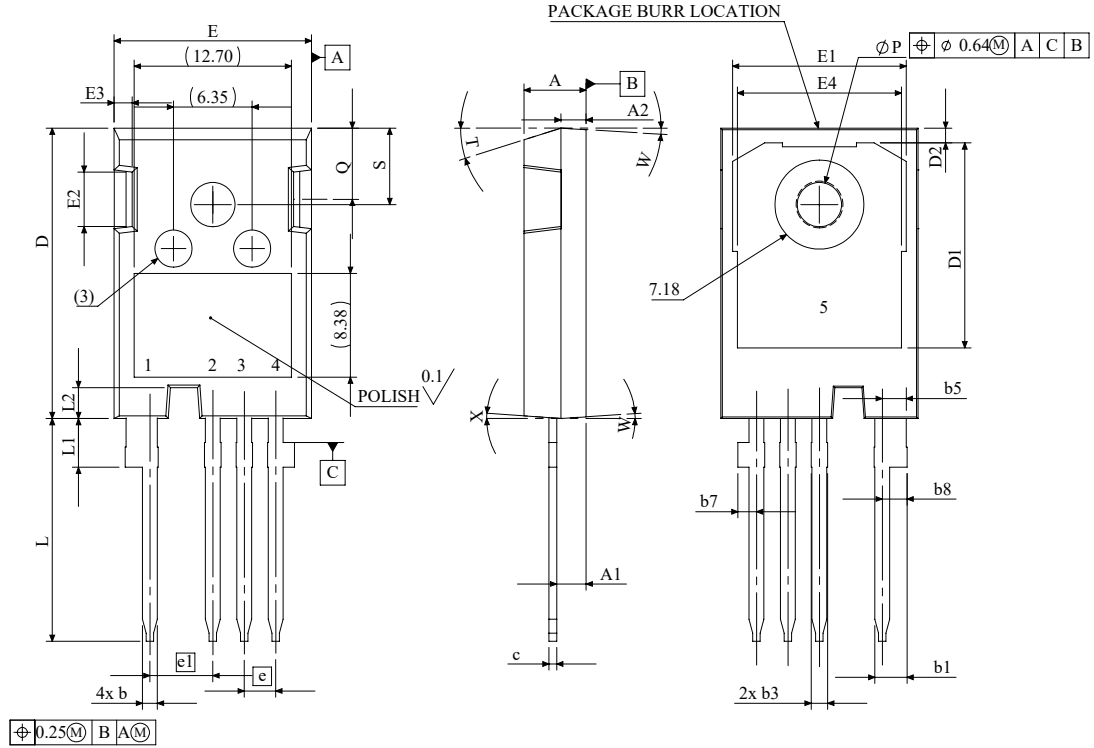


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



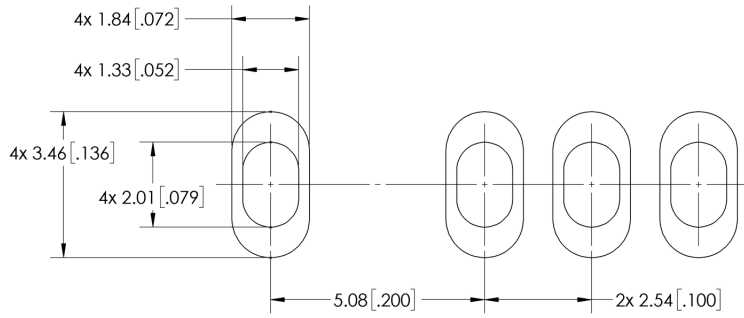
| | |
|---|---------------|
| 1 | DRAIN |
| 2 | SOURCE |
| 3 | DRIVER SOURCE |
| 4 | GATE |
| 5 | DRAIN |

NOTE:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



Recommended Solder Pad Layout





Revision history

| Document Version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| 1.0 | November-2022 | Initial datasheet |



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