**02311FAP-C**

Huawei® 02311FAP Compatible TAA 100GBase-ER4 CFP2 Transceiver (SMF, 1310nm, 40km, LC, DOM)

**Features:**

- CFP MSA 1.0 Compliance
- Duplex LC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

**Applications:**

- 100GBase Ethernet
- Access and Enterprise

**Product Description**

This Huawei® 02311FAP compatible CFP2 transceiver provides 100GBase-ER4 throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Huawei® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

**Rev. 051623**

**Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| **Storage Temperature** | $T_S$ | -40 | 85 | ℃ |
| **Supply Voltage** | Vcc | -0.5 | 3.6 | V |
| **Operating Relative Humidity** | RH | 0 | 85 | % |

**Note:**

1. Exceeding any one of these values may destroy the device immediately.

**Recommended Operating Conditions**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Operating Case Temperature** | TC | 0 | | 70 | ℃ |
| **Power Supply Voltage** | Vcc | 3.14 | 3.3 | 3.46 | V |
| **Data Rate** | DR | | 103.2 | 112 | Gb/s |

## Electrical Characteristics

| Parameter | | | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| **Voltage Supply Electrical Characteristics** | | | | | | | | |
| **Supply Current** | **Tx Section** | | Icc | A | | | 3.75 | 1 |
| | **Rx Section** | | | | | | | |
| **Power Supply Noise** | | | Vrip | | | | 2% DC | 1MHz |
| | | | | | | | 3% 1 | 10MHz |
| **Total Dissipation Power** | **Class1** | | Pw | W | | | 3 | |
| | **Class2** | | | | | | 6 | |
| | **Class3** | | | | | | 9 | |
| | **Class4** | | | | | | 12 | |
| **Low Power Mode Dissipation** | | | Plow | W | | | 2 | |
| **Inrush Current** | **Class1** | **and** | I-inrush | mA/usec | | | 100 | |
| **Turn-off Current** | **Class2** | | I-turnoff | mA/usec | -100 | | | |
| **Inrush Current** | **Class3** | **and** | I-inrush | mA/usec | | | 200 | |
| **Turn-off Current** | **Class4** | | I-turnoff | mA/usec | -200 | | | |
| **Different Signal Electrical Characteristics** | | | | | | | | |
| **Single Ended Data Input Swing** | | | | mV | 20 | | 525 | |
| **Single Ended Data Output Swing** | | | | mV | 180 | | 385 | |
| **Differential Signal Output Resistance** | | | | Ω | 80 | | 120 | |
| **Differential Signal Input Resistance** | | | | Ω | 80 | | 120 | |
| **3.3V LVCMOS Electrical Characteristics** | | | | | | | | |
| **Input High Voltage** | | | 3.3VIH | V | 2.0 | | Vcc+0.3 | |
| **Input Low Voltage** | | | 3.3VIL | V | -0.3 | | 0.8 | |
| **Input Leakage Current** | | | 3.3IIN | uA | -10 | | +10 | |
| **Output High Voltage (IOH=100uA)** | | | 3.3VOH | V | Vcc-0.2 | | | |
| **Output Low Voltage (IOL=100uA)** | | | 3.3VOL | V | | | 0.2 | |
| **Minimum Pulse Width of Control Pin Signal** | | | t_CNTL | us | 100 | | | |
| **1.2V LVCMOS Electrical Characteristics** | | | | | | | | |
| **Input High Voltage** | | | 1.2VIH | V | 0.84 | | 1.5 | |
| **Input Low Voltage** | | | 1.2VIL V | 0.3 | 1.2VIL V | | 0.36 | |
| **Input Leakage Current** | | | 1.2IIN | uA | -100 | | +100 | |
| **Output High Voltage** | | | 1.2VOH | V | 1.0 | | 1.5 | |
| **Output Low Voltage** | | | 1.2VOL | V | -0.3 | | 0.2 | |
| **Output High Current** | | | 1.2IOH | mA | | | -4 | |
| **Output Low Current** | | | 1.2IOL | mA | +4 | | | |
| **Input Capacitance** | | | Ci | pF | | | 10 | |

## High Speed Electrical Characteristics

| Parameter | Symbol | Unit | Min. | Max. | Notes |
|---|---|---|---|---|---|
| **Impedance** | Zd | Ω | 90 | 110 | |
| **Frequency** | | MHz | 161.1328125 | | 1/64 of electrical lane rate |
| **Frequency Stability** | △f | ppm | -100 | 100 | For Ethernet |
| | | | -20 | 20 | For Telecom |
| **Differential Voltage** | VDIFF | mV | 400 | 900 | Peak to Peak Differential |
| **Common mode noise (rms)** | | mV | | 17.5 | |
| **RMS jitter** | | ps | | 10 | Random Jitter Over frequency band of 10KHZ<f<10MHZ |
| **Clock Duty Cycle** | | % | 40 | 60 | |

## Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| **Signaling Rate per Lane** | | 25.78125 ±100 ppm | | | GBd | 9 |
| | | 27.9525 ±20 ppm | | | GBd | OTU4 |
| **Four Lane Wavelength Range** | λ1 | 1294.53 | 1295.56 | 1296.59 | nm | |
| | λ2 | 1299.02 | 1300.05 | 1301.09 | nm | |
| | λ3 | 1303.54 | 1304.58 | 1305.63 | nm | |
| | λ4 | 1308.09 | 1309.14 | 1310.19 | nm | |
| **Total launch power** | | | | 8.9 | dBm | 9 |
| **Average launch power, each lane** | Pavg | -2.9 | | 2.9 | dBm | 2 |
| **Optical modulation amplitude, each lane (OMA)2** | OMA | 0.1 | | 4.5 | dBm | |
| **Difference in launch power between any two lanes (OMA)** | | | | 3.6 | dB | |
| **Extinction ratio** | ER | 8 | | | dB | 9 |
| **Side-mode suppression ratio** | SMSR | 30 | | | dB | |
| **Transmitter and dispersion penalty, each lane** | TDP | | | 2.5 | dB | |
| **Optical return loss tolerance** | | | | 20 | dB | |
| **Transmitter reflectance3** | | | | –12 | dB | |
| **Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}** | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | 9 |
| **Receiver** | | | | | | |
| **Receive Rate for Each Lane** | | | 25.78125 | 27.9525 | Gbps | |
| **Overload Input Optical Power** | Pmax | 5.5 | | | dBm | 3 |
| **Average Receive Power for Each Lane** | Pin | -16 | | 4.5 | dBm | 4, 5 (- |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | 20.9) |
| **Receive Power in OMA for Each Lane** | PinOMA | | | 4.5 | dBm | |
| **Difference in Receive Power in OMA between Any Two Lanes** | | | | 4.5 | dBm | |
| **Receiver Sensitivity in OMA for Each Lane** | SOMA | | | -16 | dBm | 6 (-21.4) |
| **Stressed Receiver Sensitivity in OMA for Each Lane** | | | | -12 | dBm | 7, 8（-17.9） |

**Notes:**

1. The supply current includes CFP2 module's supply current and test board working current.
2. Average launch power, each lane (min) is informative for 100GBase-LR4, not the principal indicator of signal strength.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
4. The average receive power, each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
6. Receiver sensitivity (OMA), each lane (max) is informative
7. Measured with conformance test signal at TP3 for BER=10-12
8. Conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB; stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.
9. 100GBase-ER4

**Pin Descriptions**

| Pin | Name | I/O | Logic | Description |
|---|---|---|---|---|
| **1** | GND | | | |
| **2** | (TX_MCLKn) | O | CML | For optical waveform testing. Not for normal use. |
| **3** | (TX_MCLKp) | O | CML | For optical waveform testing. Not for normal use. |
| **4** | GND | | | |
| **5** | N.C | | | No Connect |
| **6** | N.C | | | 3.3V ± 5% |
| **7** | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| **8** | 3.3V_GND | | | 3.3V Module Supply Ground, internally connected to Signal Ground |
| **9** | 3.3V | | | 3.3V Module Supply Voltage |
| **10** | 3.3V | | | Module Vendor I/O B, NC |
| **11** | 3.3V | | | "1" or NC = transmitter disabled,<br>"0" = transmitter enabled |
| **12** | 3.3V | | | "1" = loss of signal (low optical signal), "0" = normal condition |
| **13** | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| **14** | 3.3V_GND | | | "1" or NC = module in low power (safe) mode,<br>"0" = power-on enabled |
| **15** | VND_IO_A | I/O | | Module Vendor I/O A. Do Not Connect! |
| **16** | VND_IO_B | I/O | | Module Vendor I/O A. Do Not Connect! |
| **17** | PRG_CNTL1 | I | LVCMOS w/ PUR | Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used |
| **18** | PRG_CNTL2 | I | LVCMOS w/ PUR | Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used |
| **19** | PRG_CNTL3 | I | LVCMOS w/ PUR | Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used |
| **20** | PRG_ALRM1 | O | LVCMOS | Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up |
| **21** | PRG_ALRM2 | O | LVCMOS | Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready. |
| **22** | PRG_ALRM3 | O | LVCMOS | Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault |
| **23** | GND | | | |
| **24** | TX_DIS | I | LVCMOS w/ PUR | Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled |
| **25** | RX_LOS | O | LVCMOS | Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition |
| **26** | MOD_LOPWR | I | LVCMOS w/ PUR | Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled |
| **27** | MOD_ABS | O | GND | Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host |
| **28** | MOD_RSTn | I | LVCMOS w/ PDR | Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module |
| **29** | GLB_ALRMn | O | LVCMOS | Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host |
| **30** | GND | | | |

| | | | | |
|---|---|---|---|---|
| **31** | MDC | I | 1.2VCMOS | Management Data Clock (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010) |
| **32** | MDIO | I/O | 1.2VCMOS | Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010) |
| **33** | PRTADR0 | I | 1.2VCMOS | MDIO Physical Port address bit 0 |
| **34** | PRTADR1 | I | 1.2VCMOS | MDIO Physical Port address bit 1 |
| **35** | PRTADR2 | I | 1.2VCMOS | MDIO Physical Port address bit 2 |
| **36** | VND_IO_C | I/O | | Module Vendor I/O C. Do Not Connect! |
| **37** | VND_IO_D | I/O | | Module Vendor I/O D. Do Not Connect! |
| **38** | VND_IO_E | I/O | | Module Vendor I/O E. Do Not Connect! |
| **39** | 3.3V_GND | | | |
| **40** | 3.3V_GND | | | |
| **41** | 3.3V | | | 3.3V Module Supply Voltage |
| **42** | 3.3V | | | 3.3V Module Supply Voltage |
| **43** | 3.3V | | | 3.3V Module Supply Voltage |
| **44** | 3.3V | | | 3.3V Module Supply Voltage |
| **45** | 3.3V_GND | | | |
| **46** | 3.3V_GND | | | |
| **47** | N.C | | | No Connect |
| **48** | N.C | | | |
| **49** | GND | | | |
| **50** | (RX_MCLKn) | O | CML | For optical waveform testing. Not for normal use. |
| **51** | (RX_MCLKp) | O | CML | For optical waveform testing. Not for normal use. |
| **52** | GND | | | |
| **53** | GND | | | |
| **54** | N.C. | | | |
| **55** | N.C. | | | |
| **56** | GND | | | |
| **57** | RX0p | | | 25 Gbps receiver data; Lane 0 |
| **58** | RX0n | | | 25 Gbps receiver data bar; Lane 0 |
| **59** | GND | | | |
| **60** | RX1p | | | 25 Gbps receiver data; Lane 1 |
| **61** | RX1n | | | 25 Gbps receiver data bar; Lane 1 |
| **62** | GND | | | |
| **63** | N.C. | | | |
| **64** | N.C. | | | |
| **65** | GND | | | |
| **66** | N.C. | | | |
| **67** | N.C. | | | |
| **68** | GND | | | |
| **69** | RX2p | | | 25 Gbps receiver data; Lane 2 |
| **70** | RX2n | | | 25 Gbps receiver data bar; Lane 2 |
| **71** | GND | | | |
| **72** | RX3p | | | 25 Gbps receiver data; Lane 3 |

| | | | | |
|---|---|---|---|---|
| **73** | RX3n | | | 25 Gbps receiver data bar; Lane 3 |
| **74** | GND | | | |
| **75** | N.C. | | | |
| **76** | N.C. | | | |
| **77** | GND | | | |
| **78** | (REFCLKp) | | CML | Module reference clock. No connect. |
| **79** | (REFCLKn) | | CML | Module reference clock. No connect. |
| **80** | GND | | | |
| **81** | N.C. | | | |
| **82** | N.C. | | | |
| **83** | GND | | | |
| **84** | TX0p | | | 25 Gbps transmitter data; Lane 0 |
| **85** | TX0n | | | 25 Gbps transmitter data bar; Lane 0 |
| **86** | GND | | | |
| **87** | TX1p | | | 25 Gbps transmitter data; Lane 1 |
| **88** | TX1n | | | 25 Gbps transmitter data bar; Lane 1 |
| **89** | GND | | | |
| **90** | N.C. | | | |
| **91** | N.C. | | | |
| **92** | GND | | | |
| **93** | N.C. | | | |
| **94** | N.C. | | | |
| **95** | GND | | | |
| **96** | TX2p | | | 25 Gbps transmitter data; Lane 2 |
| **97** | TX2n | | | 25 Gbps transmitter data bar; Lane 2 |
| **98** | GND | | | |
| **99** | TX3p | | | 25 Gbps transmitter data; Lane 3 |
| **100** | TX3n | | | 25 Gbps transmitter data bar; Lane 3 |
| **101** | GND | | | |
| **102** | N.C. | | | |
| **103** | N.C. | | | |
| **104** | GND | | | |

**Hardware Control Pins**

The CFP2 Module support real-time control functions via hardware pins, listed in the following.

| Pin | Symbol | Description | I/O | Logic | H | L | Pull-up/down |
|---|---|---|---|---|---|---|---|
| **17** | PRG_CNTL1 | Programmable Control 1 MSA Default: TRXIC_RS Tn, TX&RX ICs reset, "0": reset;"1" | I | 3.3V LVCMOS | per CFP MSA Management Interface Specification | | Pull-Up Note1 |
| **18** | PRG_CNTL2 | Programmable Control 2 MSA Default: Hardware Interlock LSB | I | 3.3V LVCMOS | | | Pull-Up Note1 |
| **19** | PRG_CNTL3 | Programmable Control 3 MSA Default: Hardware Interlock MSB | I | 3.3V LVCMOS | | | Pull-Up Note1 |
| **26** | MOD_LOPW R | Module Low Power Mode | I | 3.3V LVCMOS Low Power Enable Pull-Up | Low Power | Enable | Pull-Up Note1 |
| **28** | MOD_RSTn | Module Reset (Invert) | I | 3.3V LVCMOS | Enable | Reset | Pull-Down Note2 |

**Notes:**

1. Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP2 module
2. Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP2 module

**Hardware Alarm Pins**

The CFP2 Module supports alarm hardware pins listed in the following

| Pin | Symbol | Description | I/O | Logic | H | L | Pull-up/down |
|---|---|---|---|---|---|---|---|
| **20** | PRG_ALR M1 | Programmable Alarm 1 MSA Default: HIPWR_ON | O | 3.3V LVCMOS | Active High per MDIO document | | |
| **21** | PRG_ALR M2 | Programmable Alarm 2 MSA default: MOD_READY, Ready State has been reached | O | 3.3V LVCMOS | | | |
| **22** | PRG_ALR M3 | Programmable Alarm 3 MSA Default: MOD_FAULT | O | 3.3V LVCMOS | | | |
| **27** | MOD_ABS | Module Absent | O | 3.3V LVCMOS | Absent | Present | Pull-Down Note1 |
| **25** | RX_LOS | Receiver Loss of Signa | O | 3.3V LVCMOS | Loss of Signal | OK | |

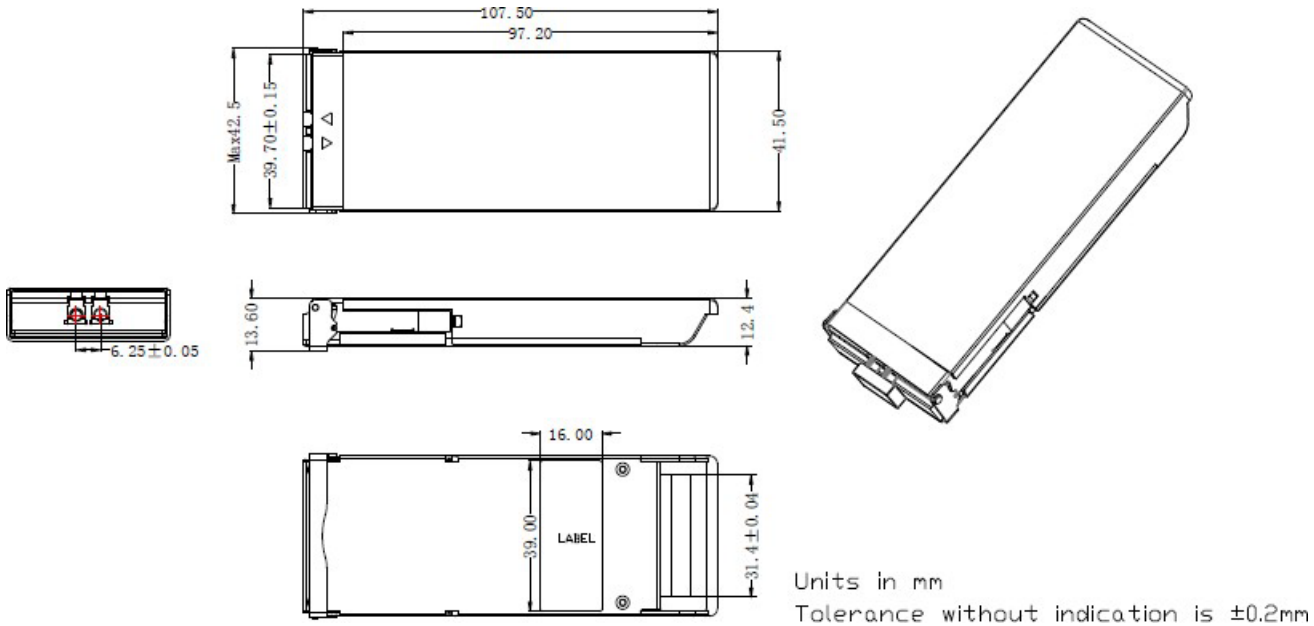
**Note:**

1. Pull-Down resistor (<100Ohm) is located within the CFP2 module. Pull-up should be located on the host

**CFP2 Lane Assignment**

| Lane | Center Frequency | Center Wavelength | Wavelength Range |
|---|---|---|---|
| **L0** | 231.4 THz | 1295.56 nm | 1294.53 to 1296.59 nm |
| **L1** | 230.6 THz | 1300.05 nm | 1299.02 to 1301.09 nm |
| **L2** | 229.8 THz | 1304.58 nm | 1303.54 to 1305.63 nm |
| **L3** | 229.0 THz | 1309.14 nm | 1308.09 to 1310.19 nm |

**Mechanical Specifications**



**About ProLabs**

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

**Complete Portfolio of Network Solutions**

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

**Trusted Partner**

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.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