Evaluation Board User Guide
UG-292

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD6641 DPD Observation Receiver

FEATURES

Full featured evaluation board for the AD6641
SPI interface for setup and control
External, on-board oscillator or AD9517 clocking options
Balun/transformer or amplifier input drive options
LDO regulator or switching power supply options
VisualAnalog and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A),
CUI EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000,
Windows ME, or Windows XP
USB 2.0 port, recommended (USB 1.1 compatible)
AD6641 board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

AD6641 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application, *Understanding ADC Testing and Evaluation*

GENERAL DESCRIPTION

This document describes the AD6641 evaluation board, which provides all of the support circuitry required to operate this part in its various modes and configurations. The application software used to interface with the devices is also described.

The AD6641 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP

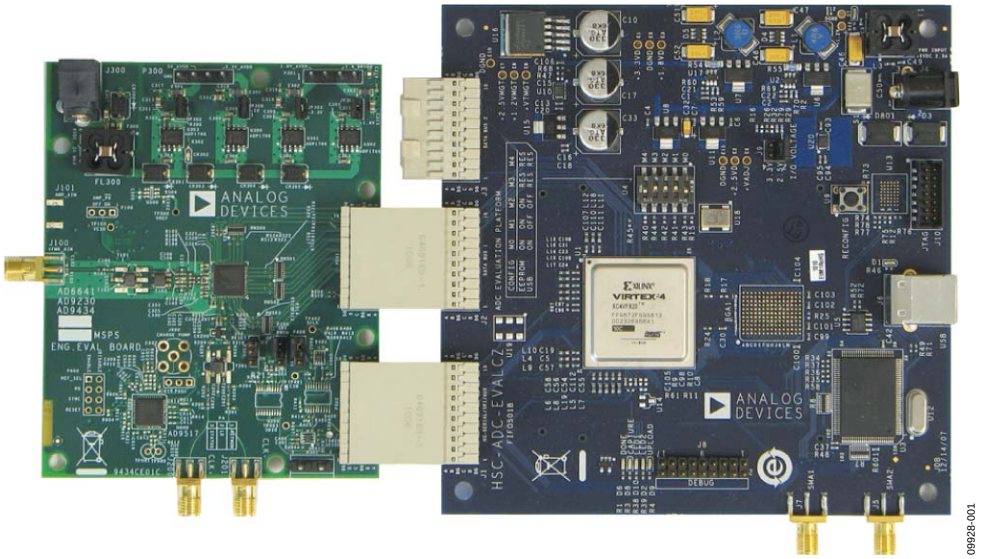

Figure 1. AD6641 Family Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

TABLE OF CONTENTS

REVISION HISTORY

7/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The evaluation board provides all of the support circuitry required to operate the AD6641 in its various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 21 to Figure 31 for the complete schematics and layout diagrams. These diagrams illustrate the routing and grounding techniques that should be applied at the system level when designing application boards using the AD6641 receiver.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V to 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at J300. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, JP301 through JP303 can be removed to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P300 and P301 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply should have a 1 A current capability.

An additional 5V_AVDD supply is used to bias the optional input path amplifier. If used, this supply should have a 1 A current capability.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA or HP 8644B signal generators or an equivalent. Use a 1 meter shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude in the signal generators (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multipole, narrow-band band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE, Allen Avionics, and K&L band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The LVDS output signals are routed to the FPGA on the data capture board.

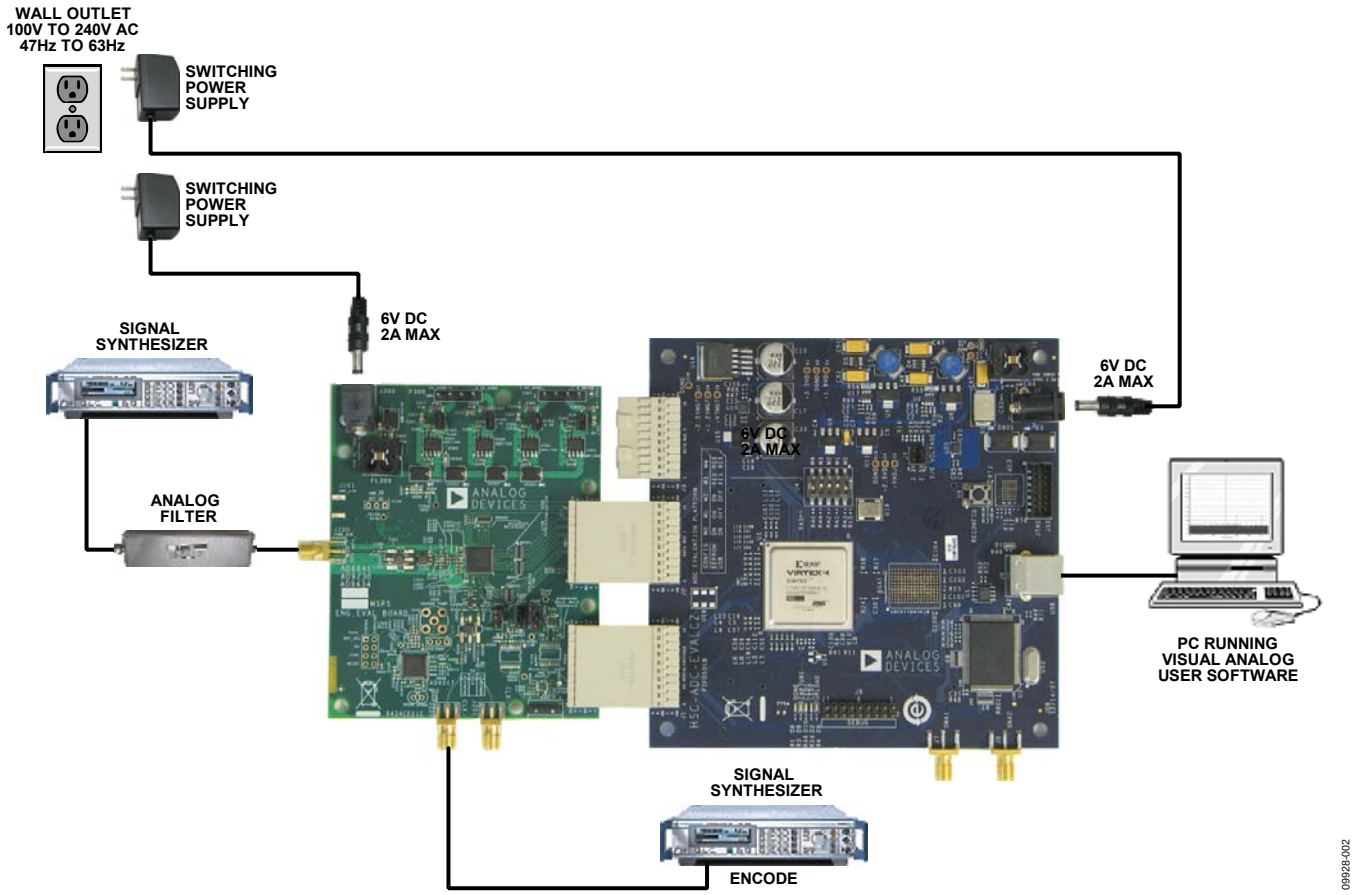

Figure 2. Evaluation Board Connection

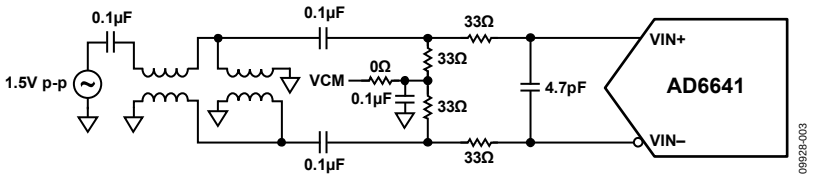

Figure 3. Default Analog Input Configuration of the AD6641

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD6641 evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V to 240 V ac wall outlet (at 47 Hz to 63 Hz) and J300.

Analog Input

The input on the evaluation board is set up for a double balun-coupled analog input with a 50 Ω impedance (see Figure 3). The analog input to the AD6641 is a differential buffer. For best dynamic performance, source impedances driving VIN+ and VIN− are matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

The analog inputs are self-biased by an on-chip reference to provide a common-mode voltage level of nominally 1.7 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.5 V p-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of an SPI control.

VREF

The AD6641 VREF pin (Pin 31) allows the user to monitor the on-board voltage reference or provide an external reference (requires configuration through the SPI). The three optional

settings are internal V_{REF} (the pin is connected to 20 kΩ to ground), export V_{REF}, and import V_{REF}. See the settings for Register 0x18 in Table 1.

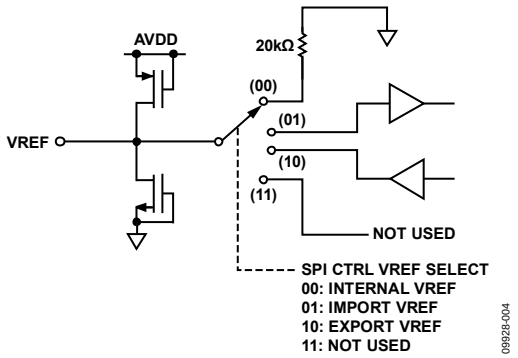

Figure 4. Equivalent VREF Input/Output Circuit

Clock Circuitry for the AD9434/AD9484

The default clock input circuit on the evaluation board uses a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T201) that adds a low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR200 before entering the ADC clock inputs.

The evaluation board is by default set up to be clocked with the transformer-coupled input network connected to the external clock source through the SMA connector, J200 (labeled CLK+).

PDWN

To enable the power-down feature, see the description of the serial port interface Register 0x08 in the AD6641 data sheet.

Table 1. Register 0x18 Settings

Address (Hexadecimal)	Parameter Name	Bits[7:6]	Bit 5	Bits[4:0]
0x18	Input range	VREF select[1] 00 = internal V_{REF} (20 kΩ pull-down internally) 01 = import V_{REF} (apply 0.59 V to 0.8 V to Pin 31) 10 = export V_{REF} (monitor) 11 = not used	0	Input voltage range setting (V) 11100 = 1.60 11101 = 1.58 11110 = 1.55 11111 = 1.52 00000 = 1.50 00001 = 1.47 00010 = 1.44 00011 = 1.42 00100 = 1.39 00101 = 1.36 00110 = 1.34 00111 = 1.31 01000 = 1.28 01001 = 1.26 01010 = 1.23 01011= 1.20 01100 = 1.18

[1] V_{REF} x 2 = input range.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9434 and AD6641 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the AD6641 evaluation board to the HSC-ADC-EVALCZ boards as shown in Figure 1.
2. Connect one 6 V, 2 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD6641 board.
3. Connect one 5 V, 3 A (6 V, 2 A can optionally be used) switching power supply (such as the CUI KSAFD0500300W1US supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable. (Connect to J6.)
5. On the ADC evaluation board, make sure that jumpers are on the J300 to J303 headers to connect the power supplies. Connect Pin 1 to Pin 2 of P200 and Pin 2 to Pin 3 of P400 to connect the SPI bus to the ADC.
6. On the ADC evaluation board, provide a clean, low jitter clock source to connector J200 at the desired ADC conversion rate.
7. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal at the J100 connector. Use a 1 meter, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog® on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog-New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 5 where the AD6641 is shown as an example).

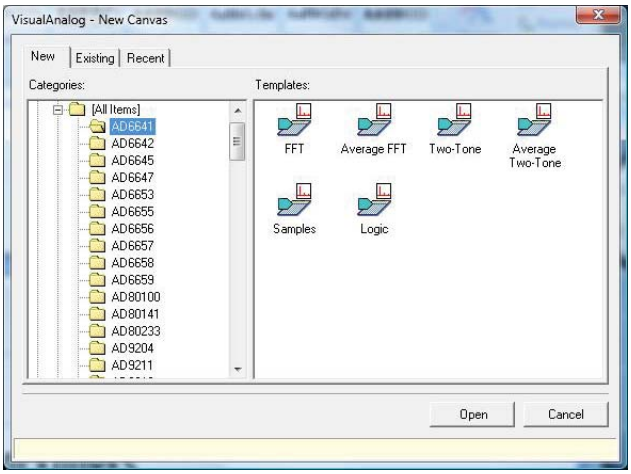

Figure 5. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 6). Click **Yes**, and the window closes.

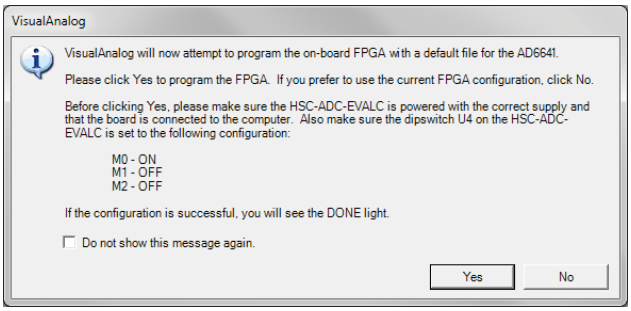

Figure 6. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the VisualAnalog window, to see what is shown in Figure 7.

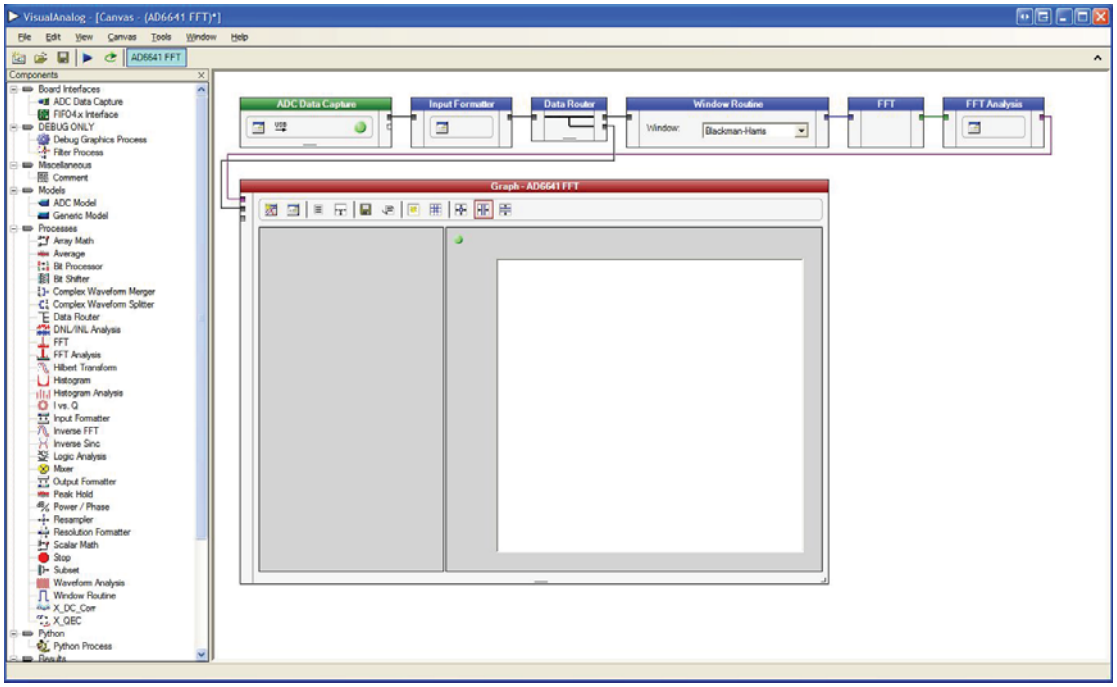

Figure 7. VisualAnalog, Main Window

To set up for SPORT mode, do the following:

1. Click the **Settings** button of the **ADC Data Capture** block in the VisualAnalog main window (see Figure 7).
2. In the **ADC Data Capture Settings** box, click the **Capture Board** tab (see Figure 8). The **ad6641_fifo.bin** program file should be displayed in the **Program File** box. If it is not, use the **Browse** button to locate the file.

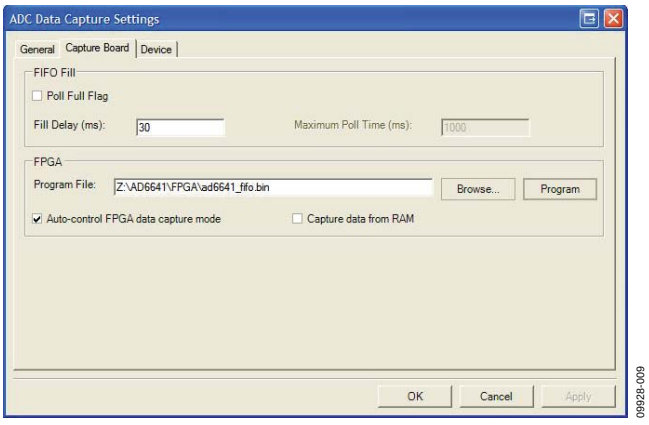

Figure 8. Capture Board Settings

3. Click the **Program** button. The DONE LED on the HSC-ADC-EVALCZ board should illuminate, indicating that the FPGA has been programmed correctly.
4. In the **Output Data** panel of the **General** tab of the **ADC Data Capture Settings** box, set **Length** to **16384** (see Figure 9).

Figure 9. General Settings Tab

5. On the **Device** tab of the **ADC Data Capture Settings** box, set **Output Mode** to **SDR** and, in the **Output Por**t box select **SPORT** (see Figure 10).

   Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*.

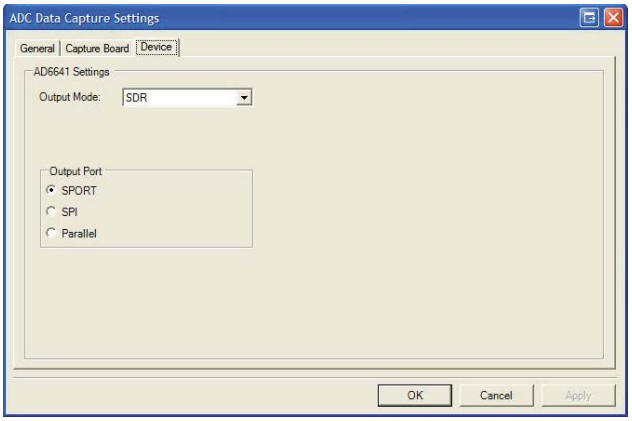

Figure 10. Device Settings Tab

6. After the changes are made to the capture settings, click **Collapse Display** (see Figure 11).

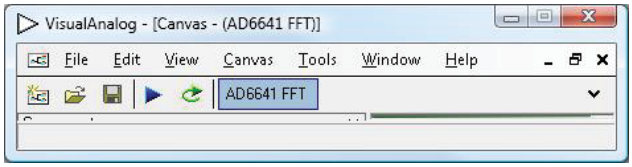

Figure 11. VisualAnalog Window Toolbar, Collapsed Display

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI controller software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 12).

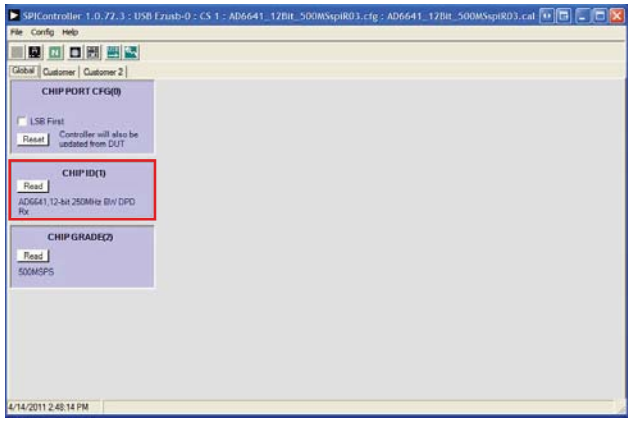

Figure 12. SPI Controller, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 13).

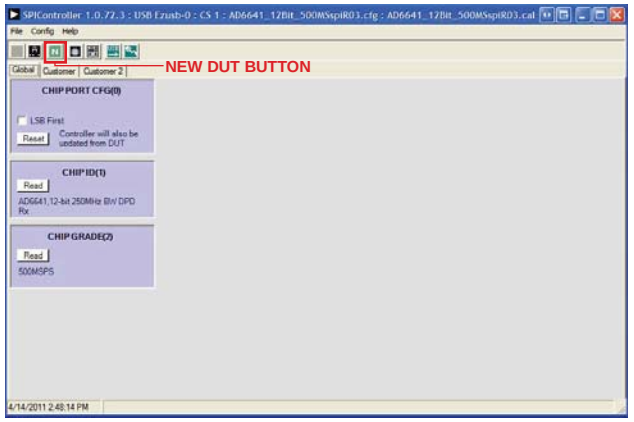

Figure 13. SPI Controller, New DUT Button

3. In the **Customer 2** tab of the **SPIController** window (see Figure 14, set the following options:
   Fill Count = 255
   Dump Operation = Master
   Readback Mode = SPORT

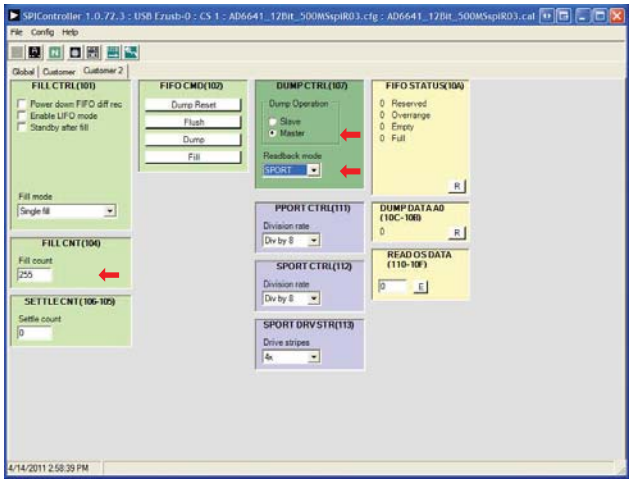

Figure 14. SPI Controller, Customer Tab

Note that other settings can be changed in the **Customer** tab (see the AN-878 Application Note, *High Speed ADC SPI Control Software*, and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information).

7. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 15).

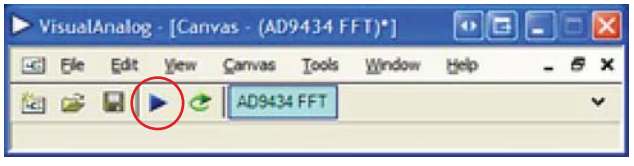

Figure 15. Run Button (Encircled in Red) in the VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. Examine the **Fund Power** reading in the left panel of the **VisualAnalog Graph – AD6641 Average FFT** window (see Figure 16).

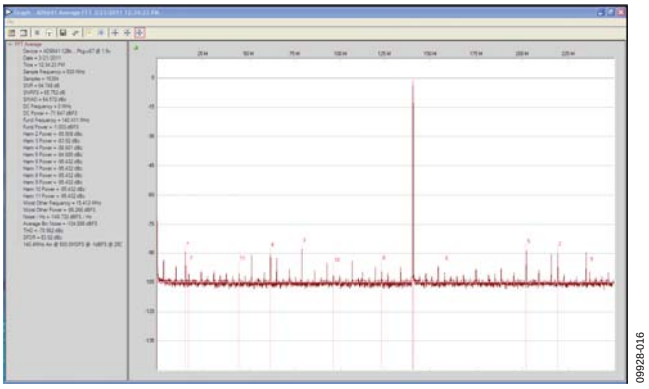

Figure 16. Graph Window of VisualAnalog

2. Click the disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 17 for an example.

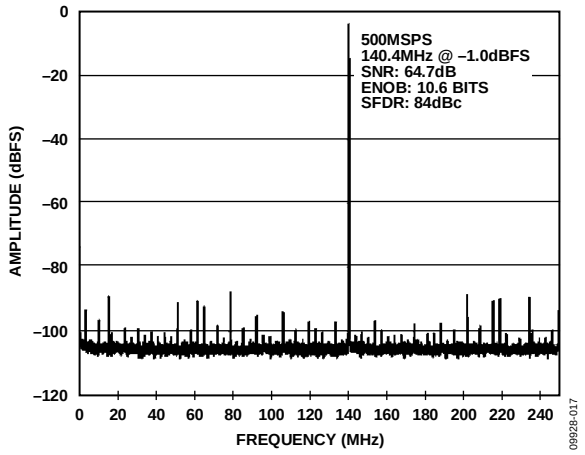

Figure 17. Typical FFT, AD9434

Additional Output Mode Options

To run the part in parallel mode, change the settings as follows.

In the SPI controller,

1. In the **Customer 2** tab, set **Readback Mode** to **Parallel**.
2. In the **Customer** tab, **Output Modes** panel, set **Data Format** to **CMOS**.

In VisualAnalog,

1. In the **Capture Board** tab, select **ad6641_pfifo.bin** and click the **Program** button.
2. In the **Device** tab, set **Output Port** to **Parallel**.

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In VisualAnalog, click the **Settings** button in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, do the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** is clicked, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure the FPGA has been programmed by verifying that the DONE LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure the correct FPGA program was installed by selecting the **Settings** button in the **ADC Data Capture** block in VisualAnalog. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If VisualAnalog indicates that the FIFO capture timed out,

- Make sure all power and USB connections are secure.
- Confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

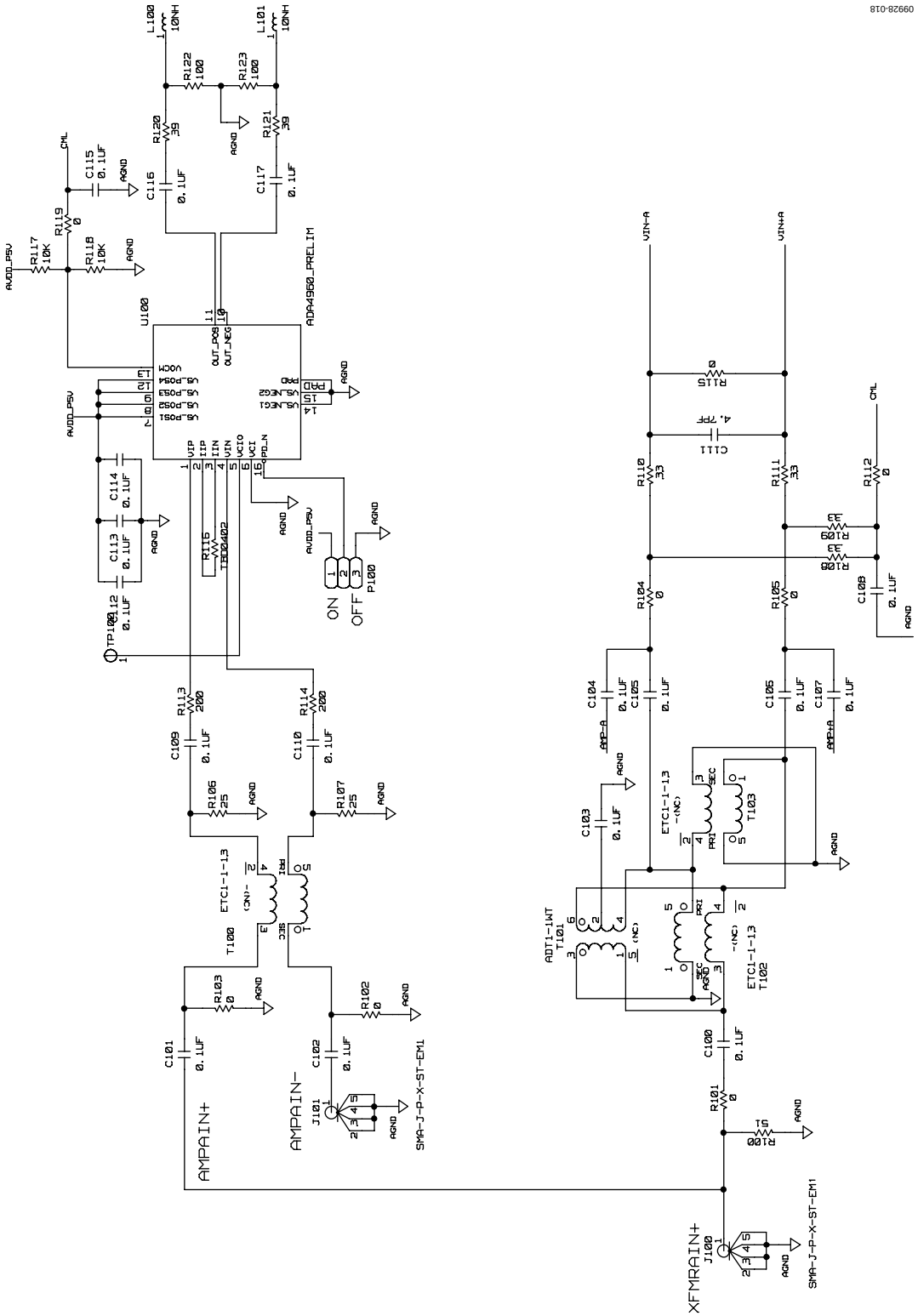

Figure 18. Analog Input Circuits

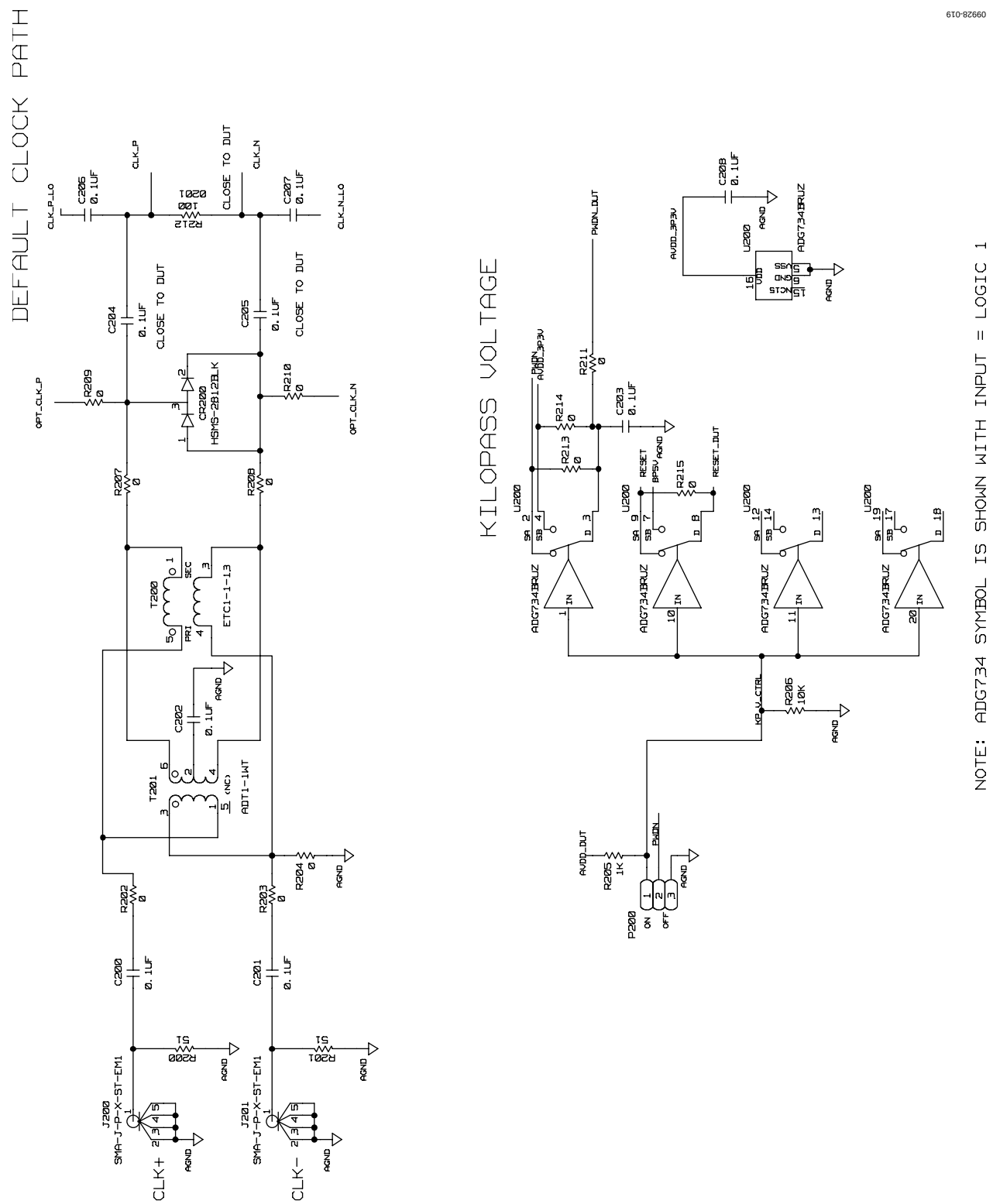

Figure 19. Clock Input Circuits

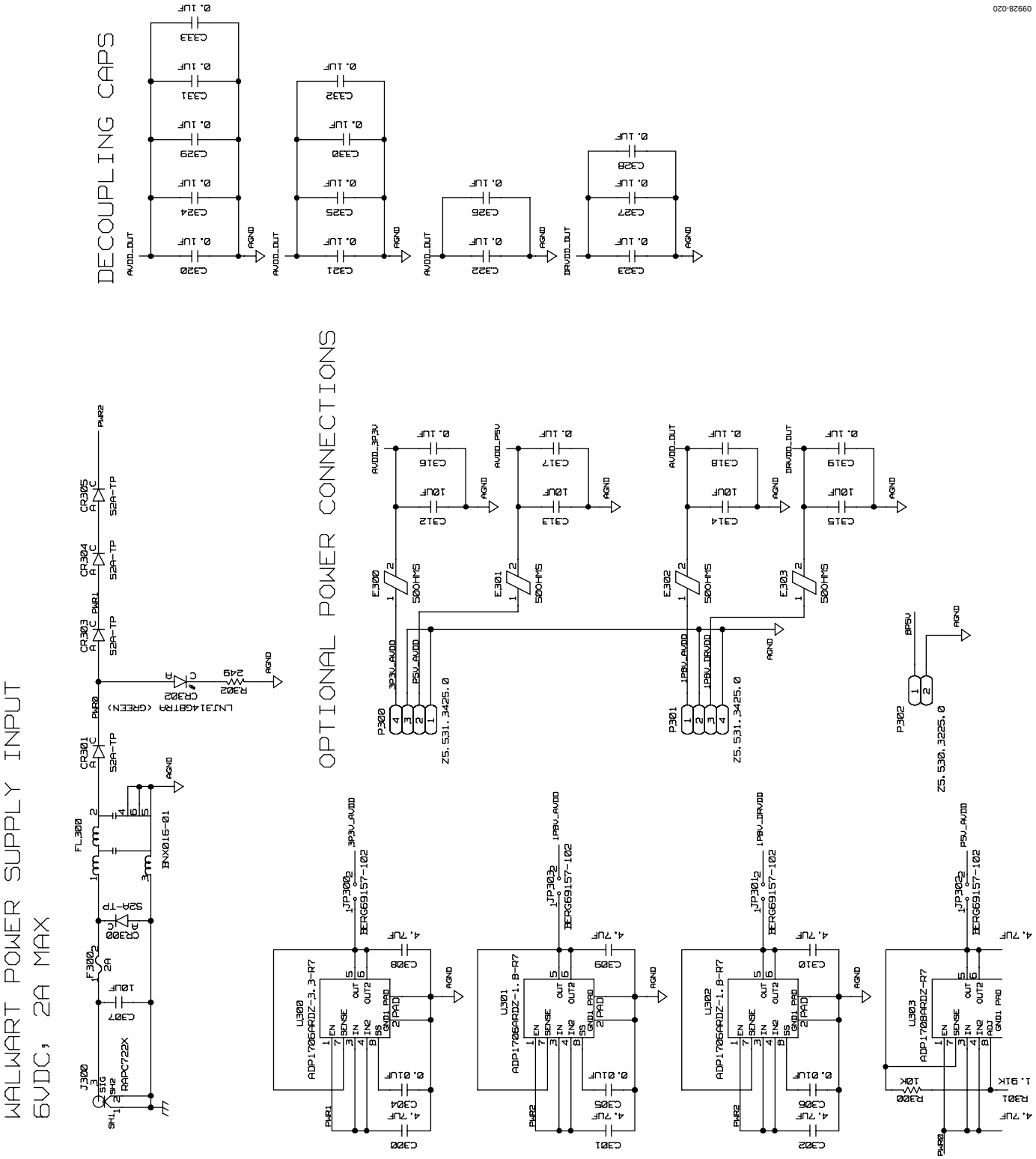

Figure 20. Board Power Supply Circuits

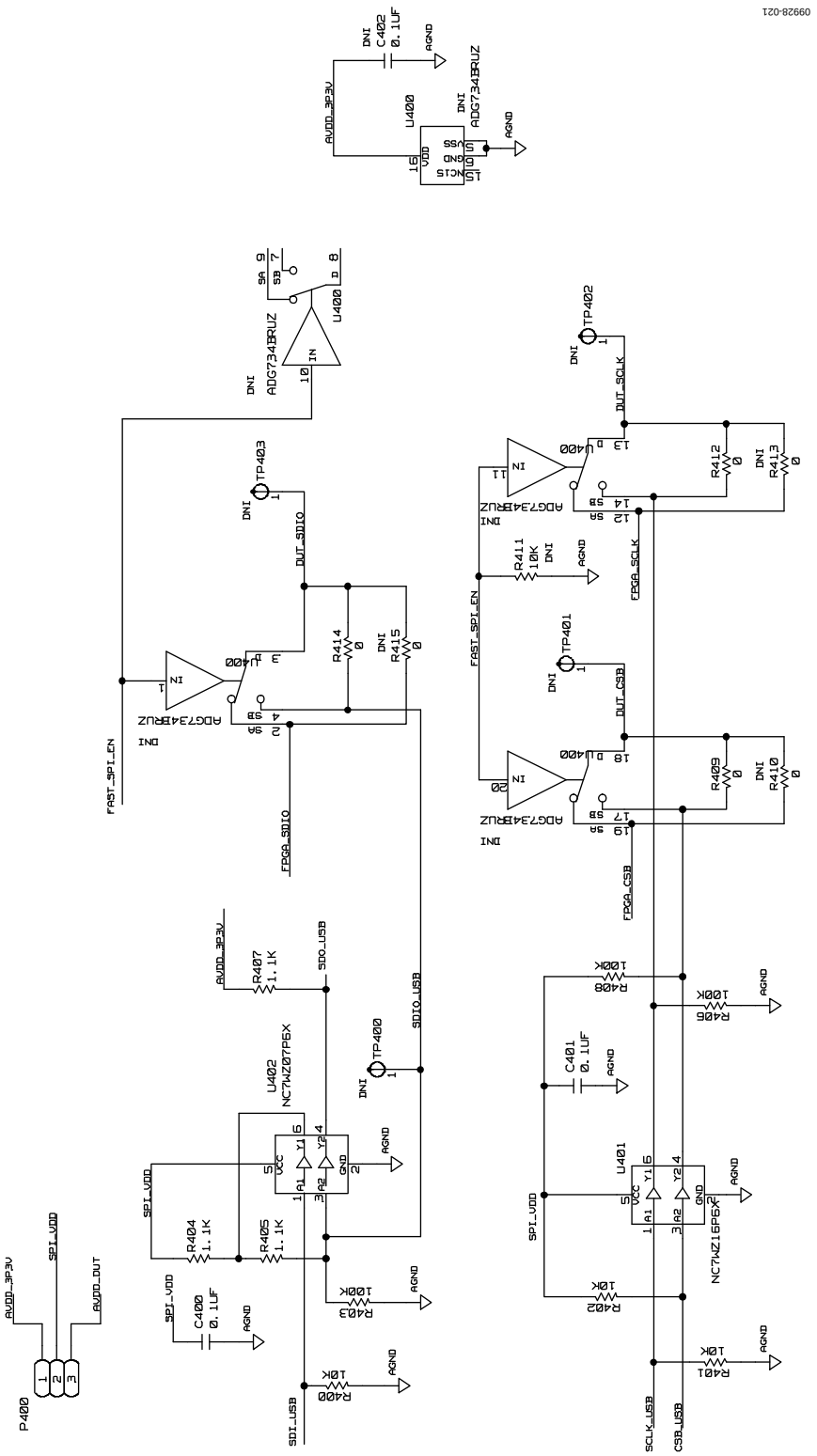

Figure 21. SPI Interface Circuits

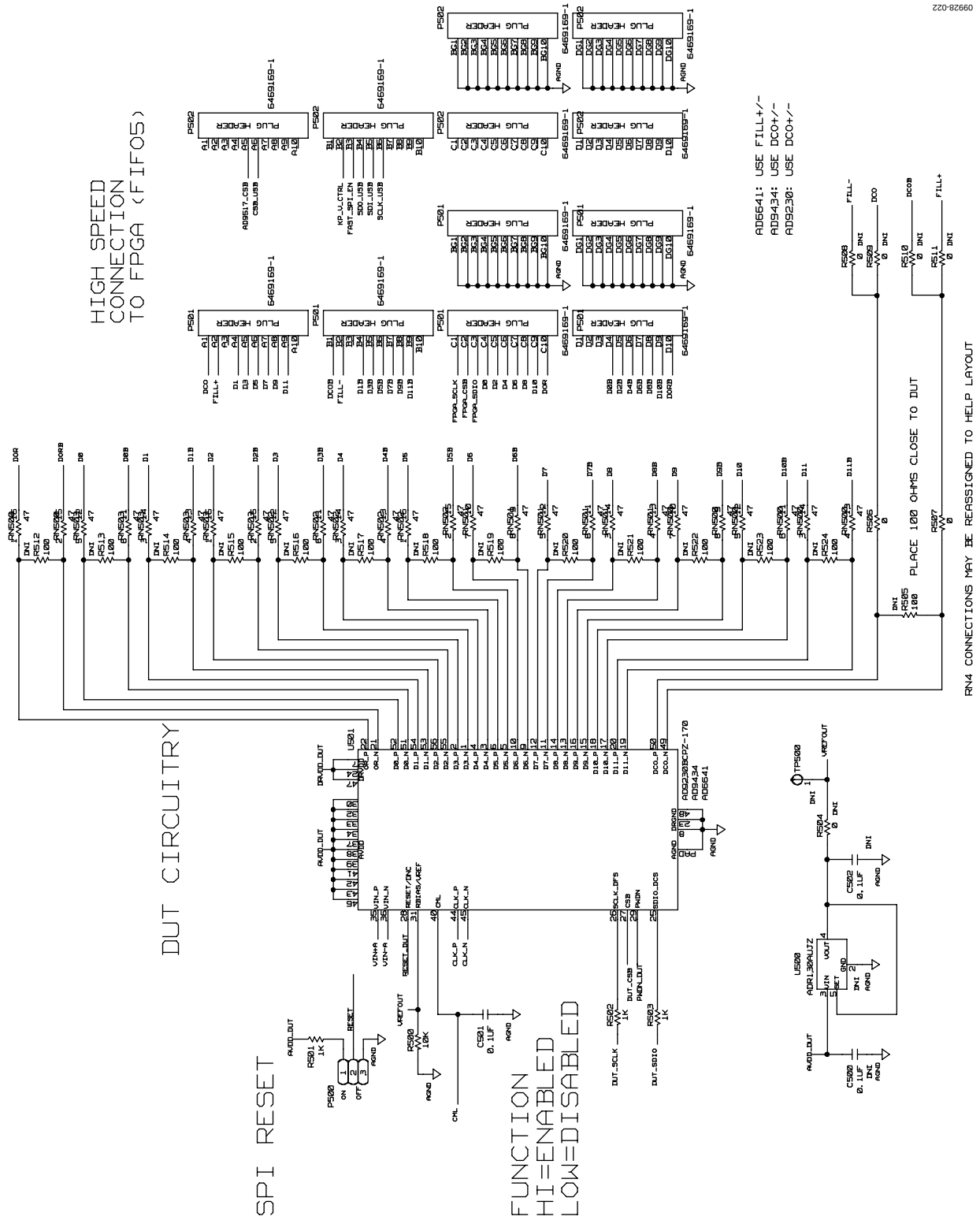

Figure 22. DUT Interface Circuits

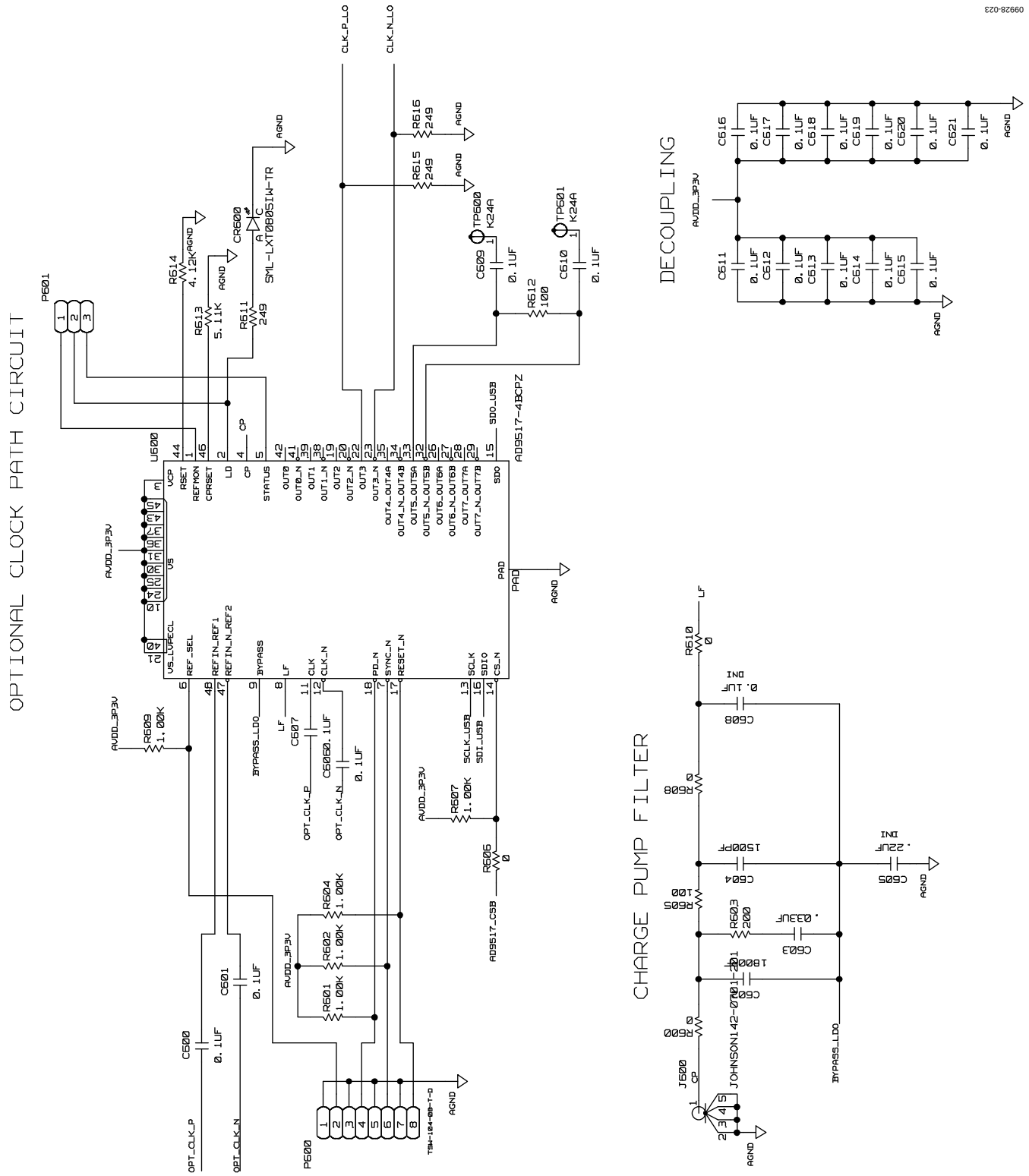

Figure 23. Optional AD9517 Clock Input Circuit

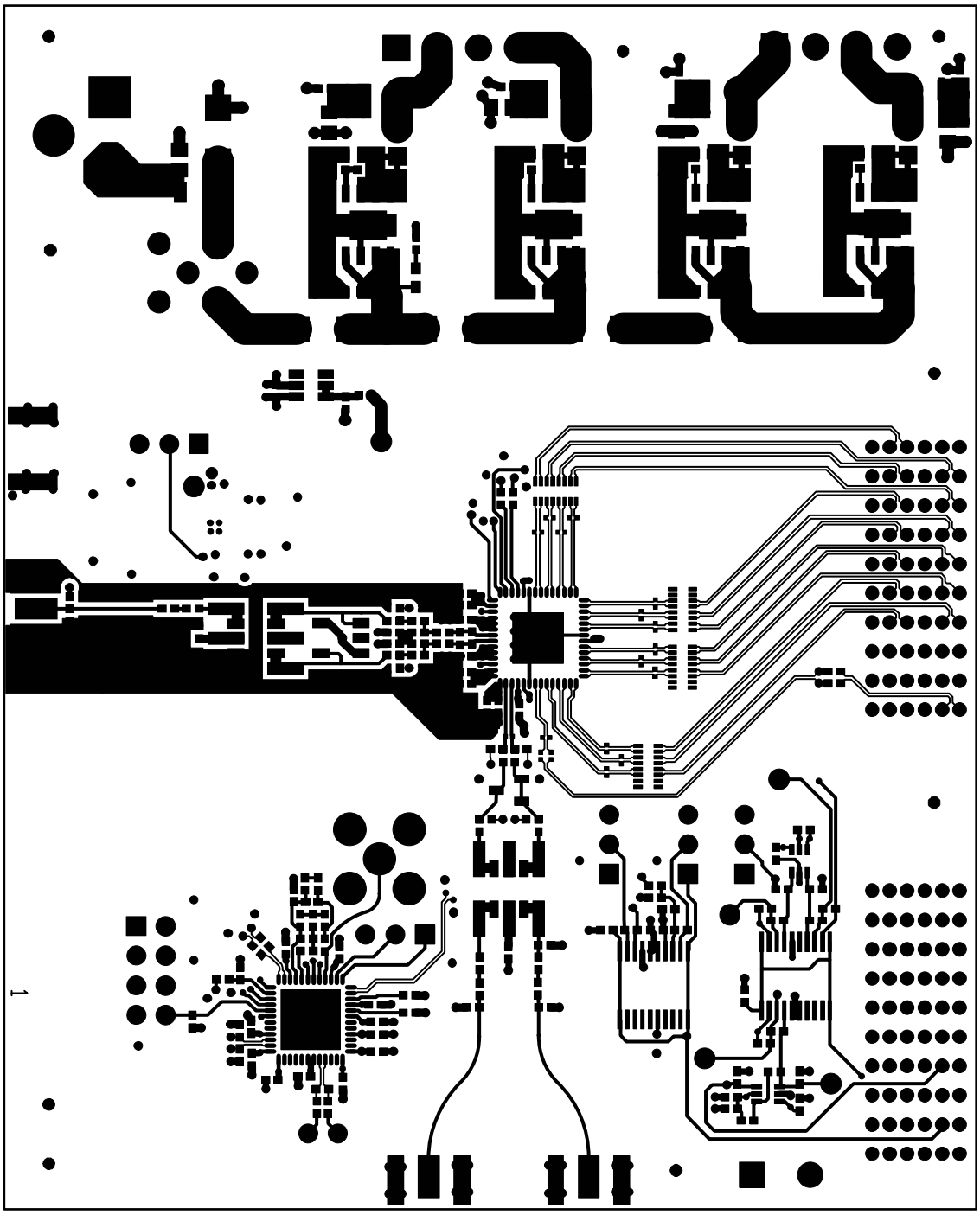

Figure 24. Top Side

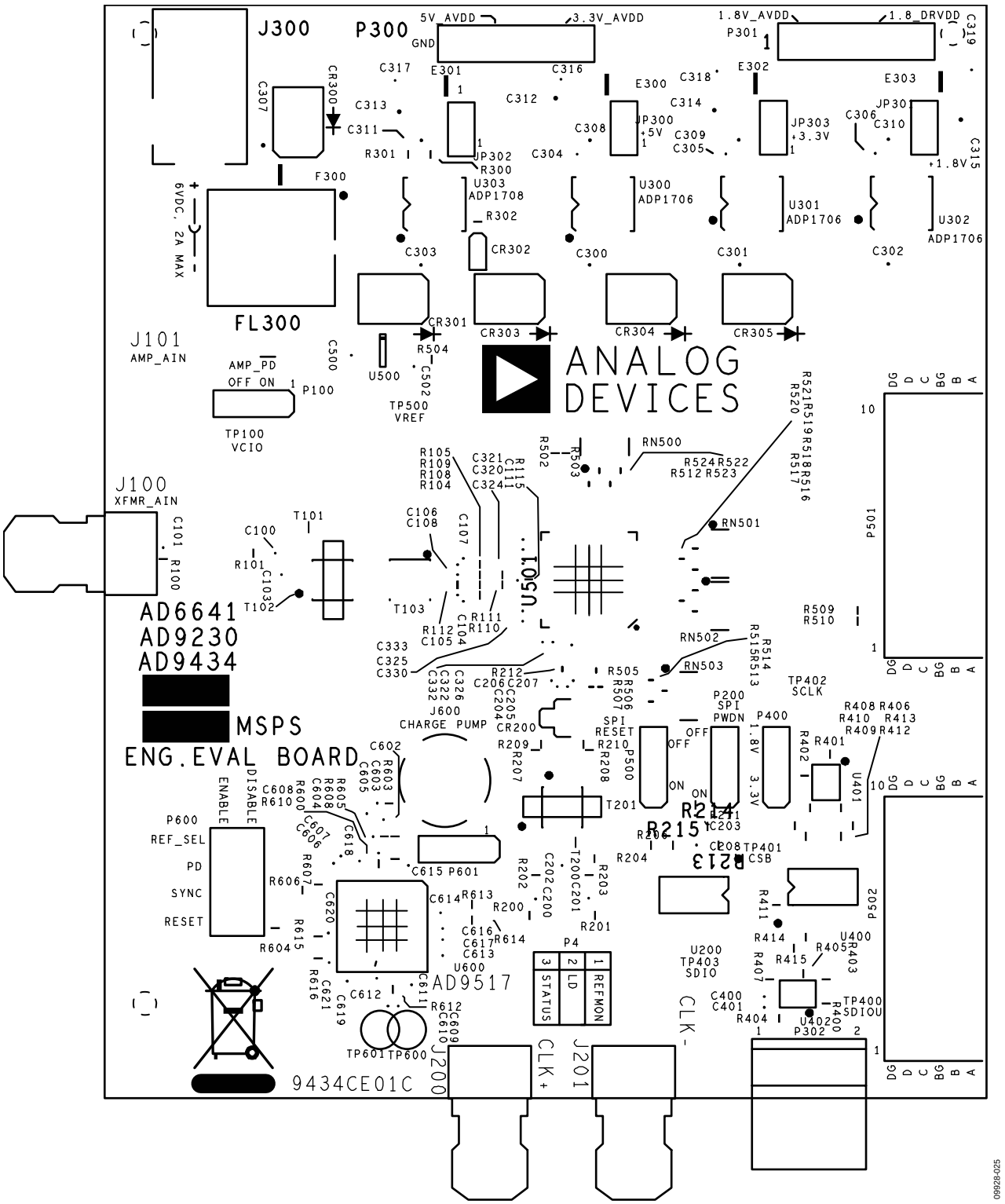

Figure 25. Top Silk Screen

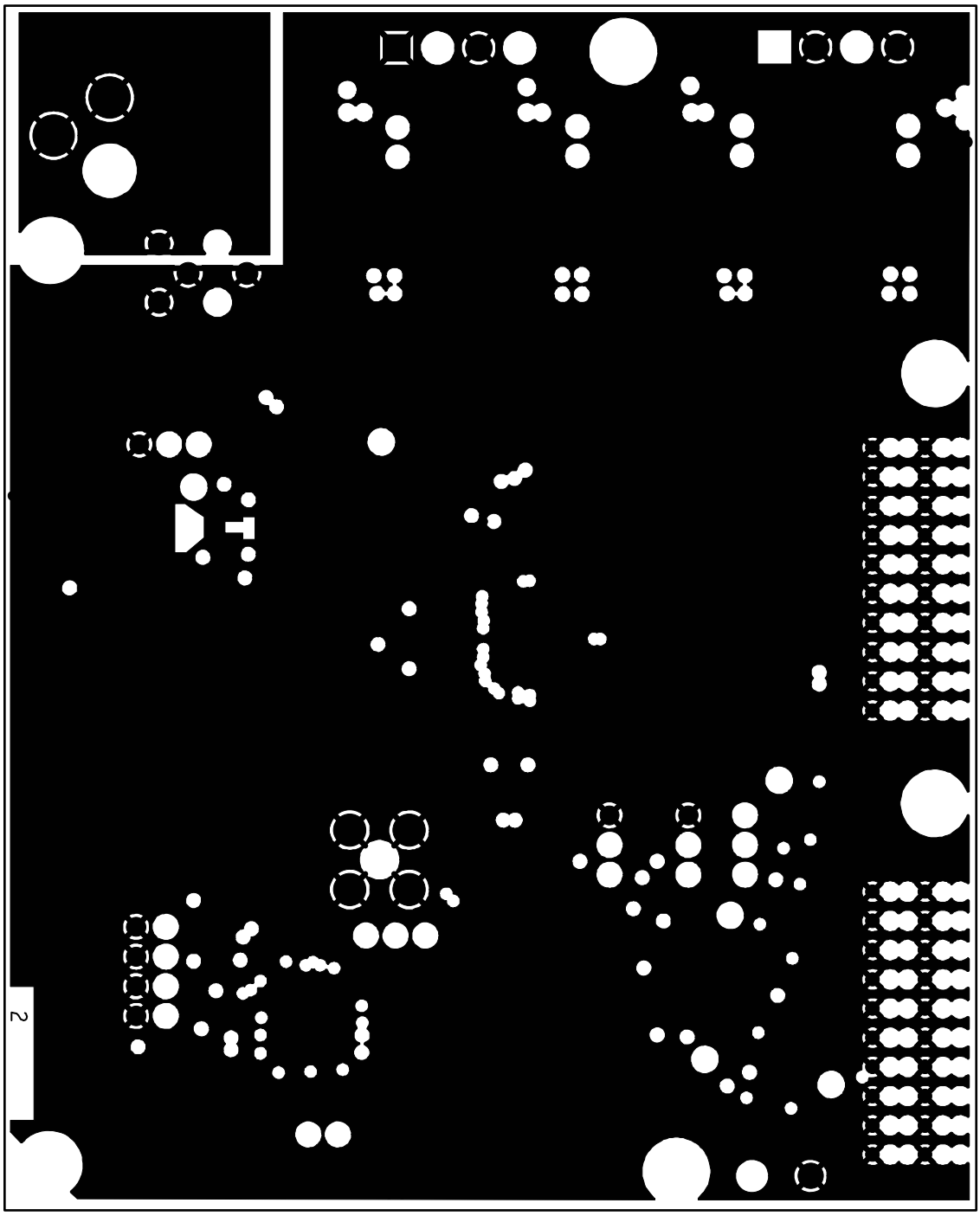

Figure 26. Ground Plane (Layer 2)

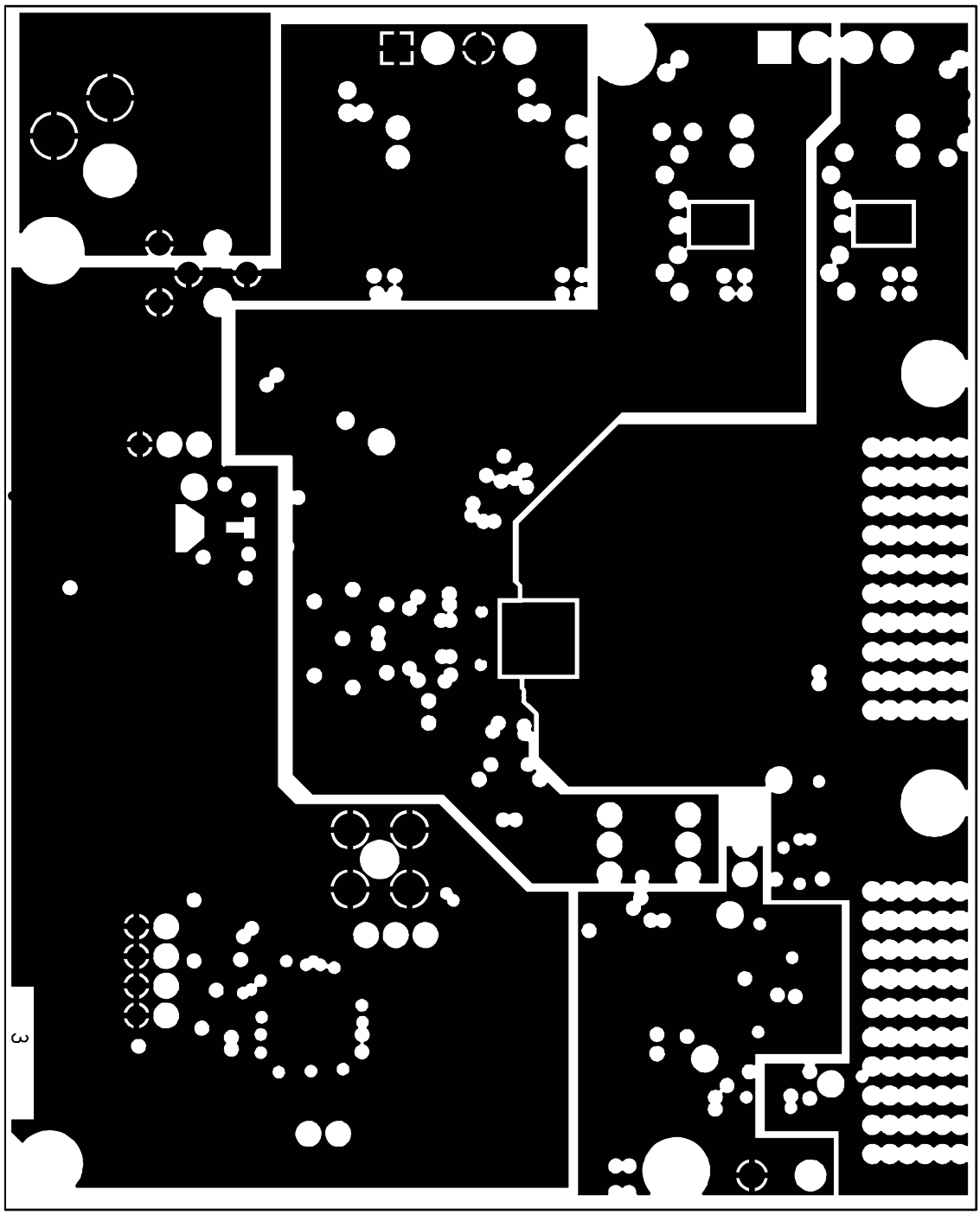

Figure 27. Power Plane (Layer 3)

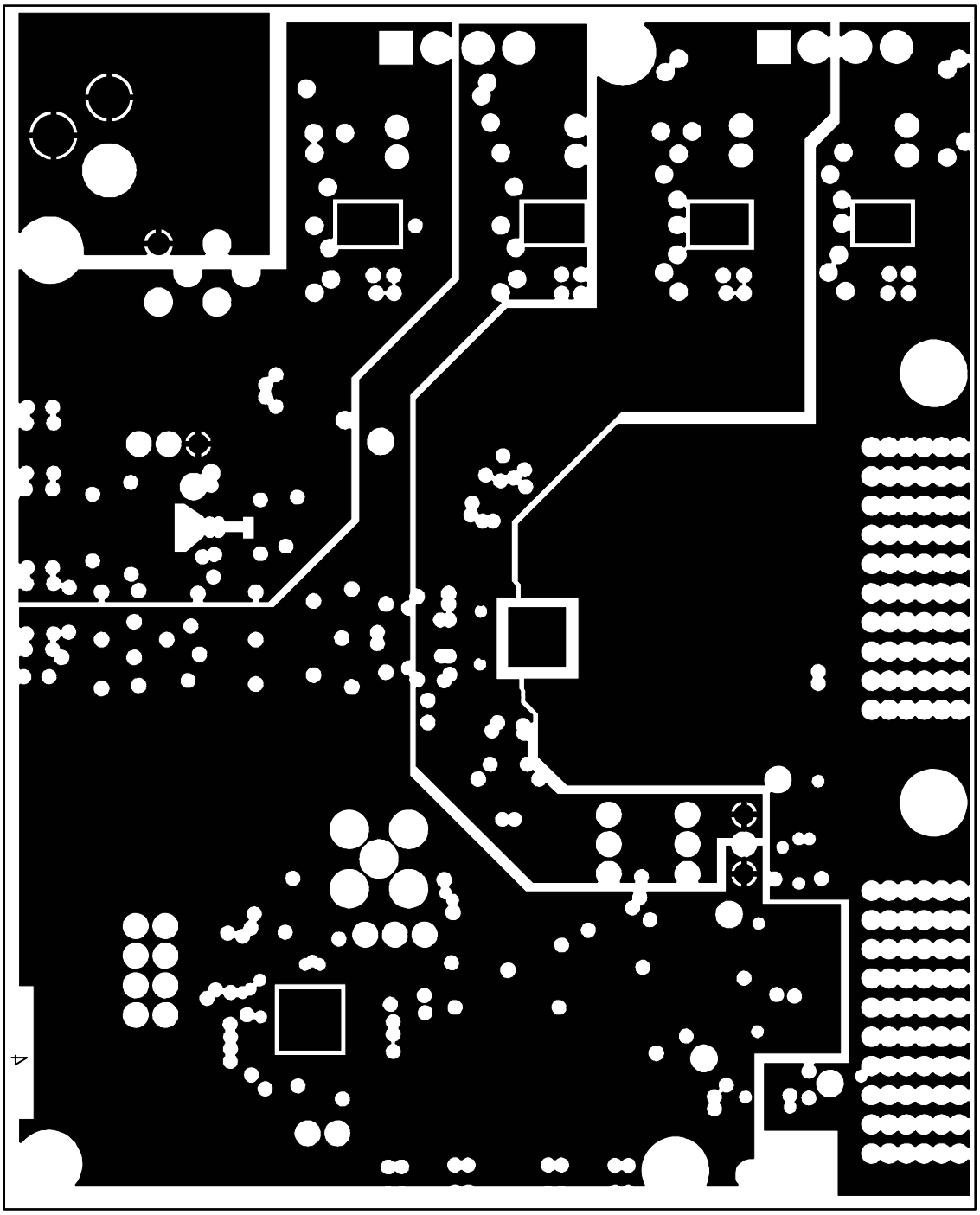

Figure 28. Power Plane (Layer 4)

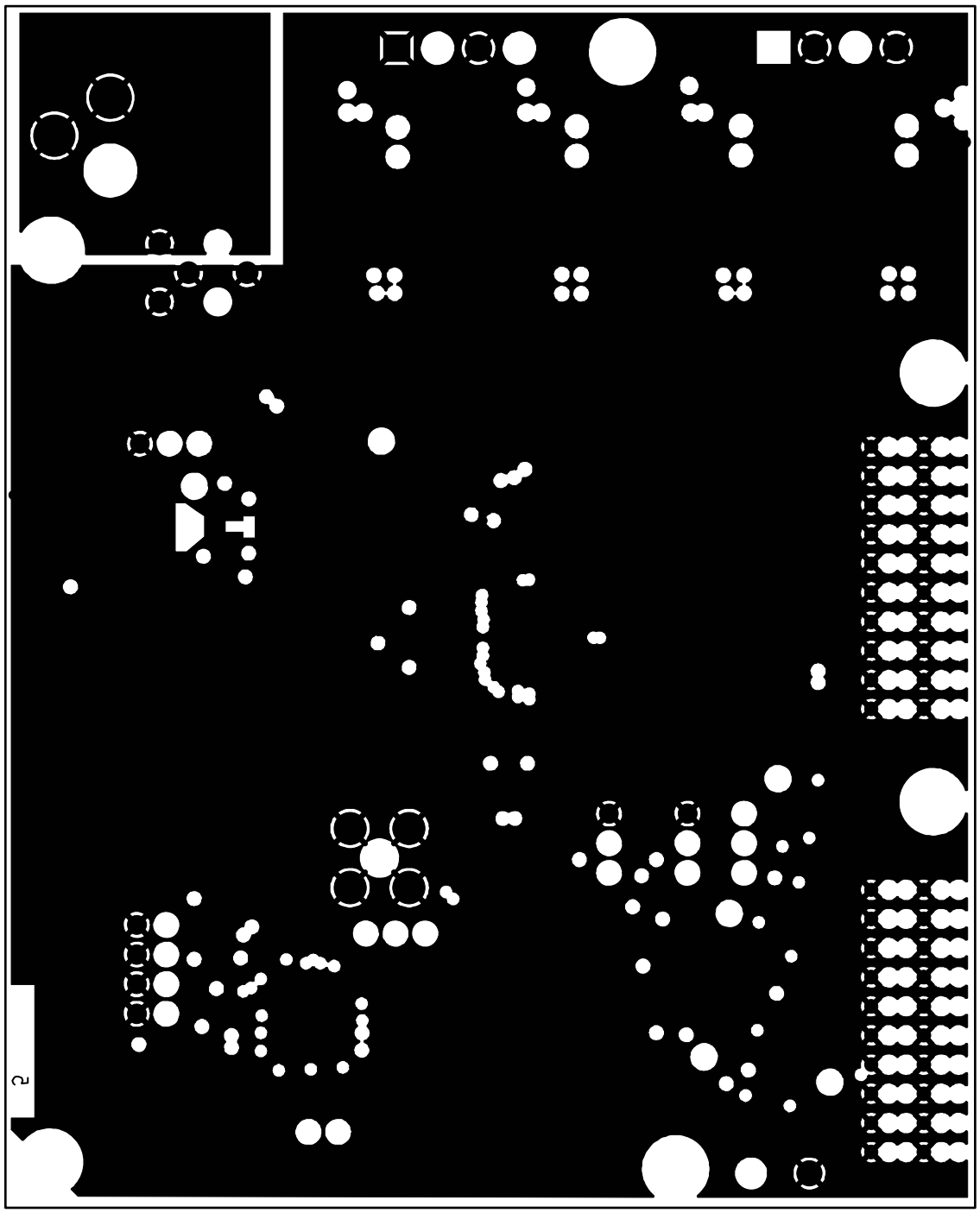

Figure 29. Ground Plane (Layer 5)

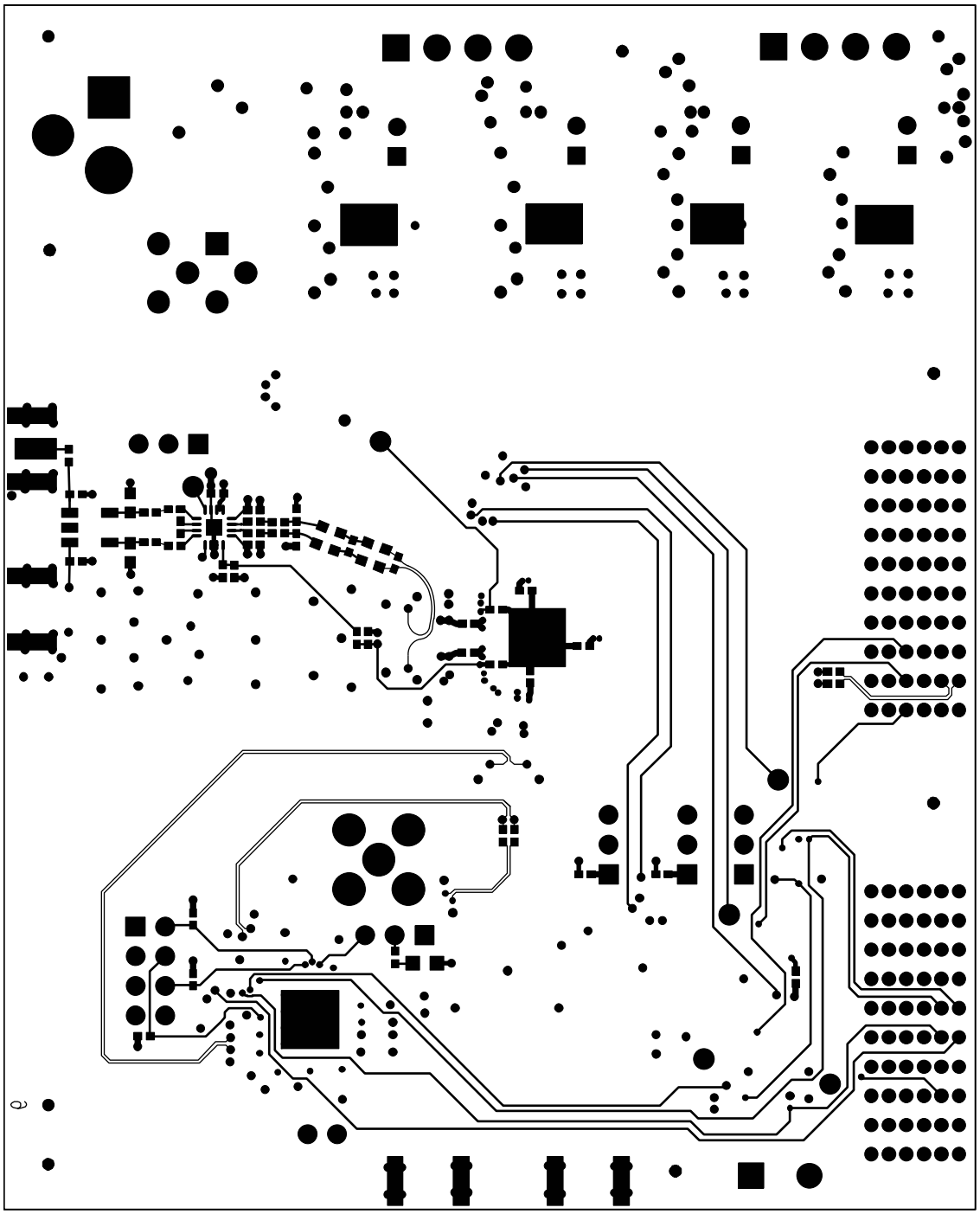

Figure 30. Bottom Side

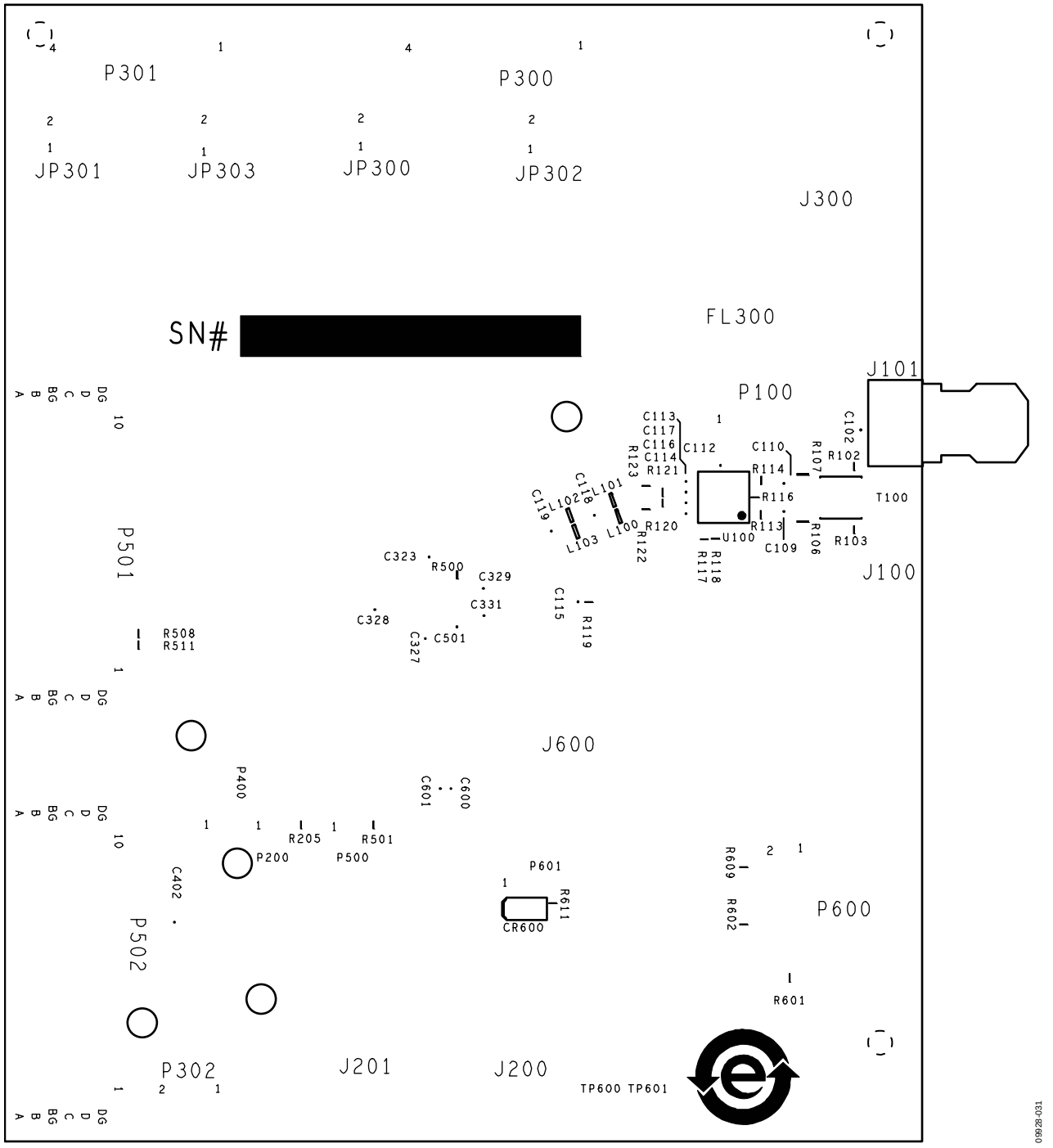

Figure 31. Bottom Silk Screen

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. AD6641 BOM

Qty	Reference Designator	Description	Value	Mfg	Mfg_PN
1	N/A	PCB BOARD, 9434CE01C	0	0	0
32	C100, C103, C105, C106, C108, C115, C200, C201, C202, C204, C205, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C400, C401, C501	CAP CER X7R 0402	0.1 µF	Murata	GRM155R71C104KA88D
1	C111	CAP High Q microwave chip NP0 0402	4.7 pF	Panasonic	ECD-G0E4R7C
8	C300, C301, C302, C303, C308, C309, C310, C311	CAP CER chip	4.7 µF	Panasonic	ECJ-1VB0J475M
3	C304, C305, C306	CAP CER chip X8R	0.01 µF	TDK	C1005X8R1E103K
5	C307, C312, C313, C314, C315	CAP CER monolithic	10 µF	Murata	GRM21BR61C106KE15L
1	C605	CAP CER chip	0.22 µF	Panasonic	ECJ-0EB0J224K
1	CR200	Diode SHTKY dual series	HSMS-2812BLK	Avago	HSMS-2812BLK
5	CR300, CR301, CR303, R304, CR305	Diode recovery rectifier	S2A-TP	Micro Commercial Components Corp	S2A-TP
1	CR302	LED green surface mount	LNJ314G8TRA (green)	Panasonic	LNJ314G8TRA
4	E300, E301, E302, E303	Inductor ferrite beads	50 Ω	Murata	BLM31PG500SN1L
1	F300	Slim line lead-free 1206	2 A	Littelfuse	0466002.NR
1	FL300	FLTR noise suppression LC combined type	BNX016-01	Murata	BNX016-01
3	J100, J200, J201	CONN-PCB SMA ST edge mount	SMA-J-P-X-ST-EM1	Samtec	SMA-J-P-X-ST-EM1
1	J300	CONN-PCB powerjack MINI 0.08 IN. R/A T/H	RAPC722X	Switchcraft	RAPC722X
4	JP300, JP301, JP302, JP303	CONN-PCB Berg JMPR ST male 2P	BERG69157-102	Berf	69157-102
3	P200, P400, P500	CONN-PCB Berg HDR ST male 3P	SAMTECTSW10608GS3PIN	Samtec	TSW-103-08-G-S
2	P300, P301	CONN-PCB, pluggable header	Z5.531.3425.0	Wieland	Z5.531.3425.0
1	P302	CONN-PCB term strip header 2P	Z5.530.3225.0	Wieland	Z5.530.3225.0
2	P501, P502	CONN_PCB 60-pin RA connector	6469169-1	Tyco	6469169-1
18	R101, R104, R105, R119, R202, R203, R204, R205, R207, R208, R211, R213, R215, R409, R412, R414, R508, R511	RES film SMD 0402	0	Panasonic	ERJ-2GE0R00X
4	R108, R109, R110, R111	RES film SMD 0402	33	Panasonic	ERJ-2GEJ330X
2	R200, R201	RES film SMD 0402	51	Panasonic	ERJ-2GEJ510X
2	R212, R505	RES prec thick film chip R0201	100	Panasonic	ERJ-1GEF1000C
4	R300, R400, R401, R402	RES prec thick film chip R0402	10 K	Panasonic	ERJ-2RKF1002X
1	R301	RES prec thick film chip R0402	1.91 K	Panasonic	ERJ-2RKF1911X
1	R302	RES film SMD 0402	249	Venkel	CR0402-16W-2490FT
3	R403, R406, R408	RES prec thick film chip R0402	100 K	Panasonic	ERJ-2RKF1003X
3	R404, R405, R407	RES film SMD 0402	1.1 K	Panasonic	ERJ-2GEJ112X
3	R409, R412, R414	RES thick film chip	0	Multicomp	0402WGF0000TCE

Qty	Reference Designator	Description	Value	Mfg	Mfg_PN
2	R506, R507	RES chip SMD 0201	0	Panasonic	ERJ-1GE0R00C
3	R501, R502, R5023	RES ultrareliability MF chip	1 K	Susumu	RG1005P-102-B-T5
1	R603	RES prec thick film chip R0402	200	Panasonic	ERJ-2RKF2000X
4	RN500, RN501, RN502, RN503	RES NTWRK 16-pin/8 RES surface mount	47	Panasonic	EXB-2HV470JV
3	T102, T103, T200	XFMR RF 1:1	ETC1-1-13	Macom	ETC1-1-13
1	U300	IC-ADI low dropout CMOS LIN REG	ADP1706ARDZ-3.3-R7	Analog Devices	ADP1706ARDZ-3.3-R7
2	U301, U302	IC-ADI low dropout CMOS LIN REG	ADP1706ARDZ-1.8-R7	Analog Devices	ADP1706ARDZ-1.8-R7
1	U303	IC-ADI low dropout CMOS LIN REG	ADP1708ARDZ-R7	Analog Devices	ADP1708ARDZ-R7
1	U401	IC tiny logic UHS dual buffer	NC7WZ16P6X	Fairchild	NC7WZ16P6X
1	U402	IC tiny logic UHS dual buffer	NC7WZ07P6X	Fairchild	NC7WZ07P6X
1	U501	IC-ADI 12-bit 1.8 V ADC converter	0	Analog Devices	0
1	U600	IC-ADI 12-output CLK GEN with INT 1.6 GHZ VCO	AD9517-4BCPZ	Analog Devices	AD9517-4BCPZ
1	U100	IC-ADI low dist UHS DIFF ADC DRVR	ADA4960-1ACPZ	Analog Devices	AD4960-Prelim
39	C101, C102, C104, C107, C108, C109, C110, C112, C113, C114, C116, C117, C118, C119, C203, C206, C207, C208, C402, C500, C502, C600, C601, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621	CAP CER X7R 0402	0.1 µF	Murata	GRM155R71C104KA88D
1	C602	CAP CER chip	1800 pF	Panasonic	ECJ-0EB1E182K
1	C603	CAP CER	0.033 µF	Panasonic	0402YD333KAT2A
1	C604	CAP CER chip	1500 pF	Panasonic	ECJ-0EB1H152K
1	CR600	LED red surface mount	SML-LXT0805IW-TR	Lumex	SML-LXT0805IW-TR
1	E301	Inductor ferrite beads		Murata	BLMBIPG500SN1L (populate for ADA4960)
1	J101	CONN-PCB SMA ST edge mount	SMA-J-P-X-ST-EM1	Samtec	SMA-J-P-X-ST-EM1
1	J600	CONN-PCB coax SMA ST	JOHNSON142-0701-201	Johnson	142-0701-201
4	L100, L101, L102, L103	Inductor SM	10 nH	Panasonic	ELJ-RE10NGF2
2	P100, P601	CONN-PCB Berg HDR ST male 3P	SAMTECTSW10608GS3PIN	Samtec	TSW-103-08-G-S
1	P600	CONN-PCB header 8-pin double row	TSW-104-08-T-D	Samtec	TSW-104-08-T-D
1	R100	RES film SMD 0402	51	Panasonic	ERJ-2GEJ510X
14	R102, R103, R112, R115, R205, R209, R210, R504, R509, R510, R600, R606, R608, R610	RES film SMD 0402	0	Panasonic	ERJ-2GE0R00X
2	R106, R107	RES high precision SMD 0603	25	Vishay	P0603E25R0BNT
2	R113, R114	RES prec thick film chip R0402	200	Panasonic	ERJ-2RKF2000X
1	R116	Do not install (TBD_R0402)	TBD0402	TBD0402	TBD0402
5	R117, R118, R206, R411, R500	RES prec thick film chip R0402	10 K	Panasonic	ERJ-2RKF1002X
2	R120, R121	RES film SMD 0402	39	Panasonic	ERJ-2GEJ390X
2	R122, R123	RES film SMD 0402	100	Susumu	RG1005P-101-B-T5
3	R410, R413, R415	RES thick film chip	0	Multicomp	0402WGF0000TCE

Qty	Reference Designator	Description	Value	Mfg	Mfg_PN
13	R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524	RES prec thick film chip R0201	100	Panasonic	ERJ-1GEF1000C
5	R601, R602, R604, R607, R609	RES prec thick film chip R0402	1.00 K	Panasonic	ERJ-2RKF1001X
2	R605, R612	RES film SMD 0402	100	Venkel	CR0402-16W-1000FPT
3	R611, R615, R616	RES film SMD 0402	249	Venkel	CR0402-16W-2490FT
1	R613	RES prec thick film chip R0402	5.11 K	Panasonic	ERJ-2RKF5111X
1	R614	RES prec thick film chip R0402	4.12 K	Panasonic	ERJ-2RKF4121X
1	T100	XFMR RF 1:1	ETC1-1-13	Macom	ETC1-1-13
2	T101, T201	XFMR RF	ADT1-1WT	Mini-Circuits®	ADT1-1WT
6	TP100, TP400, TP401, TP402, TP403, TP500	CONN-PCB pin receptacle	3102-3-00-15-00-00-08-0	Mill-Max	3102-3-00-15-00-00-08-0
2	TP600, TP601	CONN-PCB pin vector	K24A	Vector	K24A
2	U200, U400	IC-ADI CMOS, quad SPDT switches	ADG734BRUZ	Analog Devices	ADG734BRUZ
1	U500	Precision series sub-band gap voltage ref	ADR130AUJZ	Analog Devices	ADR130AUJZ

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

www.analog.com