SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFG128064A-FPGA

VERSION : B

DATE : 2022.12.20

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2022.12.20 Sidney	GIFAR 2022.12.20 Hazel	GIFAR 2022.12.20 Roger

晶 發 科 技 股 份 有 限 公 司
GI FAR TECHNOLOGY CO.,LTD
新北市樹林區東豐街 81 號
No. 81, Dongfeng St, Shulin District, 238034, New Taipei City, Taiwan, R.O.C.
TEL: +886-2-8684-1188 FAX: +886-2-8684-8532

Revision Record

Data(y/m/d)	Ver.	Description	page
2009.03.02	00	New	18
2017.04.17	A	修改公司抬頭、格式統一	
2022.12.20	B	更新公司抬頭認證圖示	

CONTENTS

1. SCOPE

This specification covers the engineering requirements for the GFG128064A-FPGA liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 128 × 64 dot matrix LCD
- FSTN , Positive mode LCD panel
- Transflective , Normal temperature type
- 6 o'clock
- Back light: Edge LED (BLUE)
- Multiplexing driving : 1/65duty, 1/9bias
- Conteroller IC UC1601

2.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 × 64
Dot dimensions(mm)	0.334 × 0.403
Dot spacing (mm)	0.364 × 0.433
Module dimensions (Horizontal × Vertical × Thickness, mm)	56.6 × 44.2 × 7.65 max.
Viewing area (Horizontal × Vertical, mm)	50.6 × 31
Active area (Horizontal × Vertical, mm)	46.562 × 27.682

2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V_{DD}	V	-0.3 to +4.0
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+0.3

Note 1: Referenced to V_{SS}=0V

2.4 Electrical Characteristics (Without LED back-light)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.4		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq$ 2.4V, 25°C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geq$ 2.4V, 25°C	0.80		1.32	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.8V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	μA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2	3	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2	3	kΩ
F_{FR}	Average Frame Rate	LC[3] = 0b	66	76	--	Hz

2.5 Optical Characteristics Absolute maximum ratings

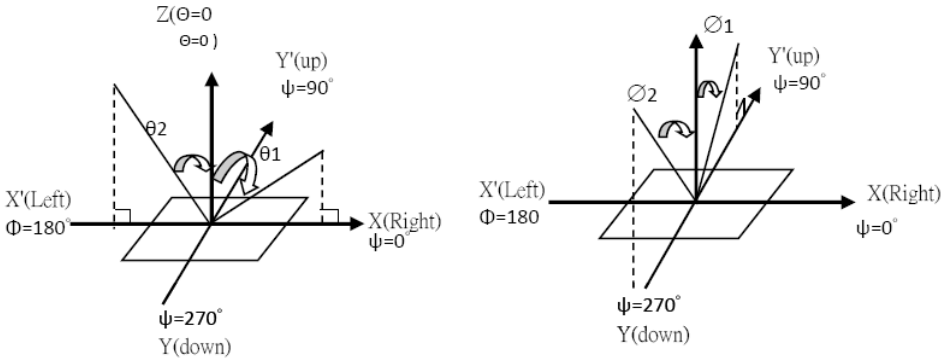
Item	Symbol	Rating	Unit
Operating temperature range	Top	0~50	°C
Storage temperature range	Tst	-20~70	°C

2.6. Optical Characteristics

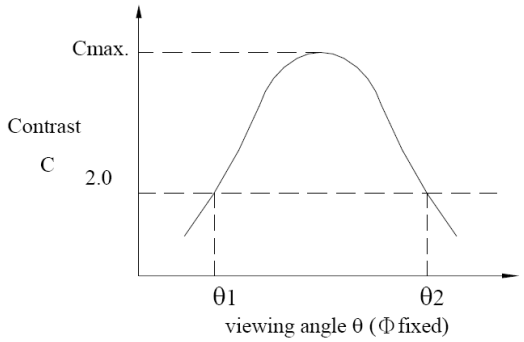
1/65 duty, 1/9 bias, Vop=10.2 V, Ta=25℃

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vop		9.9	10.2	10.5	
Viewing angle	θ1、θ2	C≥2.0,∅=0°C	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2.0	-	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	135	350ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	98	350ms	Note 4

Note 1: Definition of angles θ and ∅

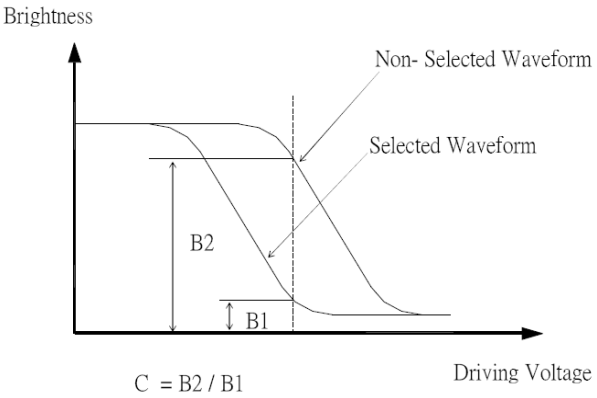


Note 2: Definition of viewing angles θ1 and θ2

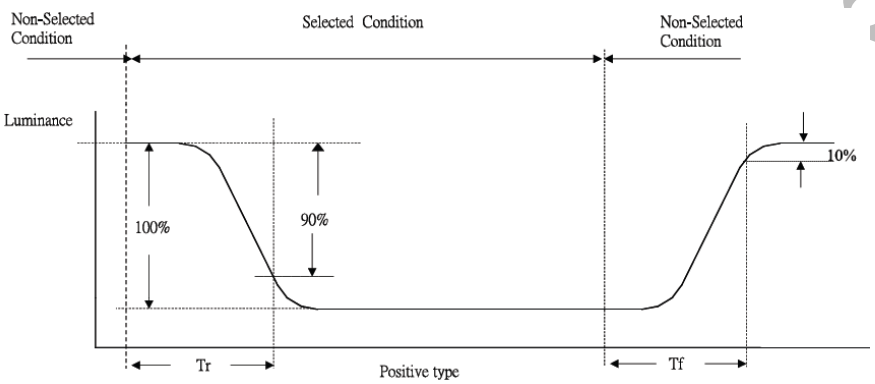


Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C



Note 4: Definition of response time



2.7 LED Back-light Characteristics

2.7.1 Electrical / optical specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	If=30mA, Blue	2.7	3.0	3.3	V
Wavelength	λρ	If=30mA, Blue	466	-	474	nm
Spectral Line half width	△λ	If=30mA, Blue	-	30	-	nm
LED *Luminous Intensity	I_V	If=30mA, Blue	50	100	--	cd/m^2
Reverse Current	I_R	VR=5V, Blue	--	--	30	uA
Luminous Uniformity	ΔLv	If=30mA, Blue	70			%

Note: * Measured at the bare LED back-light unit.

2.7.2 LED Maximum Operating Range

Item	**Symbol**	**BLUE**	**Unit**
Power Dissipation	P_{AD}	165	mW
Forward Current	I_F	50	mA
Reverse Voltage	V_R	10	V

3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	70℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-20℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	50℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	0℃	120 hrs	Appearance Without defect	
6	Thermal Shock	0℃, 30min. → 50℃,30min. (1cycle)		Appearance Without defect	10 cycles

** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

4. OPERATING INSTRUCTIONS

4.1 Input signal Function

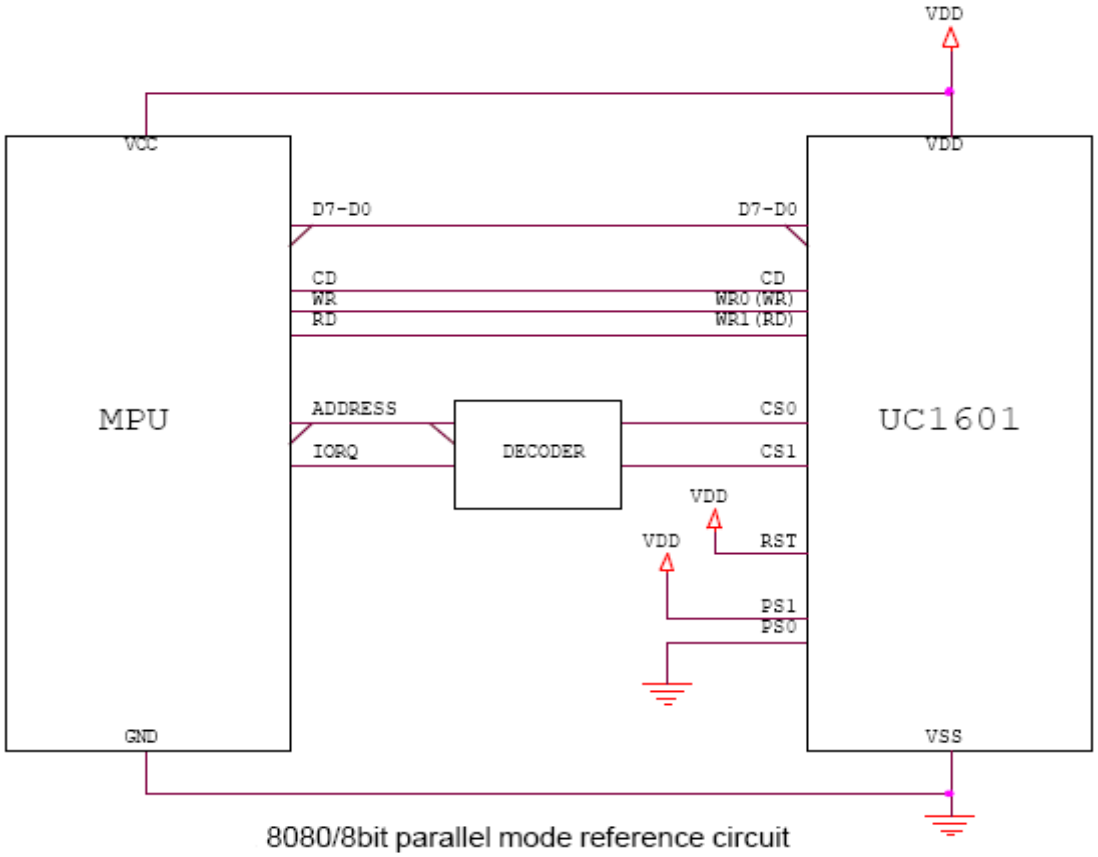
Pin No	Symbol	I/O	Function
1~4	NC	-	No Connection.
5	V_{LCD}	PWR	Main LCD power supply.
6	V_{B0+}	PWR	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}.
7	V_{B0-}	PWR	
8	V_{B1-}	PWR	
9	V_{B1+}	PWR	
10	VSS	PWR	Power Ground.
11	VDD	PWR	Power supply terminal VCC.
12	BM1	I	Bus mode: “HL”: 8080 “HH”: 6800
13	BM0	I	BM[1:0] “LH”: S9 “LL”: S8
14	DB7	I/O	Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect DB0 to SCK, DB3 to SDA.
15	DB6	I/O	
16	DB5	I/O	
17	DB4	I/O	
18	DB3/SDA	I/O	
19	DB2	I/O	
20	DB1	I/O	
21	DB0/SCK	I/O	
22	WR1	I	WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details. The meaning of WR [1:0] depends on whether the interface is in the 6800 mode, or the 8080 mode. In serial modes, these two pins are not used and can be connected to Vss.
23	WR0	I	
24	CD	I	Select the incoming command if it is a control instruction or for display data. CD pin is not used in S9 mode, connect it to Vdd or Vss. ”L”: control instruction ”H”: display data
25	RST	I	When RST=”L”, all control registers are re-initialized by their default states.
26	/CS0	I	Chip Select or Chip Address. In parallel mode and S8 mode, chip is selected when /CS0=”L”. When the chip is not selected, DB[7:0] will be high impedance.
27~30	NC	-	No Connection.

	BM=1x (Parallel)	BM=0x (Serial)
D0	D0	SCK
D1	D1	
D2	D2	
D3	D3	SDA
D4	D4	
D5	D5	
D6	D6	-
D7	D7	-

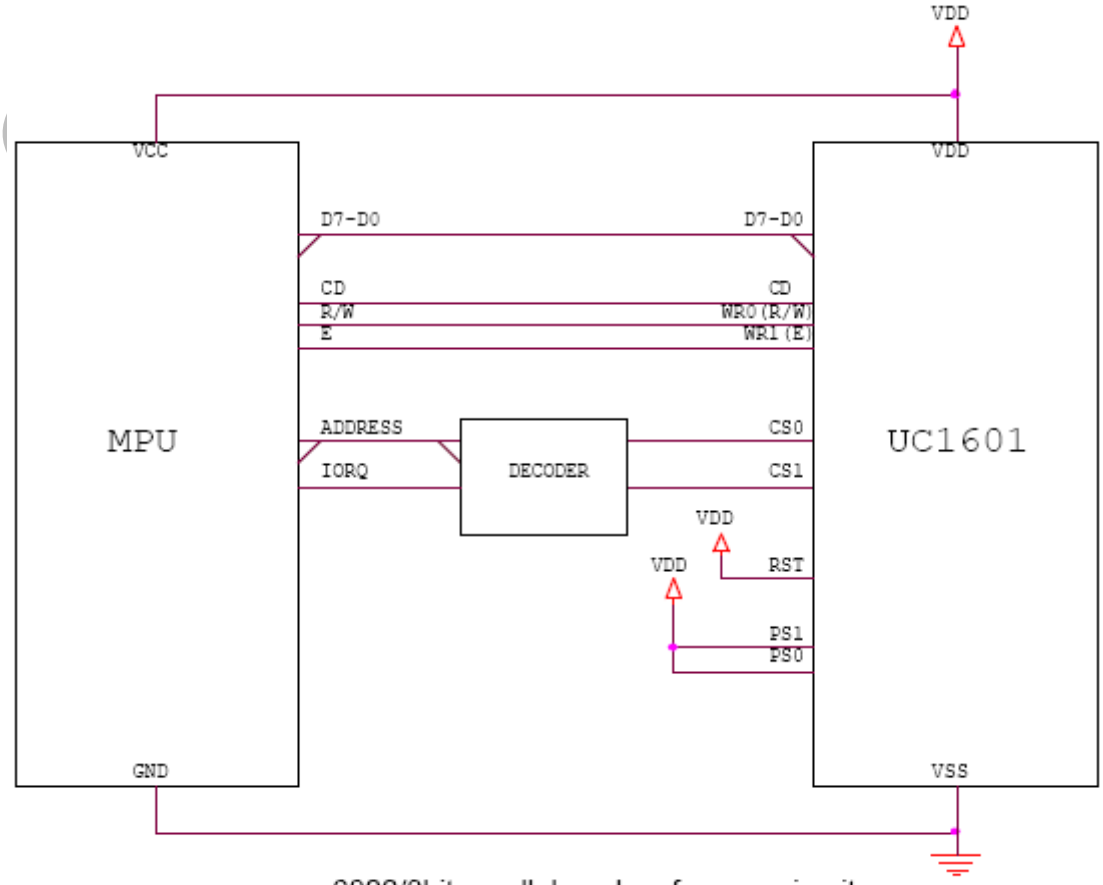
Bus Type		8080	6800	SPI (S8)	SPI (S9)
Control & Data Pins	BM[1:0]	10b	11b	00b	01b
	CS[1:0]	Chip Select			
	CD	Control/Data			–
	WR0	$\overline{WR}$	R/$\overline{W}$	–	
	WR1	$\overline{RD}$	EN	–	
	Access	Read/Write		Write Only	
	D[7:0]	8-bit bus (Tri-state)		D0=SCK, D3=SDA	

* Connect unused control pins and data bus pins to V_{DD} or Vss

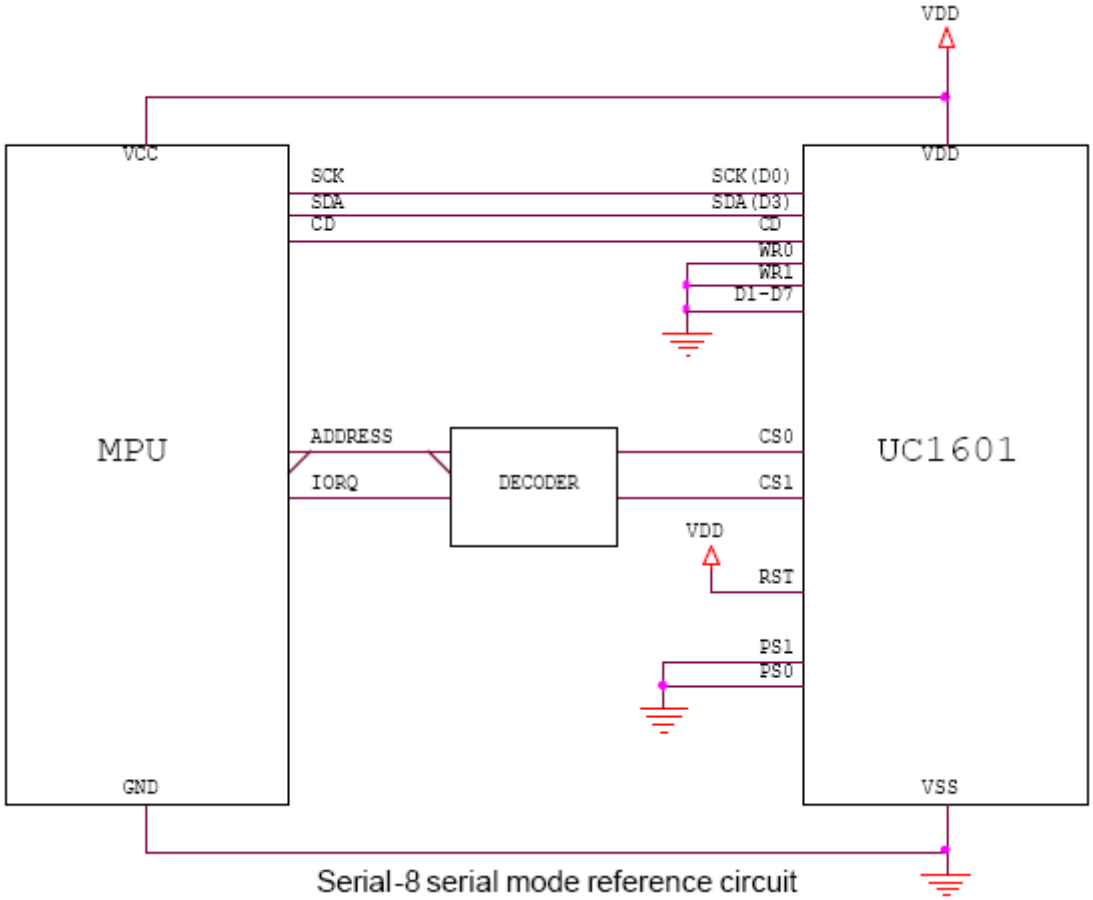
4.2 Voltage Generator Circuit



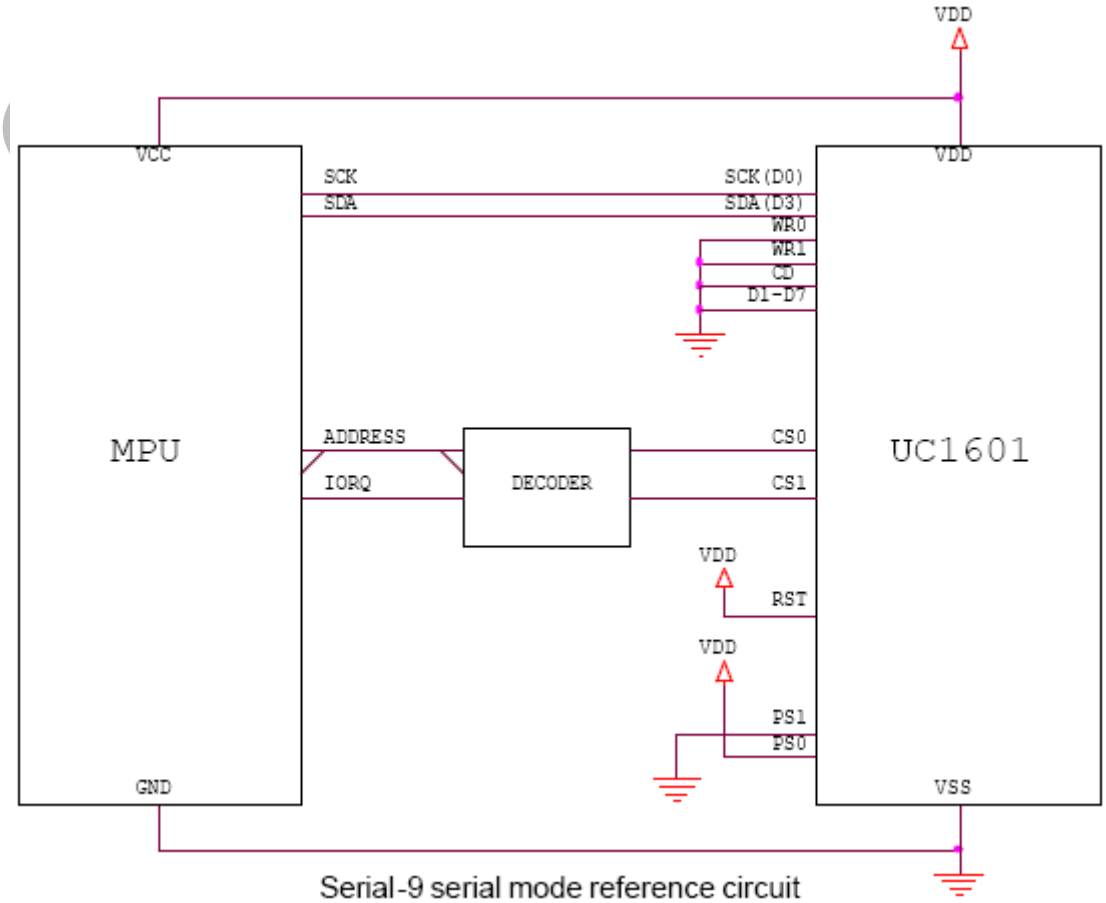
8080/8bit parallel mode reference circuit



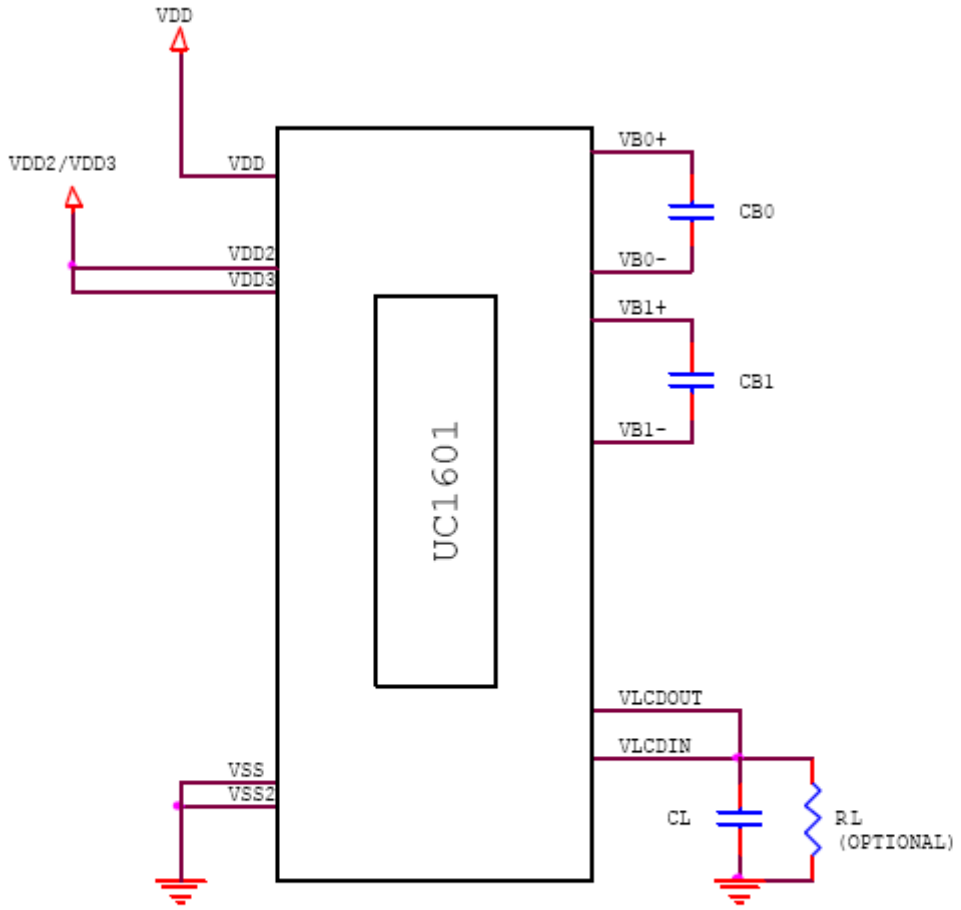
6800/8bit parallel mode reference circuit



Serial-8 serial mode reference circuit



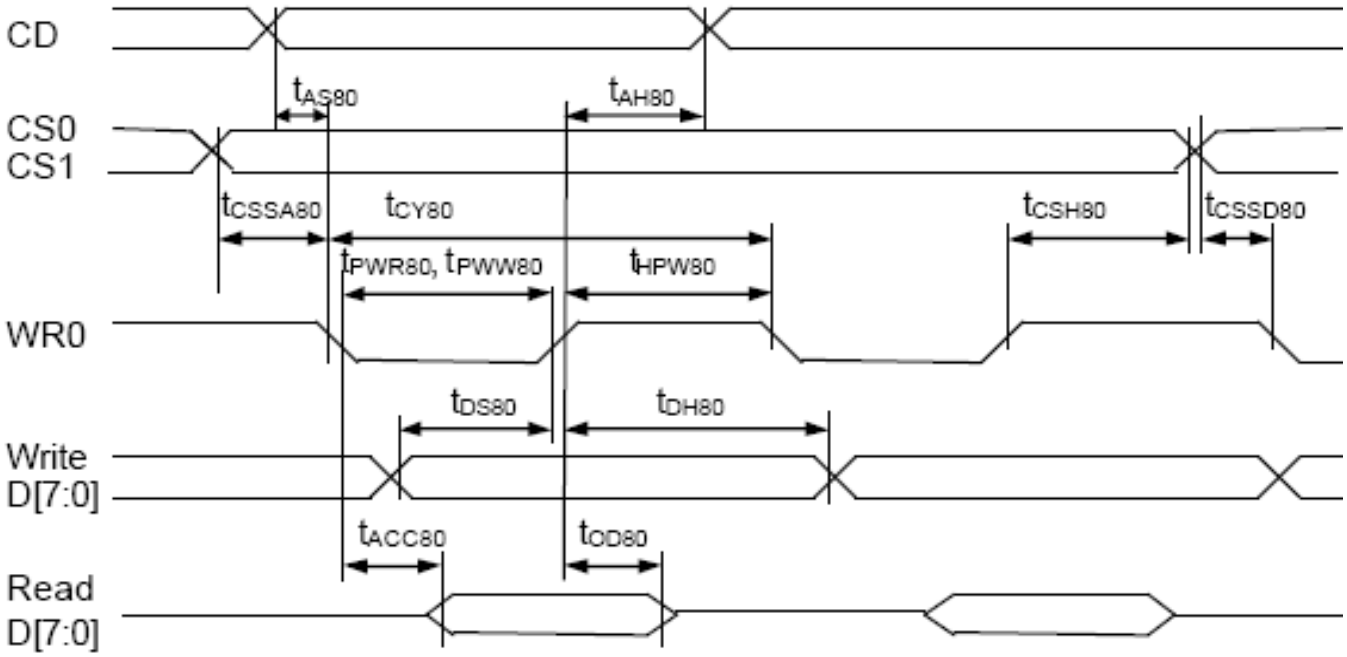
Serial-9 serial mode reference circuit



Note

- Recommended component values:
  C_B: 100x~200x LCD load capacitance or 1.0uF (2V), whichever is higher.
  C_L: 10nF ~ 30nF (25V) is appropriate for most applications.
  R_L: 10MΩ. Acts as a draining circuit when the pow er is abnormally shut down.

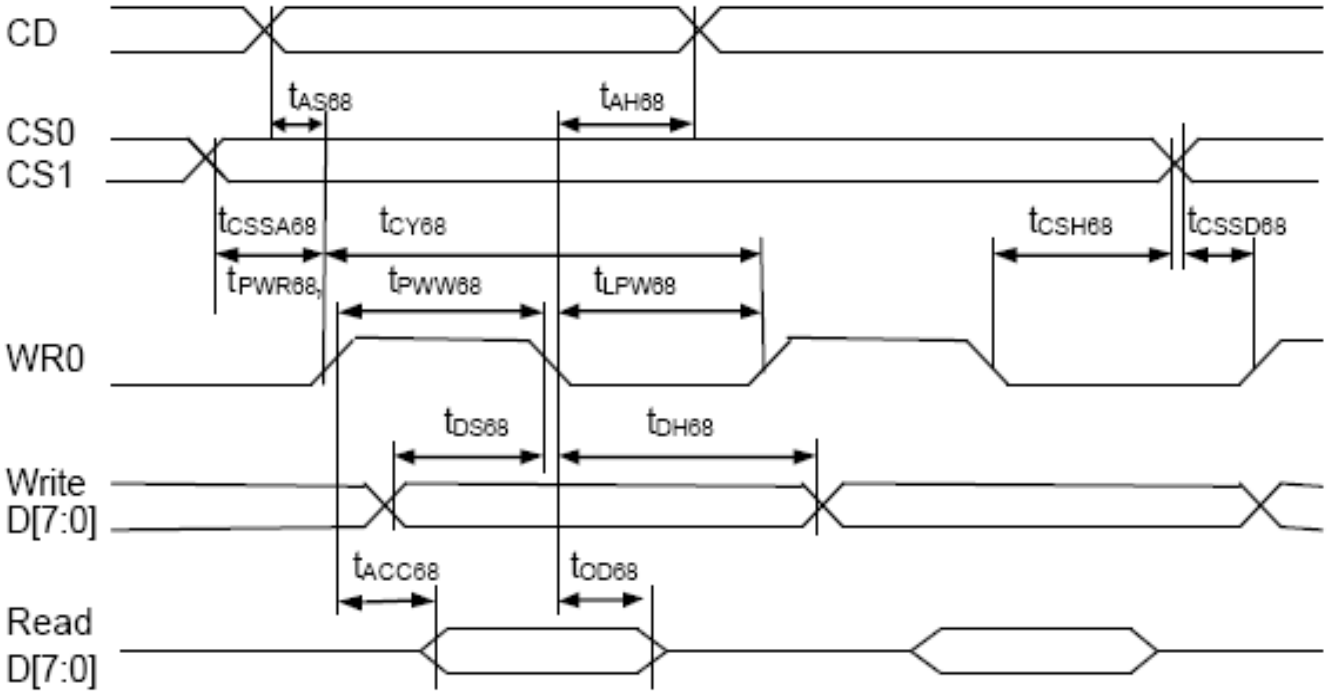
4.3 Timing Diagram



Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

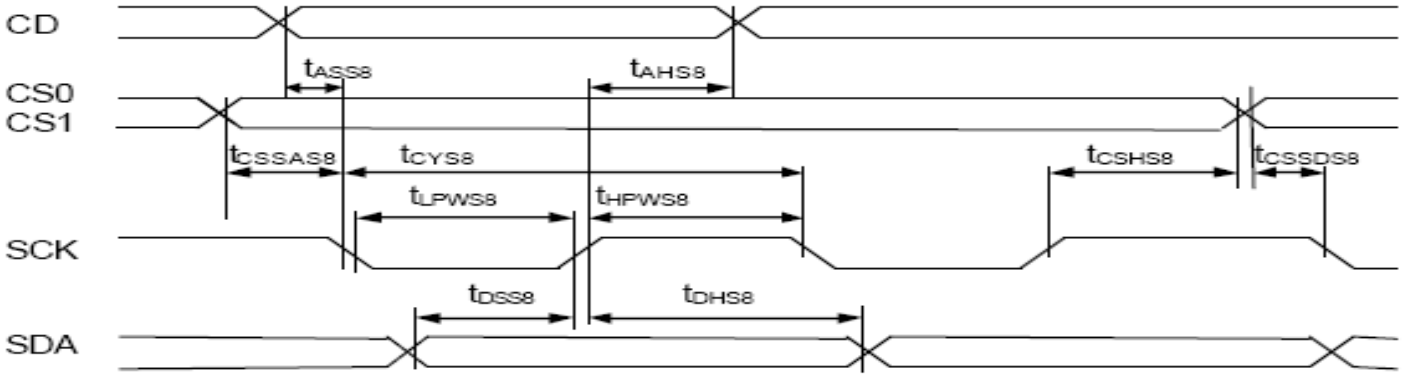
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY80}		System cycle time		135	–	nS
t_{PWR80}	WR1	Pulse width (read)		65	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80} t_{DS80} t_{DH80}	WR0, WR1 D0~D7	High pulse width Data setup time Data hold time		65 30 20	– –	nS nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS



Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

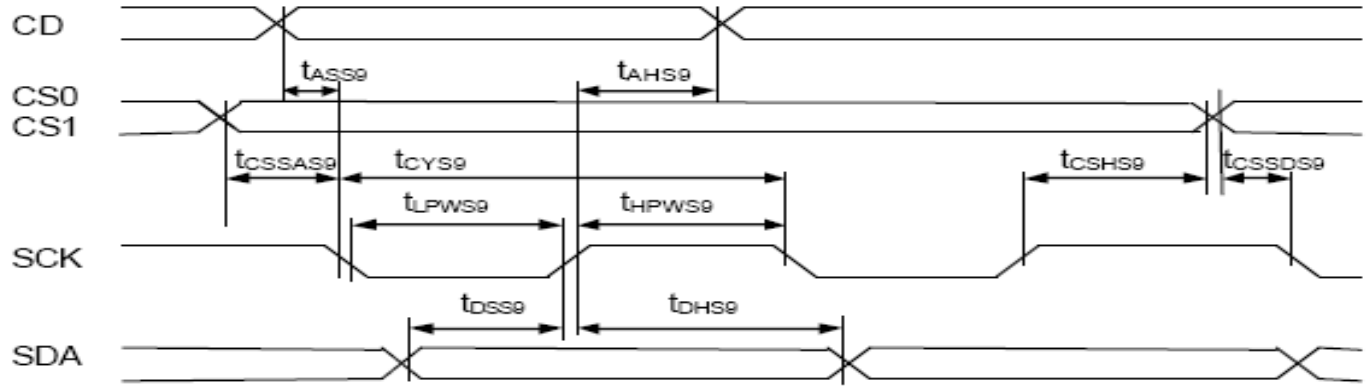
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		0	–	nS
t_{AH68}		Address hold time		40		
t_{CY68}		System cycle time		135	–	nS
t_{PWR68}	WR1	Pulse width (read)		65	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width		65	–	nS
t_{DS68}	D0~D7	Data setup time		30	–	nS
t_{DH68}		Data hold time		15		
t_{ACC68}		Read access time	C_L = 100pF	–	50	nS
t_{OD68}		Output disable time		10	50	
T_{CSSA68}	CS1/CS0	Chip select setup time		10		nS
T_{CSSD68}				10		
T_{CSH68}				20		



Serial Bus Timing Characteristics (for S8)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		40	–	nS
t_{CYS8}	SCK	System cycle time		135	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8}	SDA	Data setup time		30	–	nS
t_{DHS8}		Data hold time		15		
t_{CSSAS8}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS8}				10		
t_{CSHS8}				20		



Serial Bus Timing Characteristics (for S9)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS9}	CD	Address setup time		0	–	nS
t_{AHS9}		Address hold time		40	–	nS
t_{CYS9}	SCK	System cycle time		135	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9}	SDA	Data setup time		30	–	nS
t_{DHS9}		Data hold time		15		
t_{CSSAS9}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS9}				10		
t_{CSHS9}				20		

5. NOTES

▪ Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 ^{o}C±10 ^{o}C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

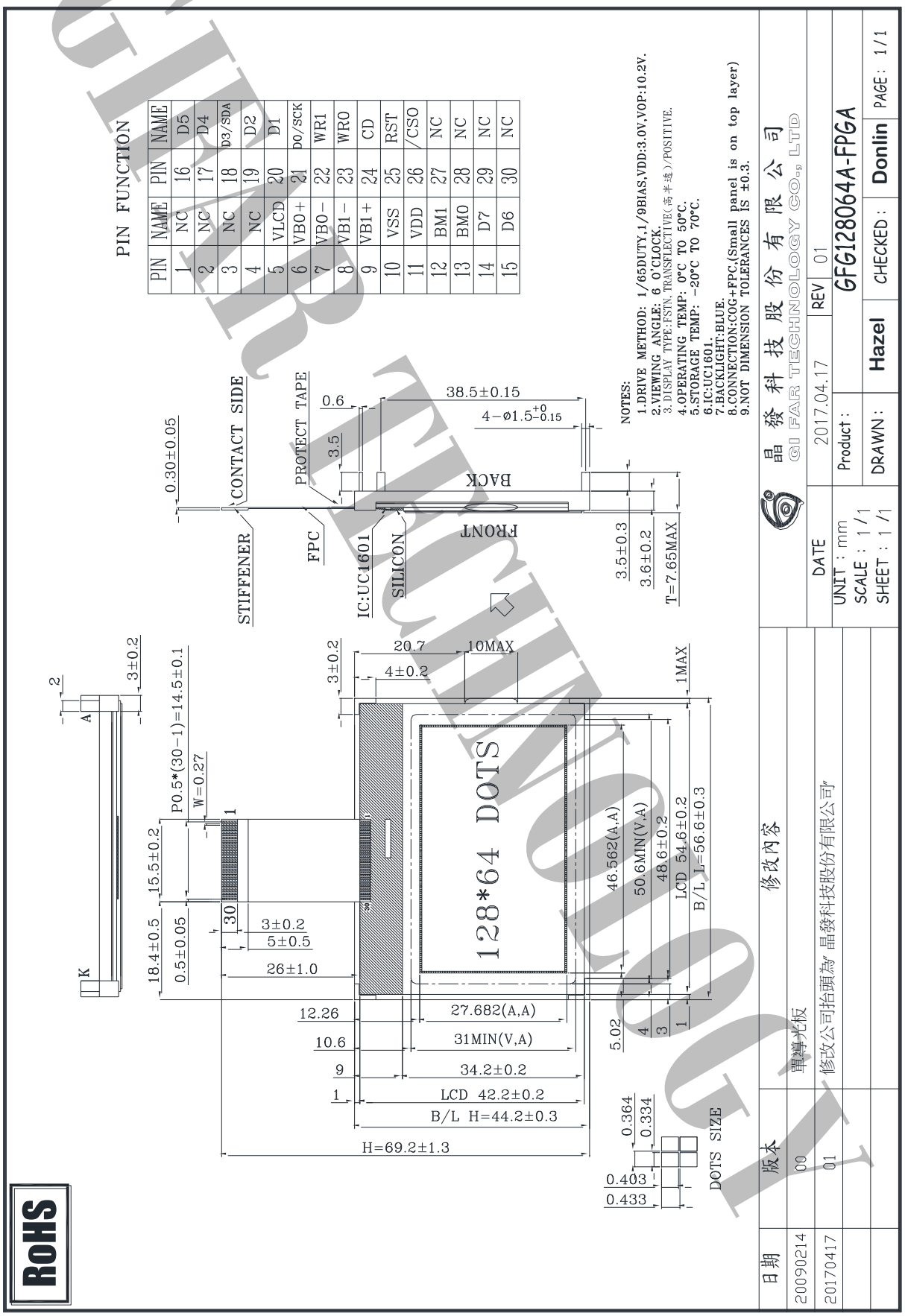
- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

Quality warranty period: Within one year after shipment date (excluding abnormal usage way and abnormal environments.)

7. LCM Dimension



8. PACKAGE INFORMATION

1	1 Tray	:	15 pcs (modules)
2	1 stack	:	10 tray +1 Cover tray
3	1 Carton	:	2 stack
4	Total pcs	:	1 Carton = 300 pcs
5	Carton size = NO. 17	:	495*315*435mm
6	Net weight	:	4.1 KG
7	Gross weight	:	10 KG

** Packaging information**

- **1 Tray = 15 pcs**

- **1 stack=10 tray+1 Cover tray** ****Each layer of tray should be staggered stacked**

- **1 Carton = 2 stack Total pcs = 300 pcs**

出貨檢驗標準書

Shipping inspection standard

核准 Approved by	審核 Checked by	作成 Made by
ANDY	JACKY	RUBY

1.目的 Purpose：
規範出貨產品之檢驗項目及判斷標準，確保產品出貨能滿足客戶要求。
Standardize the inspection items and judgment standards to ensure the products that shipped out can meet customer's requirements.

2.範圍 Area：
適用於出廠之所有產品。
Applicable to all products shipped from the factory.

3.名詞解釋 Explanation of terms：
3-1 主要缺陷：亦會造成功能缺失或嚴重外觀缺陷。
Major Defects: It also causes loss of function or serious appearance defects.

3-2 次要缺陷：稍有缺陷但不影響客戶使用。
Minor defect: Slightly defective but does not affect customer use.

4.檢驗體制 Inspection system：
4-1 抽樣計劃：依 ANSI/ASQ Z1.4 一般檢驗水準Ⅱ 之 正常檢驗一次抽驗方案。
Sampling plan: According to ANSI/ASQ Z1.4 general inspection level Ⅱ the normal inspection one-time sampling plan.

4-2 允收水準 Acceptable Level：(AQL)
主要缺陷 Major defect：0.4 %
次要缺陷 Minor defect：0.65 %

5.檢驗條件 Inspection conditions：
5-1 使用相關之檢測儀器及測試、量測工具。
Use relevant testing instrument, testing and measuring tools .

5-2 環境要求：其條件需控制在常溫下 23℃±3℃及溼度 70%RH 以下。
Environmental requirements: The conditions should be controlled at room temperature 23℃±3℃ and humidity below 70%RH.

5-3 外觀檢驗：須在 380±20% LUX 的白色日光燈下，其目視距離需於產品離 30±5 cm 檢驗。
Appearance inspection: Under the white fluorescent lamp of 380±20% LUX , the visual distance shall be checked above the product 30 ± 5 cm.

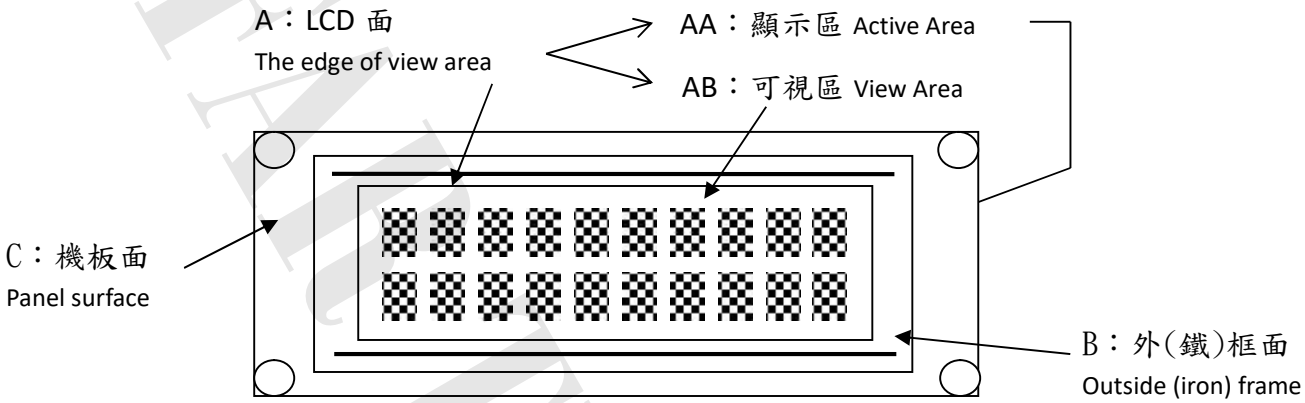
5-4 電性測試 Electrical Testing：
5-4-1 有背光之產品需關燈並在 5~300Lux±3%下檢驗。
The products with backlight should be tested at 5~300±3% Lux.

5-4-2 無背光之產品需開燈並在 60~300Lux±3%白色日光燈下檢驗。
Products without backlight need to be turned on and tested under 60~300 ± 3% LUX white fluorescent lamps .

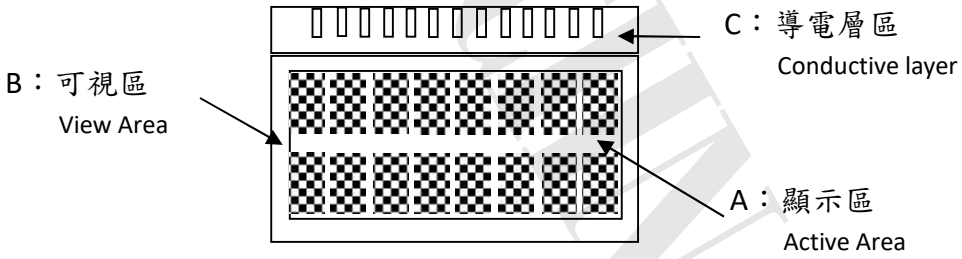
5-5 檢查視角依產品視角方向。
Check the viewing angle according to the product viewing angle.

5-6 其不良現象檢視區域 Bad phenomenon View area

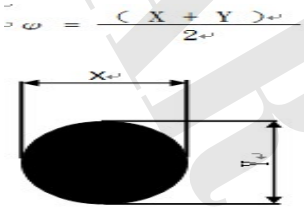
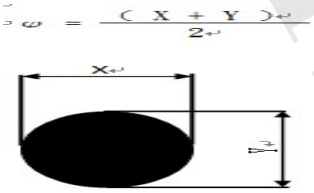
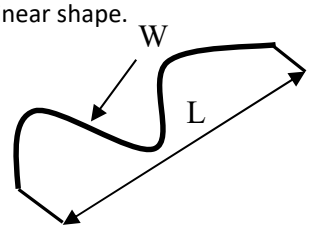
5-6-1 適用種類 Applicable category：COB、TFT



5-6-2 適用種類 Applicable category：COG、TAB、TN



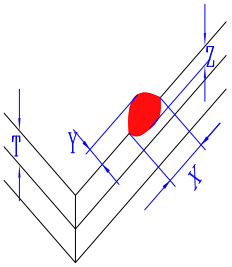
COG

<table>
<tr><td colspan="2">種類 Category</td><td colspan="4">COG</td></tr>
<tr><td>編號
No.</td><td>檢驗項目
Item</td><td colspan="2">檢驗內容及判定標準
Inspection Content & Standard</td><td>區域
Zone</td><td>類別
Category</td><td>缺陷等級
Level</td></tr>
<tr><td>1</td><td>點類(一)
Dot(1)</td><td>黑點、刺傷…等圓狀
Black dot、Stab…and other round shape
  </td><td>兩點距離須超過 5 ㎜
Two points have to be ≧ 5 mm<table><tr><td>φ (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>ϕ ≦ 0.1</td><td>無視 Ignore</td></tr><tr><td>0.1 < ϕ ≦ 0.25</td><td>3</td></tr><tr><td>0.25 < ϕ ≦ 0.3</td><td>1</td></tr><tr><td>ϕ > 0.3</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>2</td><td>點類(二)
Dot(2)</td><td>氣泡、凹凸點
Bubble、Uneven dots
  </td><td>兩點距離須超過 5 ㎜
Two points have to be ≧ 5 mm<table><tr><td>φ (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>ϕ ≦ 0.2</td><td>無視 Ignore</td></tr><tr><td>0.2 < ϕ ≦ 0.5</td><td>2</td></tr><tr><td>ϕ > 0.5</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>3</td><td>線類
Line</td><td>刮傷、毛屑…等線狀
Scratch、Fiber.. and other linear shape.
  </td><td><table><tr><td>L (㎜)</td><td>W (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>--</td><td>W ≦ 0.02</td><td>無視 Ignore</td></tr><tr><td>L ≦ 5</td><td>W ≦ 0.03</td><td>3</td></tr><tr><td>L ≦ 3</td><td>W ≦ 0.05</td><td>2</td></tr><tr><td>L > 5</td><td>W > 0.05</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>4</td><td>底色
Background color</td><td colspan="2">同批供貨不能有明顯色差
No obvious color difference allowed in same shipment.
(必要時與客端制定限度樣)
(According to the gold samples if necessary)</td><td>B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>5</td><td>FPC 外觀
FPC Appearance</td><td colspan="2">※ FPC 上刺傷導致線路無法導通 拒收
Stabbing on the FPC causes the line to fail to conduct
Reject
※ FPC 上髒污或是殘留異物以致線路無法導通 拒收
Dirty or residual foreign matter on the FPC makes the circuit unable to conduct
Reject
※ FPC 直角折痕、斷裂 拒收
FPC right-angle crease and fracture Reject</td><td>C</td><td>外觀
Appearance</td><td>主要
Major
AQL 0.4%</td></tr>
</table>

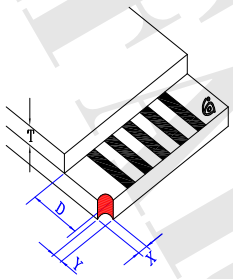
COG

6	點、線類 (三) Dot、Line (3)	※ 於全黑、白畫面下看見之區塊狀或線狀不良　拒收 There is a block or linear in the view area under the screen is whole black or white. Reject ※ 但依 2% ND Filter 遮蓋無視　允收 But after inspecting by 2% ND Filter without seeing block or linear, it is confirmed Acceptance	A	電訊 Electronics	次要 Minor AQL0.65%
7	點、線類 (四) Dot、Line (4)	畫面中顯示出現黑、白、亮、異色點或線狀 There is a black, white, bright or other dot or lines showing in the view area. ※ 依編號 1、3 之判定標準 According to the inspection standard: No. 1 and 3.	A	電訊 Electronics	次要 Minor AQL0.65%
8	缺字 Lack of characters	顯示時畫面缺少部份字元　拒收 Lacking part of characters in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
9	無動作 No reaction	顯示畫面一直處於起始畫面而無法進行切換　拒收 The display (view area) always show in the initial screen and can't be switched to others. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
10	無畫面 No display	通電後，完全無任何畫面顯示　拒收 After connecting to the power, there is no image. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
11	斷線 Broken line	顯示畫面中少直、橫線　拒收 There is a lack of vertical or horizontal lines in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
12	CROSS TALK	顯示畫面時有局部之條紋或拖影 There are some stripes or shadow/smear showing in the view area. 拒收或與客端簽訂限度樣 Reject or inspect according to the golden sample	A	電訊 Electronics	次要 Minor AQL0.65%
13	I CON	顯示畫面缺少部份顯示圖案　拒收 Lack of partial ICON in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%

COG

<table>
<tr><td>14</td><td>深淺不一
Color difference</td><td>顯示畫面的對比，比其他顯示深或淺並依電氣規格(VOP)值判定
The color contrast of display is obviously lighter or darker than others and according to the VOP value in the electronics specification.
拒收或與客端簽訂限度樣
Reject or inspect according to the golden sample</td><td>A</td><td>電訊
Electronics</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>15</td><td>畫面異常
Abnormal screen</td><td>通電後畫面出現未定義之電訊不良現象　拒收
After connecting to the power, there is an undefined electronics appearance showing in the view area.
Reject</td><td>A</td><td>電訊
Electronics</td><td>主要
Major
AQL 0.4%</td></tr>
<tr><td>16</td><td>背光色不均
Uneven color of backlight</td><td>※ 點亮後 LED 有明暗不均現象依其均勻度判定　拒收
After lighting LEDs have brightness and darkness uneven the determined according to its uniformity.
Reject
※ 點亮後 LED 色澤不一致　拒收
LED color is inconsistent after lighting.
Reject</td><td>A</td><td>電訊
Electronics</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>17</td><td>亮度不足
Lack of brightness</td><td>波長、色座標、輝度與圖面標示定義不符　拒收
Wave length, chromatic coordinates, brightness don’t correspond to the definition of the drawing.
Reject</td><td>A</td><td>電訊
Electronics</td><td>主要
Major
AQL 0.4%</td></tr>
<tr><td>18</td><td>背光腳柱
Backlit foot post</td><td>斷裂、長度不一　拒收
Fracture, different length
Reject</td><td>--</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>19</td><td>破損
Damaged</td><td>  </td><td>Y：破損寬 X：破損長
Y: Damaged width X: Damaged length
<table>
<tr><th>Y</th><th>X</th><th>判定
Determination</th></tr>
<tr><td>Y ≦1.0</td><td>-- --</td><td>允收
Acceptance</td></tr>
<tr><td>未進入可視區
Did not enter the viewing area</td><td>≦1/8 玻璃該邊長
≦1/8 The side length of the glass</td><td>允收
Acceptance</td></tr>
<tr><td>進入可視區
Enter the viewing area</td><td>-- --</td><td>拒收
Reject</td></tr>
</table></td><td>B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
</table>

COG

<table>
<tr>
<td>20</td>
<td>角崩
Corner collapse</td>
<td>  </td>
<td>Y：破損寬 X：破損長
Y: Damaged width X: Damaged length
<table>
<tr><th>Y</th><th>X</th><th>判定
Determination</th></tr>
<tr><td>≦1/3D</td><td>-- --</td><td>允收
Acceptance</td></tr>
<tr><td>1/3D < Y ≦ D</td><td>≦1/8 玻璃邊長
≦1/8 The side length of the glass</td><td>允收
Acceptance</td></tr>
<tr><td>> D</td><td>-- --</td><td>拒收
Reject</td></tr>
</table></td>
<td>C</td>
<td>外觀
Appearance</td>
<td>次要
Minor
AQL0.65%</td>
</tr>
<tr>
<td>21</td>
<td>尺寸量測
Size Measurement</td>
<td>未依圖面上標示 拒收
No correspond to the indication on the drawing.
Reject</td>
<td>ALL</td>
<td>外觀
Appearance</td>
<td>主要
Major
AQL 0.4%</td>
</tr>
<tr>
<td>22</td>
<td>其他
Other</td>
<td>如發現有上述未定義之不良則與客端簽訂限度樣
If there is another undefined defective situation. It will be listed as others. The inspection standard is according to the golden sample.</td>
<td>ALL</td>
<td>電訊
Electronics
外觀
Appearance</td>
<td>次要
Minor
AQL0.65%</td>
</tr>
</table>