HV66

32-Channel LCD Driver with Separate Backplane Output

Features

- 32-Channel High-Voltage Push-Pull Outputs
- Up to 60V Output Voltage
- Low-Power Level Shifting
- 5 MHz Shift Register Speed
- Latched Data Outputs
- Bidirectional Shift Register (DIR)
- Backplane Output

Applications

- LCD Drivers
- Display Drivers
- Inkjet Drivers
- 3D Printer Drivers
- Microelectromechanical Systems Applications

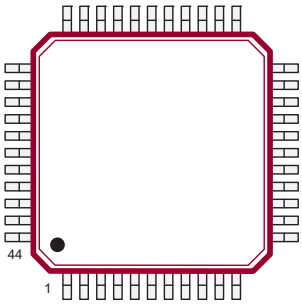
General Description

The HV66 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. This device is designed as a driver circuit for LCD displays. It can also be used in any application requiring multiple-output high-voltage current sourcing-and-sinking capabilities. The inputs are fully CMOS compatible.

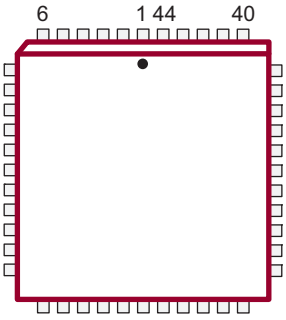
The device consists of a 32-bit Shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. The $HV_{OUT}1$ is connected to the first stage of the Shift register. Data is shifted through the Shift register on the logic rising transition of the clock. A DIR pin causes data shifting to move in a clockwise direction when grounded. When connected to V_{DD}, the pin causes data shifting to move in a counter clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. The operation of the Shift register is not affected by the latch enable (LE), blanking ($\overline{BL}$) and the polarity (POL) inputs. Transfer of data from the Shift register to the latch occurs when the latch enable (LE) input is high. The data in the latch is stored after LE transitions from high to low.

Package Types

44-lead PQFP
(Top view)

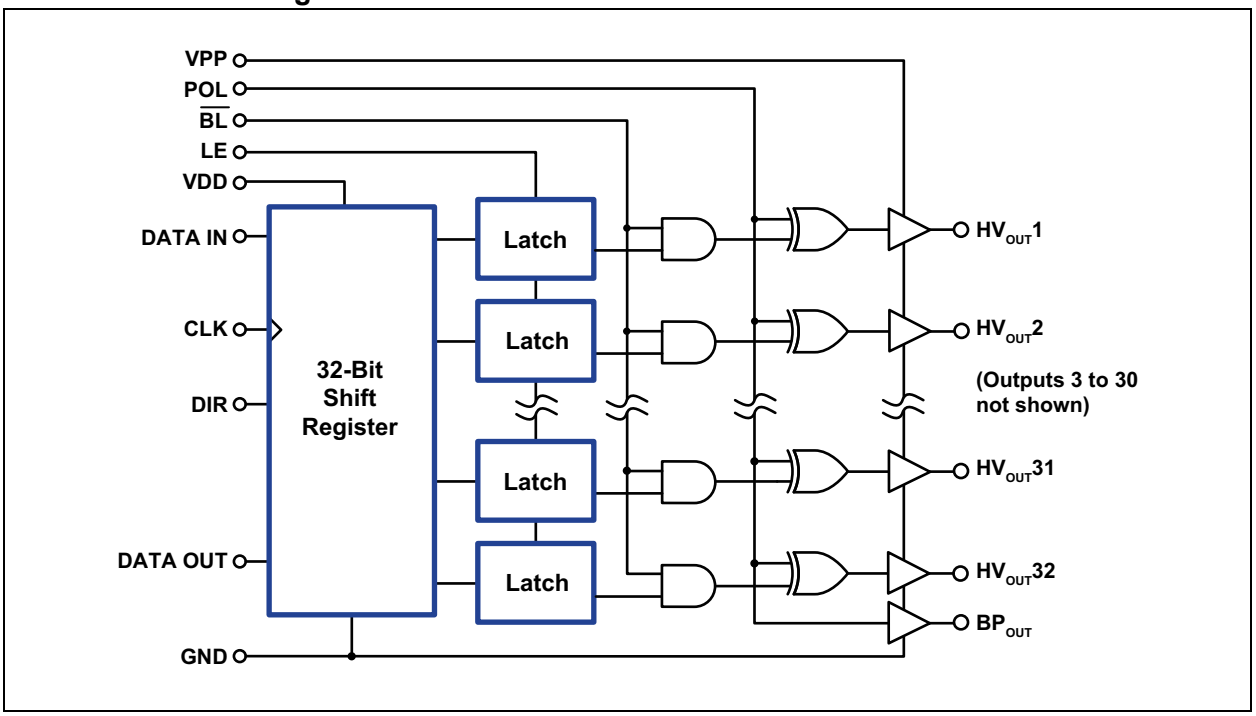


44-lead PLCC
(Top view)

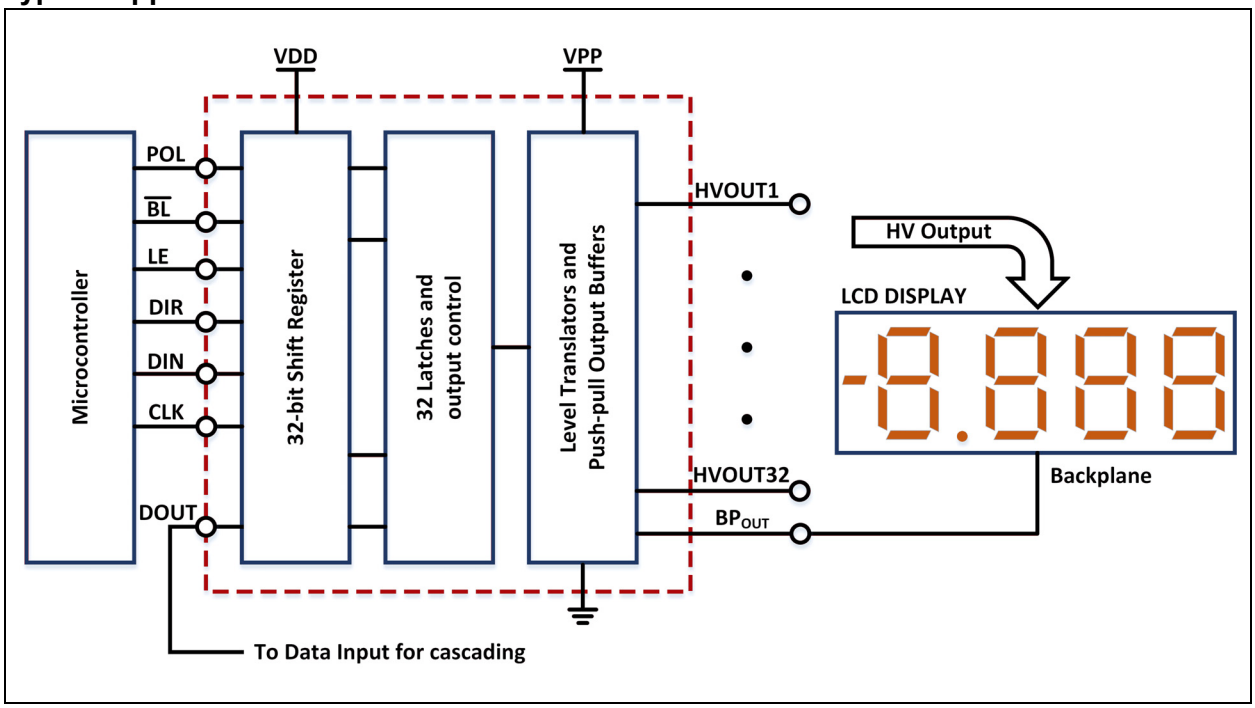


See Table 2-1 and Table 2-2 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage, V_{DD} (**Note 1**) ..... –0.5V to +7V
High-Voltage Supply Voltage, V_{PP} (**Note 1**) ..... –0.5V to +70V
Logic Input Levels ..... –0.5V to V_{DD}+0.5V
Ground Current (**Note 2**) 1.5A
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +125°C
Continuous Total Power Dissipation:
44-lead PQFP (**Note 3**) ..... 1200 mW
44-lead PLCC (**Note 3**) ..... 1200 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: All voltages are referenced to GND.
2: Duty cycle is limited by the total power dissipated in the package.
3: For operations above 25°C ambient, derate linearly to 85°C at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High-Voltage Supply Voltage	V_{PP}	12	—	60	V	
High-Level Input Voltage	V_{IH}	2.4	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.8	V	
Clock Frequency	f_{CLK}	0	—	5	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Allowable Current through Output Diodes	I_{OD}	—	—	200	mA	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated. V_{DD} = 5V, V_{PP} = 60V.							
Parameter		**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{DD} Supply Current		I_{DD}	—	—	15	mA	f_{CLK} = 5 MHz, V_{DD} = 5.5V
Quiescent V_{PP} Supply Current		I_{PPQ}	—	—	0.5	mA	
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	0.5	mA	All V_{IN} = GND or VDD
High-Level Logic Input Current		I_{IH}	—	—	1	µA	$V_{IH} = V_{DD}$
Low-Level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V
High-Level Output Data Out	HV_{OUT}	V_{OH}	50	—	—	V	I_O = –5 mA, V_{PP} = 60V
	Data Out		4.6	—	—	V	I_O = –100 µA
Low-Level Output Voltage	HV_{OUT}	V_{OL}	—	—	8	V	I_O = 5 mA, V_{PP} = 60V
	Data Out		—	—	0.4	V	I_O = 100 µA
Low-Level Output Voltage, Backplane		V_{OLBP}	—	—	3	V	I_O = 10 mA
High-Level Output Voltage, Backplane		V_{OHBP}	57	—	—	V	I_O = –10 mA

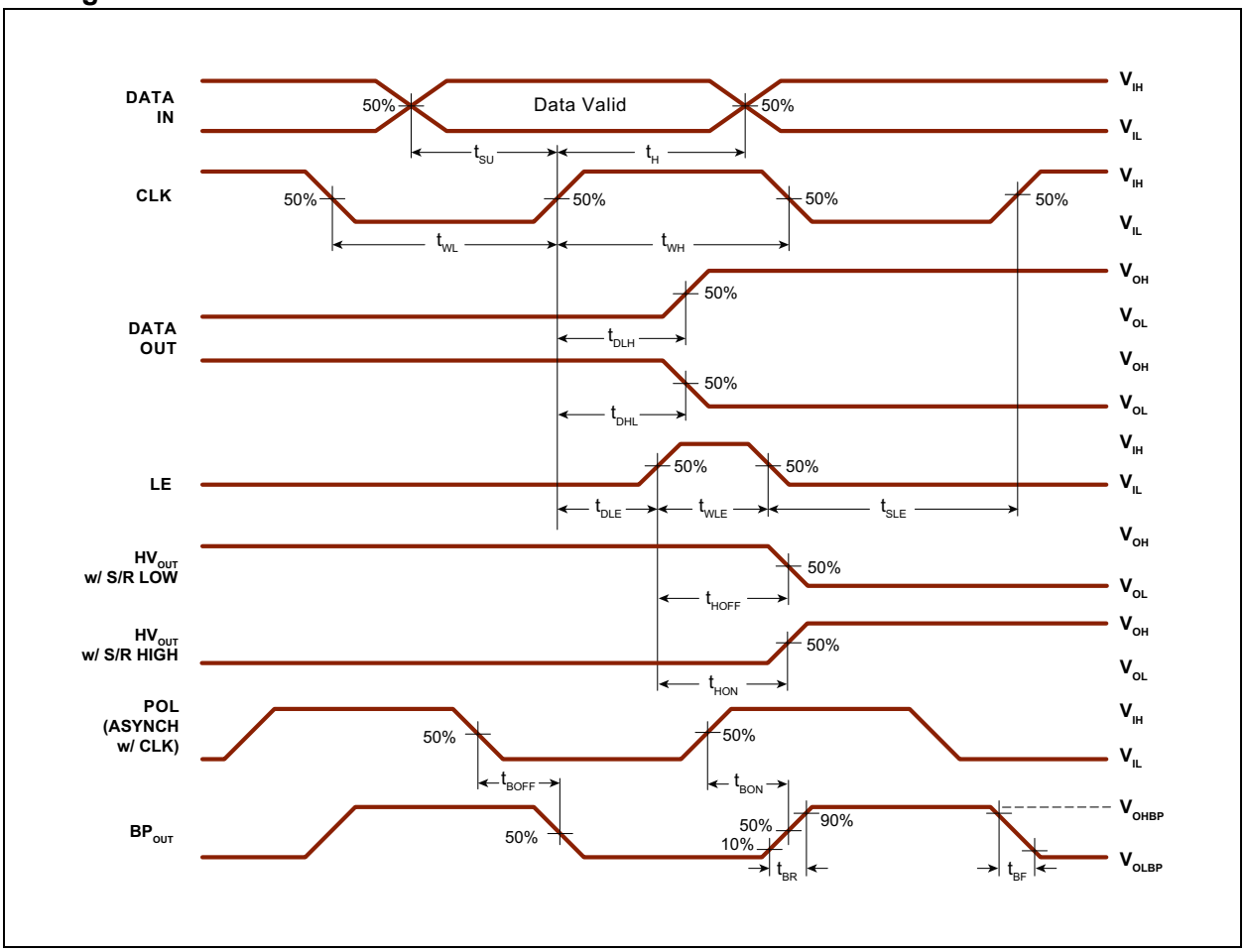
AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 5V, V_{PP} = 60V, T_A = 25°C, Logic Input Rise/Fall Time = 10 ns.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Clock Frequency	f_{CLK}	—	—	5	MHz	
Clock Width, High or Low	t_{WL}, t_{WH}	100	—	—	ns	
Data Setup Time before Clock Rises	t_{SU}	25	—	—	ns	
Data Hold Time after Clock Rises	t_H	50	—	—	ns	
Time from Latch Enable or POL to HV_{OUT}	t_{HON}, t_{HOFF}	—	—	500	ns	C_L = 20 pF
Time from POL to BP_{OUT}	t_{BON}, t_{BOFF}	—	—	500	ns	C_L = 20 pF
Delay Time Clock to Data High to Low	t_{DHL}	—	—	200	ns	C_L = 10 pF
Delay Time Clock to Data Low to High	t_{DLH}	—	—	200	ns	C_L = 10 pF
Delay Time Clock to Latch Enable Low to High	t_{DLE}	50	—	—	ns	
Latch Enable Pulse Width	t_{WLE}	100	—	—	ns	
Latch Enable Setup Time before Clock Falls	t_{SLE}	50	—	—	ns	
BP_{OUT} Rise and Fall Time	t_{BR}, t_{BF}	10	—	1000	µs	C_L = 350 pF
BP_{OUT} Rise and Fall Time Difference	$\lvert t_{BR}–t_{BF} \rvert$	—	—	100	µs	C_L = 350 pF

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–65	—	+125	°C	
PACKAGE THERMAL RESISTANCE						
44-lead PQFP	θ_{JA}	—	51	—	°C/W	
44-lead PLCC	θ_{JA}	—	37	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV66 44-lead PQFP and 44-lead PLCC are in Table 2-1 and Table 2-2, respectively. Refer to **Package Types** for the location of pins.

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT11	High-voltage output
2	HVOUT12	High-voltage output
3	HVOUT13	High-voltage output
4	HVOUT14	High-voltage output
5	HVOUT15	High-voltage output
6	HVOUT16	High-voltage output
7	HVOUT17	High-voltage output
8	HVOUT18	High-voltage output
9	HVOUT19	High-voltage output
10	HVOUT20	High-voltage output
11	HVOUT21	High-voltage output
12	HVOUT22	High-voltage output
13	HVOUT23	High-voltage output
14	HVOUT24	High-voltage output
15	HVOUT25	High-voltage output
16	HVOUT26	High-voltage output
17	HVOUT27	High-voltage output
18	HVOUT28	High-voltage output
19	HVOUT29	High-voltage output
20	HVOUT30	High-voltage output
21	HVOUT31	High-voltage output
22	HVOUT32	High-voltage output
23	DATA OUT	Data output pin
24	GND	Supply ground
25	NC	No connection
26	$\overline{BL}$	Blanking pin
27	POL	Polarity pin
28	LE	Latch enable pin
29	VDD	Logic supply voltage
30	CLK	Clock pin
31	DIR	Direction pin
32	DATA IN	Data input pin
33	VPP	High-voltage power supply
34	BPOUT	Back plane output
35	HVOUT1	High-voltage output
36	HVOUT2	High-voltage output

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	HVOUT3	High-voltage output
38	HVOUT4	High-voltage output
39	HVOUT5	High-voltage output
40	HVOUT6	High-voltage output
41	HVOUT7	High-voltage output
42	HVOUT8	High-voltage output
43	HVOUT9	High-voltage output
44	HVOUT10	High-voltage output

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT16	High-voltage output
2	HVOUT17	High-voltage output
3	HVOUT18	High-voltage output
4	HVOUT19	High-voltage output
5	HVOUT20	High-voltage output
6	HVOUT21	High-voltage output
7	HVOUT22	High-voltage output
8	HVOUT23	High-voltage output
9	HVOUT24	High-voltage output
10	HVOUT25	High-voltage output
11	HVOUT26	High-voltage output
12	HVOUT27	High-voltage output
13	HVOUT28	High-voltage output
14	HVOUT29	High-voltage output
15	HVOUT30	High-voltage output
16	HVOUT31	High-voltage output
17	HVOUT32	High-voltage output
18	DATA OUT	Data output pin
19	GND	Supply ground
20	NC	No connection
21	$\overline{BL}$	Blanking pin
22	POL	Polarity pin
23	LE	Latch enable pin
24	VDD	Logic supply voltage
25	CLK	Clock pin
26	DIR	Direction pin
27	DATA IN	Data input pin
28	VPP	High-voltage power supply

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
29	BPOUT	Black plane output
30	HVOUT1	High-voltage output
31	HVOUT2	High-voltage output
32	HVOUT3	High-voltage output
33	HVOUT4	High-voltage output
34	HVOUT5	High-voltage output
35	HVOUT6	High-voltage output
36	HVOUT7	High-voltage output
37	HVOUT8	High-voltage output
38	HVOUT9	High-voltage output
39	HVOUT10	High-voltage output
40	HVOUT11	High-voltage output
41	HVOUT12	High-voltage output
42	HVOUT13	High-voltage output
43	HVOUT14	High-voltage output
44	HVOUT15	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV66.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove $V_{PP.}$ (**Note 1**)
2	Apply $V_{DD.}$	2	Remove all inputs.
3	Set all inputs (Data, CLK, EN, etc.) to a known state.	3	Remove $V_{DD.}$
4	Apply $V_{PP.}$ (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} during operation.

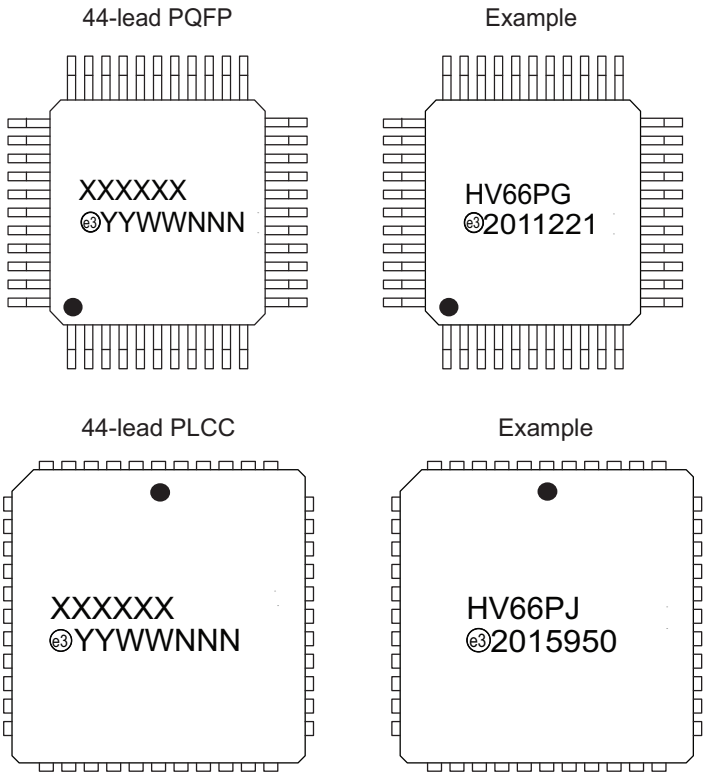
TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs			
	Data	CLK	LE	$\overline{BL}$	POL	DIR	Shift Register 1 2...32	High-voltage Output 1 2...32	Data Out *	BP_{OUT}
Load S/R, R/L Shift	L or H	↑	L	Ignore	Ignore	H	Data → Q_1... → Q_{32}	Ignore	Q_{32}	Ignore
	L or H	↑	L	Ignore	Ignore	L	Q_1←...Q_{32} ← Data	Ignore	Q_1	Ignore
Load Latches	X	H or L	H	H	H	X	*...*	$\overline{*...*}$	No Change	H
	X	H or L	H	H	L	X	*...*	*...*	No Change	L
Transparent Mode	L or H	↑	H	H	H	H	Data → Q_1... → Q_{32}	$\overline{*...*}$	Q_{32}	H
	L or H	↑	H	H	L	H	Data → Q_1... → Q_{32}	*...*	Q_{32}	L
	L or H	↑	H	H	H	L	Q_1←...Q_{32} ← Data	$\overline{*...*}$	Q_1	H
	L or H	↑	H	H	L	L	Q_1←...Q_{32} ← Data	*...*	Q_1	L
Blank Control	X	X	X	L	L	X	X	L...L	Ignore	L
	X	X	X	L	H	X	X	H...H	Ignore	H

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
Ignore = The state of the specific input or output is irrelevant to demonstrate the occurred event.
↑ = Low-to-high transition
* = Dependent on the previous stage's state before the last CLK or last LE high

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

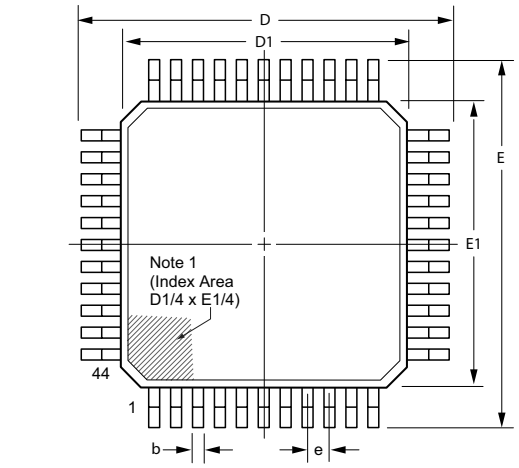


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

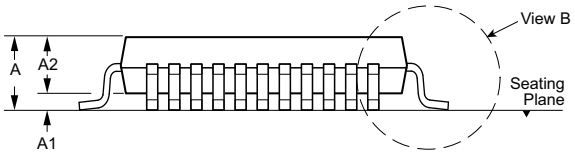
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PQFP Package Outline (PG)

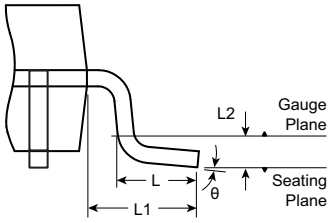
10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Top View



Side View



View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

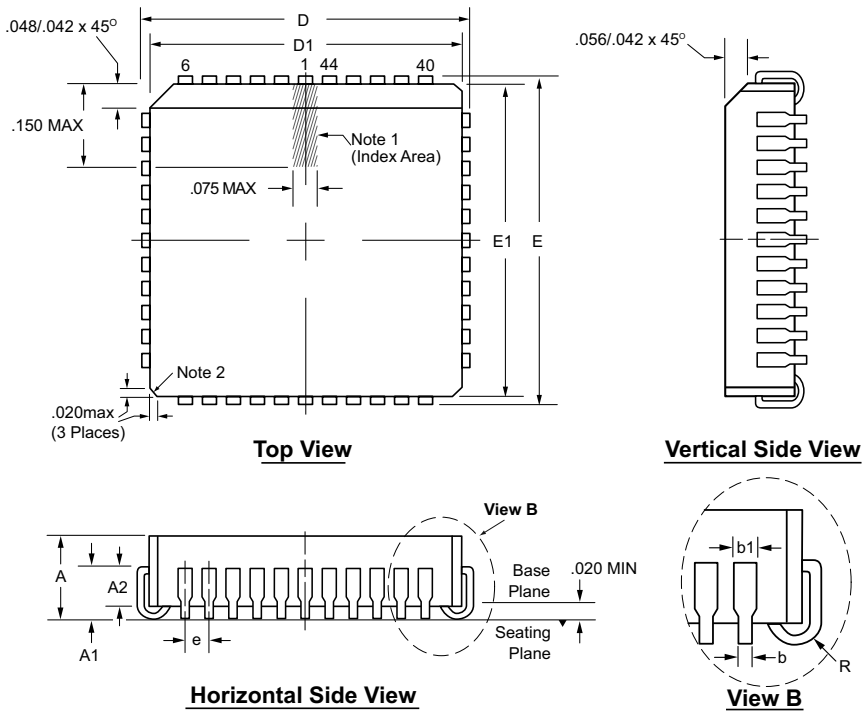
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Supertex Doc # DSFP-HV66 to Microchip DS20005886A
- Removed “HVCMOS® Technology” from the Features section
- Changed the package marking format
- Updated the 44-lead PQFP PG M919 and 44-lead PLCC PJ M903 media types
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV66	=	32-Channel LCD Driver with Separate Backplane Output
Packages:	PG	=	44-lead PQFP
	PJ	=	44-lead PLCC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	96/Tray for a PG Package
	(blank)	=	27/Tube for a PJ Package

Examples:

a) HV66PG-G: 32-Channel LCD Driver with Separate Backplane Output, 44-lead PQFP, 96/Tray

b) HV66PJ-G: 32-Channel LCD Driver with Separate Backplane Output, 44-lead PLCC, 27/Tube

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