Low Dropout, 400mA Adjustable Linear Regulator

General Description

The RT9053A is a high performance, 400mA LDO regulator and ultra low dropout. The quiescent current is as low as 42μA, further prolonging the battery life. The RT9053A also works with low ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in handheld wireless devices.

The RT9053A consumes typically 0.7μA in shutdown mode. The other features include low dropout voltage, high output accuracy, and current limiting protection. The RT9053A is available in SOT-23-5 and WDFN-6L 2x2 packages.

Ordering Information

RT9053A□□

- Package Type
  - B : SOT-23-5
  - QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free) (for WDFN-6L 2x2 Only)

Note :

Richtek roducts are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

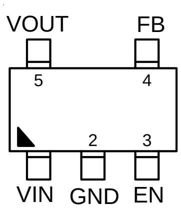
- **Adjustable Output Voltage Down to 0.8V**
- **Wide Operating Voltage Ranges : 2.2V to 5.5V**
- **Low Dropout : 230mV at 400mA**
- **Ultra Fast Response in Line/Load Transient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **Output Only 1μF Capacitor Required for Stability**
- **RoHS Compliant and Halogen Free**

Applications

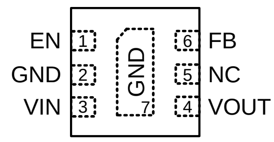
- Mega Sim Card
- CDMA/GSM Cellular Handsets
- Portable Information Appliances
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Mini PCI& PCI-Express Cards
- PCMCIA & New Cards

Pin Configurations

(TOP VIEW)



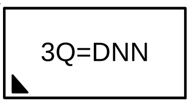
SOT-23-5



WDFN-6L 2x2

Marking Information

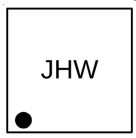
RT9053AGB



3Q= : Product Code

DNN : Date Code

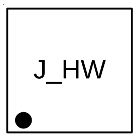
RT9053AGQW



JH : Product Code

W : Date Code

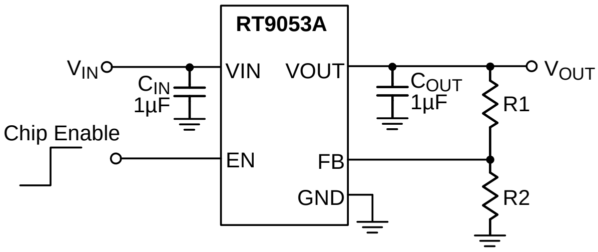
RT9053AZQW



J_H : Product Code

W : Date Code

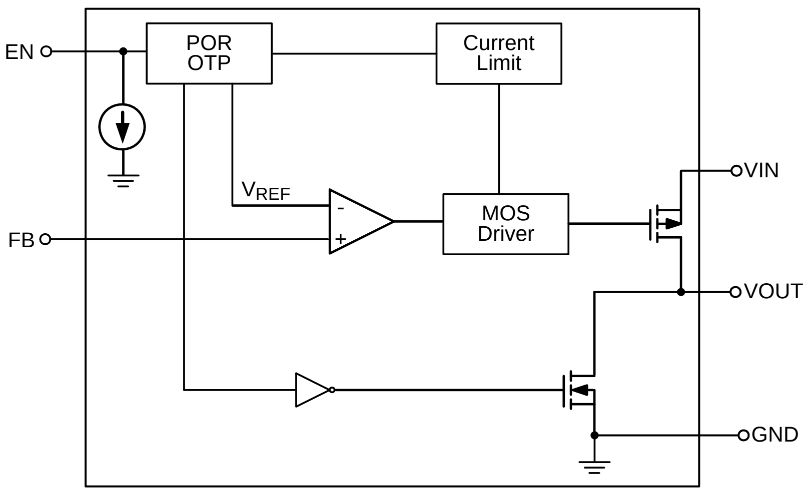
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-5	WDFN-6L 2x2		
1	3	VIN	Supply Input.
2	2, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	1	EN	Chip Enable (Active High). When the EN goes to a logic low, the device will be shutdown mode.
4	6	FB	Output Voltage Feedback.
5	4	VOUT	Regulator Output.
--	5	NC	No Internal Connection.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ------ 6V
- EN Input Voltage ------ 6V
- Power Dissipation, P_D @ T_A = 25°C (Note 2)
  SOT-23-5 ------ 0.4W
  WDFN-6L 2x2 ------ 0.606W
- Package Thermal Resistance
  SOT-23-5, θ_{JA} ------ 250°C/W
  WDFN-6L 2x2, θ_{JA} ------ 165°C/W
  WDFN-6L 2x2, θ_{JC} ------ 8.2°C/W
- Lead Temperature (Soldering 10sec.) ------ 260°C
- Junction Temperature ------ 150°C
- Storage Temperature Range ------ –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ------ 2kV
  MM (Machine Model) ------ 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ------ 2.2V to 5.5V
- Junction Temperature Range ------ –40°C to 125°C
- Ambient Temperature Range ------ –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.7V, C_{IN} = C_{OUT} = 1µF, I_{OUT} = 20mA, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
FB Reference Voltage		V_{FB}		0.792	0.8	0.808	V
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 10mA	–1	0	1	%
Quiescent Current		I_Q	I_{OUT} = 0mA	--	35	50	µA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	0.7	1.5	µA
Current Limit		I_{LIM}	R_{LOAD} = 0Ω, 2.2V ≤ V_{IN} < 5.5V	400	650	1000	mA
Dropout Voltage		V_{DROP}	I_{OUT} = 400mA	--	230	350	mV
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 400mA 2.2V ≤ V_{IN} < 5.5V	--	--	1	%
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{OUT} = 1mA	--	0. 01	0.2	%/V
EN Threshold Voltage	Logic-High	V_{IH}		1.6	--	5.5	V
	Logic-Low	V_{IL}		0	--	0.6	
Enable Pin Current		I_{EN}		--	1	2	µA
FB Pin Current		I_{FB}		--	0.1	1	µA
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Rejection Rate	PSRR	f = 1kHz, I_{OUT} = 10mA	--	–56	--	dB
		f = 10kHz, I_{OUT} = 10mA	--	–35	--	
Output Noise Voltage	VON	V_{OUT} = 1.5V, C_{OUT} = 1μF, I_{OUT} = 0mA	--	30	--	μV_{RMS}

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

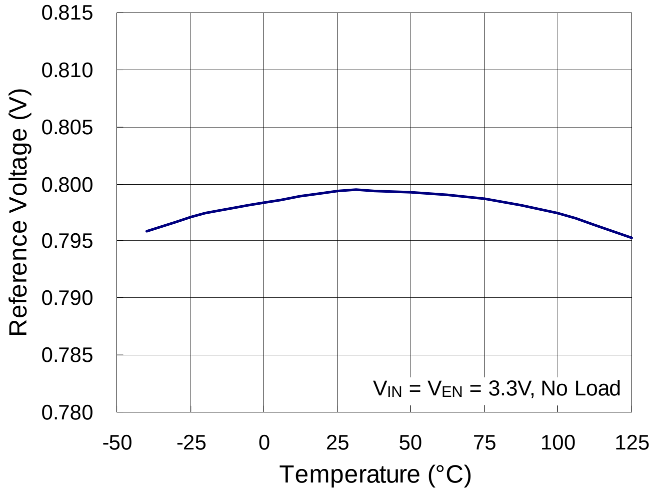
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

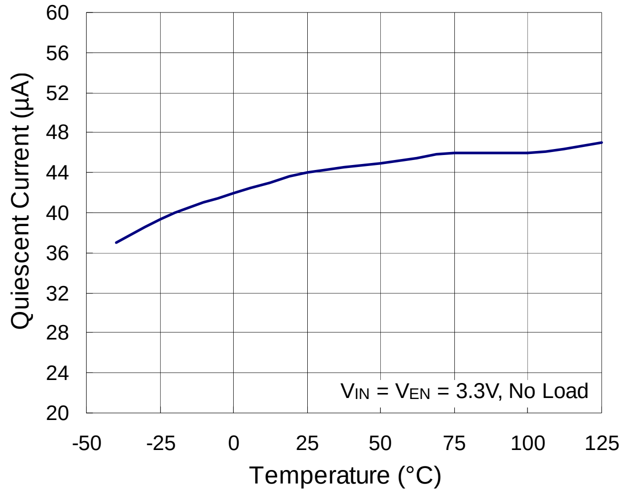
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

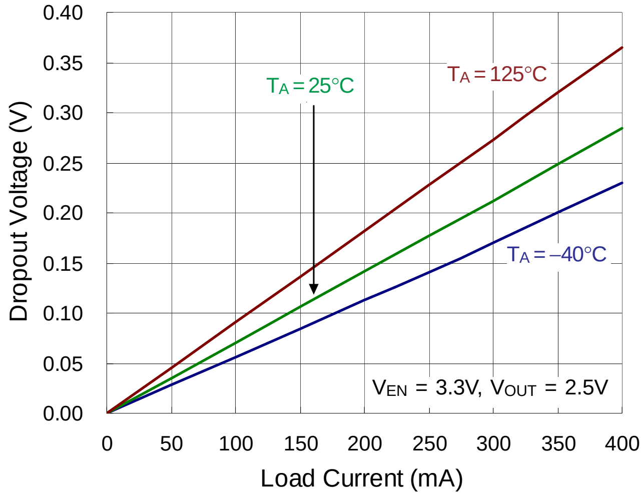
Reference Voltage vs. Temperature



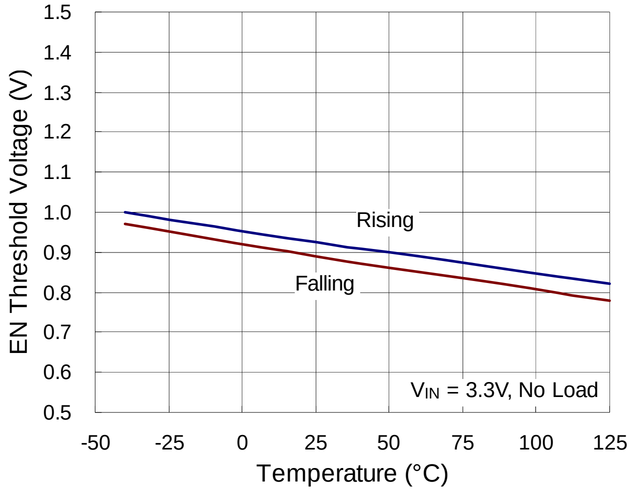
Quiescent Current vs. Temperature



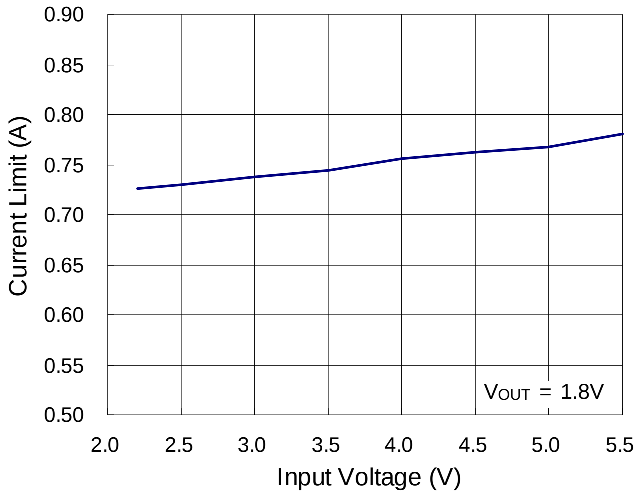
Dropout Voltage vs. Load Current



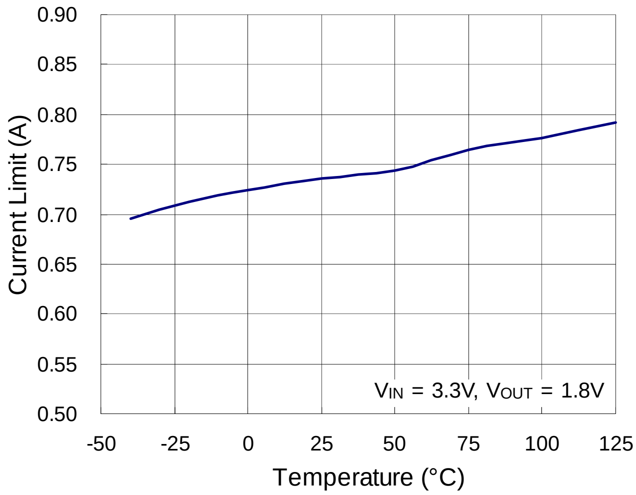
EN Threshold Voltage vs. Temperature



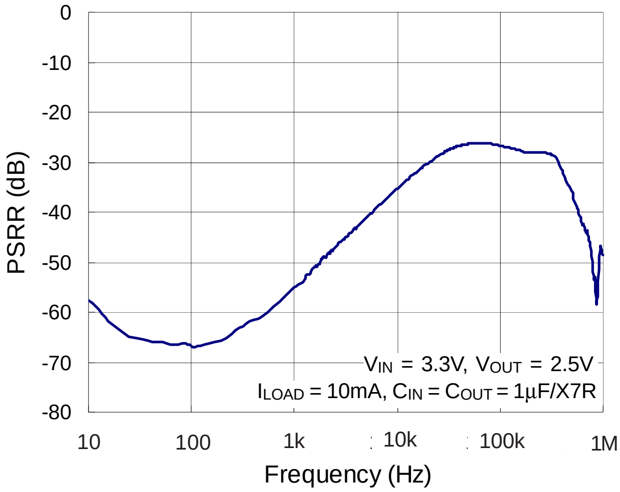
Current Limit vs. Input Voltage



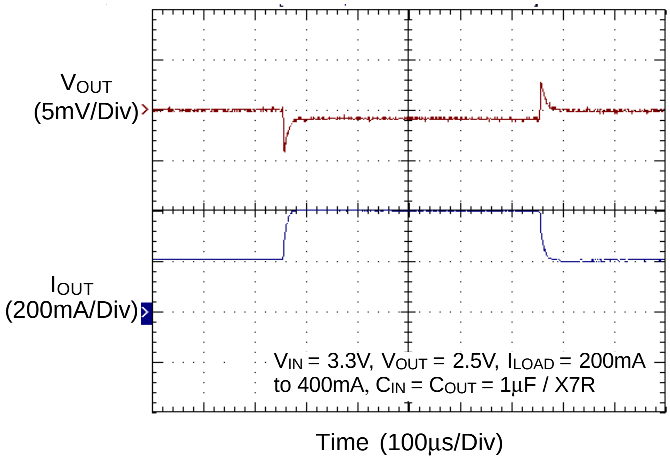
Current Limit vs. Temperature



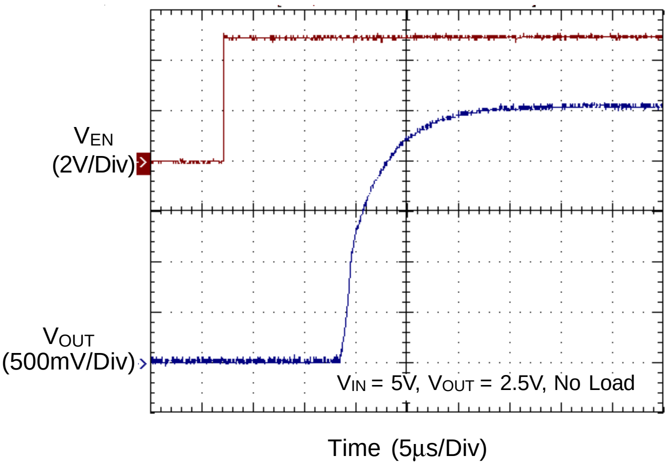
PSRR vs. Frequency



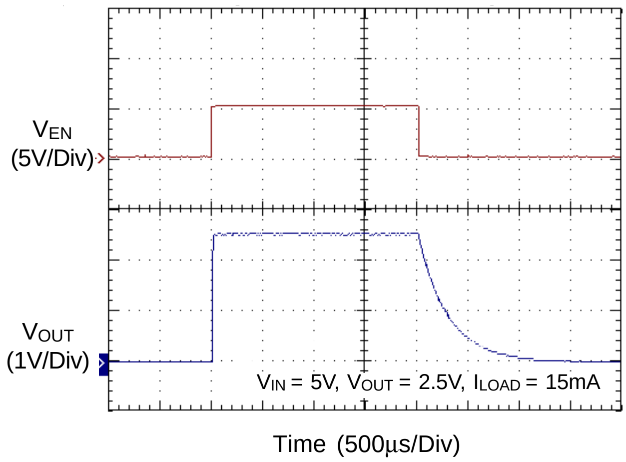
Load Transient Response



Power On from EN



Enable/Shutdown Response



Application Information

Input Capacitor Selection

Like any low dropout linear regulator, the external capacitors used with the RT9053A must be carefully selected for stability and performance. The input capacitance is recommended to be at least 1μF, and can be increased without limit. The input capacitor must be located at a distance of less than 0.5 inch from the input pin of the IC and returned to a clean ground plane. Any high-quality ceramic capacitor or tantalum capacitor can be used for the input capacitor. Using input capacitor with larger capacitance and lower ESR (Equivalent Series Resistance) can obtain better PSRR and line transient response.

Output Capacitor Selection

The RT9053A is designed specifically to work with low ESR ceramic output capacitor to save board space and have better performance. The output capacitor is recommended to be at least 1μF. Larger capacitance can reduce noise and improve load transient response, stability and PSRR. The RT9053A can operate with other types of output capacitor due to its wide stable operation range. The output capacitor should be placed less than 0.5 inch from the VOUT pin and returned to a clean ground plane.

Output Voltage Setting

The output voltage divider R1 and R2 allows adjustment of the output voltage for various application as shown in Figure 1.

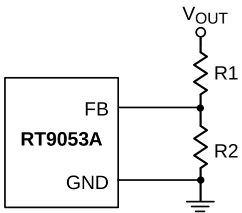


Figure 1. Output Voltage Setting

The output voltage is set according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.8V typical).

Enable Function

The RT9053A features enable/shutdown function. The voltage at the EN pin determines the enable/shutdown state of the regulator. To ensure the regulator will switch on, the enable control voltage must be greater than 1.6V. The regulator will enter shutdown mode when the voltage at the EN pin falls below 0.6V. If the enable function is not needed, the EN pin should be pulled high or simply tied to V_{IN} to keep the regulator in an on state.

PSRR

RT9053A features high Power Supply Rejection Ratio (PSRR), which is defined as the ratio of output voltage change against input voltage change.

$$PSRR = 20 \times \log\left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)$$

A low dropout regulator with a higher PSRR can provide better line transient performance.

Current Limit

The RT9053A implements an independent current limit circuit, which monitors and controls the pass element's gate voltage to limit the output current at 650mA (typ.). If the current limit condition lasts for a long time, the regulator temperature may increase high enough to damage the regulator itself. Therefore, the RT9053A implements current limit function and thermal protection function to prevent the regulator from damage when the output is shorted to ground.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9053A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. For SOT-23-5 packages, the thermal resistance, θ_{JA}, is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for WDFN-6L 2X2 package

$P_{D(MAX)}$ = (125°C − 25°C) / (250°C/W) = 0.400W for SOT-23-5 package

The thermal resistance θ_{JA} is determined by the package architecture design and the PCB layout design. However, the package architecture design had been already designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of WDFN series package.

As shown in Figure 2, we can find the relation between the copper area and the thermal resistance θ_{JA}. The thermal resistance will be reduced by adding more copper area. When IC mounted to the standard footprint, the thermal resistance θ_{JA} is 165°C/W. Adding copper area of pad to 15mm^2 under the package reduces the θ_{JA} to 150°C/W. Even further, increasing the copper area of pad to 70mm^2 reduces the θ_{JA} to 130°C/W.

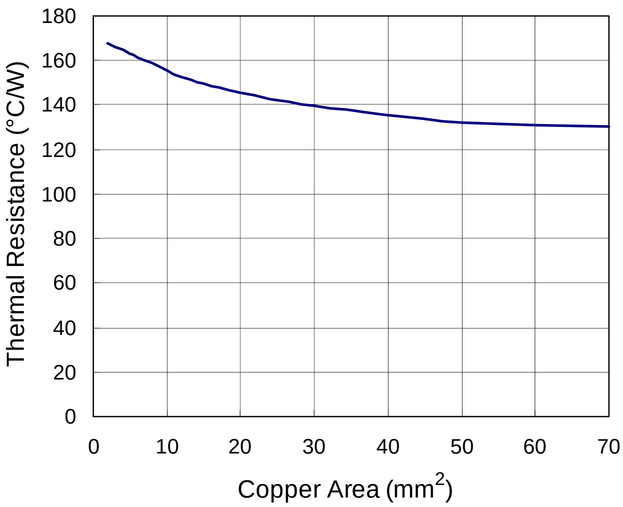


Figure 2. WDFN-6L 2x2 Thermal Resistance θ_{JA} vs. PCB Copper Area

As shown in Figure 3, we can also find the WDFN-6L 2x2 maximum power dissipation improvement by different copper area design at ambient temperature T_A = 25°C operation.

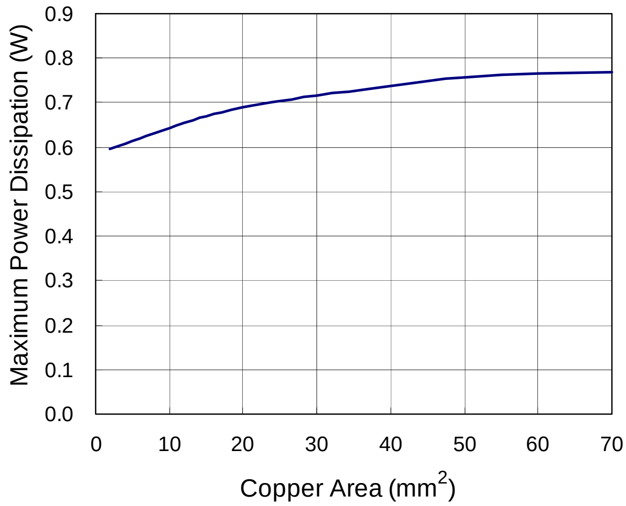


Figure 3. Maximum Power Dissipation P_D vs. PCB Copper Area

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9053A packages, the derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

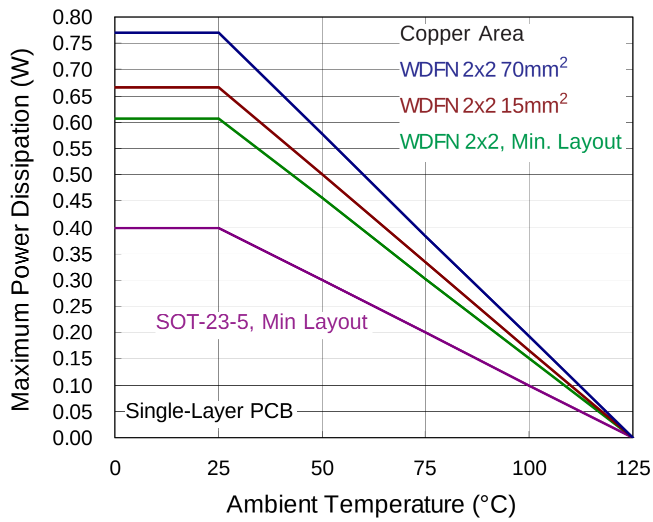
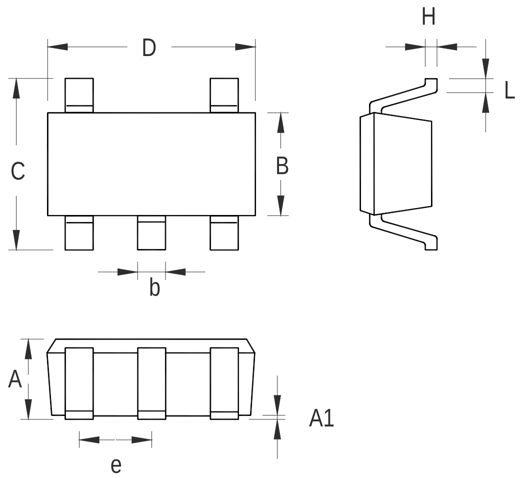


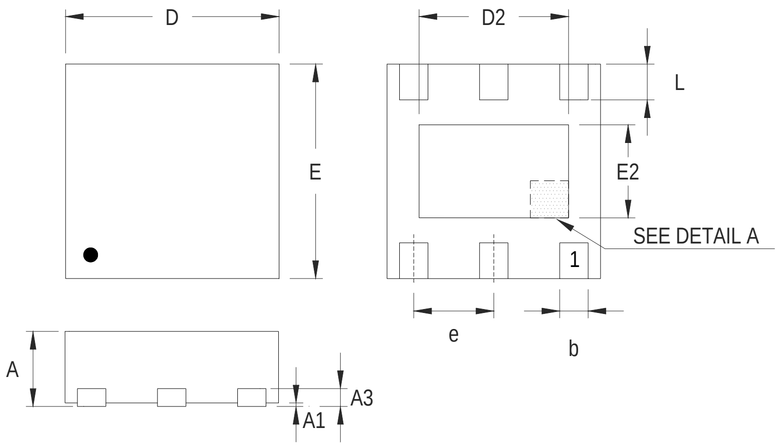
Figure 4. Derating Curves for RT9053A Packages

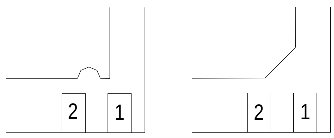
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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