TECHNICAL NOTE

System Power Supply LSIs for use in automotive electronics

Power Supply for system With built-in for system Communication functions

BD9401FM/BD9403FV

●Description

The BD9401FM/BD9403FV can be combined with the BD9400BFP to create application-specific, system power supplies. The BD9401FM features 3 built-in channels: a 1 A LDO channel, a switching regulator controller channel, and a 500 mA high-side switch channel. The BD9403FV features one built-in switching regulator controller channel. The combination of a switching regulator with an LDO enables the IC to deliver reduced voltage consumption.

●Features

1. The IC can be combined with the BD9400BFP, providing design flexibility.
2. Broad input voltage range: 7 V to 36 V
3. Built-in 1 A variable LDO (BD9401FM)
4. Output voltage accuracy of ± 2% (BD9401FM LDO)
5. Built-in 500 mA high-side switch (BD9401FM)
6. Built-in open collector type PWM controller channel for design flexibility
7. Maximum frequency: 500 kHz
8. Built-in short protection circuit (SCP)
9. Built-in thermal shutdown circuit
10. HSOP-M28/SSOP-B14 package

●Applications

Car audio, satellite navigation systems, etc.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage 1	VCC	36*1	V
Power supply voltage 2	VLDOVcc	12*1	V
Power supply voltage 3	VREG, VREF	7	V
PWM output current	IoMAX	100	mA
Power dissipation 1 (HSOPM28)	P_{01}	1.8*2	W
Power dissipation 2 (HSOPM28)	P_{02}	2.2*3	W
Power dissipation 3 (SSOPB14)	P_{03}	0.35*4	W
Power dissipation 4 (SSOPB14)	P_{04}	0.4*5	W
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STG}	+150	°C
Maximum junction temperature	T_{JMAX}	+150	°C

*1 Not to exceed Pd.

*2 Reduced by 14.4 mW/°C over 25°C during IC without heat sink operation.

*3 Reduced by 17.6 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

*4 Reduced by 2.8 mW/°C over 25°C during IC without heat sink operation.

*5 Reduced by 3.2 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●**Recommended operating ranges** (Ta = 25°C) (Not to exceed Pd.)

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage 1	VCC	8	26	V
Power supply voltage 2	VLDOVcc	3	11	V
Oscillating frequency	FOSC	30	500	KHz

●**Electrical characteristics** 1:BD9401FM (Unless otherwise specified, Ta = 25°C; V_{CC} = 13.5 V; VREF = 3.0 V; VREG = 5.0 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Total supply current]						
Total supply current VCC	I_{CC}	—	200	400	μA	PWMCTL = HSDCTL = 2 V, Io = 0 mA
Total supply current VREG	I_{VREG}	—	0.68	—	mA	VREG = 5.0 V
Total supply current VREF	I_{VREF}	—	0.96	—	mA	VREF = 3.0 V
Total supply current during standby operation	I_{STBY}	—	1	10	μA	VREF = VREG = PWMCTL = HSDCTL = 0 V
[Variable LDO regulator: 1 A]						
Output voltage		—	3.3	—	V	Io = 10 mA
NF voltage	V_{NF}	1.225	1.250	1.275	V	
Output maximum current	I_{PEAK}	1.0	—	—	A	
Line regulation	ΔV_{OLI}	—	10	20	mV	VLDOVcc = 5 V to 11 V
Load regulation	ΔV_{OLO}	—	50	100	mV	Io = 0 mA to 800 mA
Minimum I/O voltage difference	ΔV_{OLDO}	—	0.5	1.0	V	Io = 800 mA
Ripple rejection	R.R.	50	60	—	dB	Io = 10 mA, V_{IN} = 0.1 Vp.p
[High-side switch: 500 mA]						
Dropout voltage	V_{DH}	—	0.5	1.0	V	Io = 500 mA
Output maximum current	I_{PEAKH}	0.5	—	—	A	
[High-side switch control pin]						
Off voltage input range	V_{HSDOFF}	0	—	1.0	V	
On voltage input range	V_{HSDON}	2.0	—	VREF	V	
[Error amp]						
INV pin threshold voltage	VI_{NV}	1.225	1.250	1.275	V	VFB = 3.0 V
INV pin input current	I_{BIAS}	-1	—	1	uA	V_{INV} = 0 V
DC voltage gain	A_V	—	60	—	dB	
Max. output voltage	V_{FBM}	2.0	2.4	2.8	V	V_{INV} = 2.0 V
Min. output voltage	V_{FBL}	—	—	0.1	V	V_{INV} = 2.0 V
Output sinking current	I_{FBSI}	1	2.5	4	mA	V_{FB} = 3 V, V_{INV} = 0 V
Output source current	I_{FBSO}	50	100	200	uA	V_{FB} = 0 V, V_{INV} = 2 V
[PWM comparator]						
0% duty cycle	V_{TH0D}	0.90	1.00	1.10	V	FB voltage, OSCIN = 1.0 V
100% duty cycle	V_{TH100D}	1.80	2.00	2.20	V	FB voltage, OSCIN = 2.0 V
[Short protection circuit (SCP)]						
INV pin short detection voltage	V_{SINV}	0.8	0.9	1.0	V	INV voltage
Voltage when SCP is off	V_{SSCP}	—	50	100	mV	SCP voltage
Threshold voltage 1	V_{T1SCP}	0.85	1.05	1.2	V	SCP voltage, SCD, OUT: HIGH
Threshold voltage 2	V_{T2SCP}	1.80	2.00	2.2	V	SCP voltage, PWM: OFF
SCP pin source current	I_{SCP}	1.5	2.5	4.0	μA	V_{SCP} = 0 V
[Undervoltage protection circuit (UVLO)]						
Threshold voltage	V_{UVLO}	—	5.70	—	V	Vcc = 13.5 V→5 V
Hysteresis voltage	V_{HYS}	—	0.07	—	V	Vcc = 5 V→13.5 V ΔV_{UVLO}

●**Electrical Characteristics** 2:BD9401FM (Unless otherwise specified, Ta = 25°C, Vcc = 13.5 V, STDY = 3.3 V, VREF = 3.0 V, VREG = 5.0 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[PWM driver output block]						
Output saturation voltage	V_{SAT}	—	0.8	1.4	V	Io = 75 mA, V_{FB} = 3.0 V
Output current when DWM is off	V_{DOFF}	—	—	10	uA	V_{PWMOUT} = 30 V, V_{PNMCTL} = 0 V
[Switching regulator control pin]						
Off voltage input range	V_{PNMOFF}	0	—	1.0	V	
On voltage input range	V_{PWMON}	2.0	—	VREF	V	
[SCD (short protection detection) signal output pin]						
SCD low output voltage	V_{SCPL}	0.0	—	1.0	V	V_{SCP} = 0 V
SCD high output voltage	V_{SCOH}	2.0	—	VREF	V	V_{SCP} = 2 V

●**Electrical Characteristics** 3:BD9403FV (Unless otherwise specified, Ta = 25°C, Vcc = 13.5 V, STDY = 3.3 V, VREF = 3.0 V, VREG = 5.0 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Total supply current]						
Total supply current VCC	I_{CC}	—	200	400	μA	Io = 10 mA
Total supply current VREG	I_{VREG}	—	0.68	—	mA	VREG = 5.0 V
Total supply current VREF	I_{VREF}	—	0.96	—	mA	VREF = 3.0 V
Total supply current during standby operation	I_{STBY}	—	1	10	μA	VREF = VREG = PWMCTL = 0 V
[Error amp]						
INV pin threshold voltage	VI_{NV}	1.225	1.250	1.275	V	VFB = 3.0 V
INV pin input current	I_{BIAS}	-1	—	1	uA	V_{INV} = 0 V
DC voltage gain	A_V	—	60	—	dB	
Maximum output voltage	V_{FBM}	2.0	2.4	2.8	V	V_{INV} = 2.0 V
Minimum output voltage	V_{FBL}	—	—	0.1	V	V_{INV} = 2.0 V
Output sinking current	I_{FBSI}	1	2.5	4	mA	V_{FB} = 3 V, V_{INV} = 0 V
Output source current	I_{FBSO}	50	100	200	uA	V_{FB} = 0 V, V_{INV} = 2 V
[PWM comparator]						
0% duty cycle	V_{TH0D}	0.90	1.00	1.10	V	FB voltage, OSCIN = 1.0 V
100% duty cycle	V_{TH100D}	1.80	2.00	2.20	V	FB voltage, OSCIN = 2.0 V
[Short protection circuit (SCP)]						
INV pin short detection voltage	V_{SINV}	0.8	0.9	1.0	V	INV voltage
Voltage when SCP is off	V_{SSCP}	—	50	100	mV	SCP voltage
Threshold voltage 1	V_{T1SCP}	0.85	1.05	1.2	V	SCP voltage, SCD, OUT: HIGH
Threshold voltage 2	V_{T2SCP}	1.80	2.00	2.2	V	SCP voltage, PWM OFF
SCP pin source current	I_{SCP}	1.5	2.5	4.0	μA	V_{SCP} = 0 V
[Undervoltage protection circuit (UVLO)]						
Threshold voltage	V_{UVLO}	—	5.70	—	V	Vcc = 13.5 V→5 V
Hysteresis voltage	V_{HYS}	—	0.07	—	V	Vcc = 5 V→13.5 V ΔV_{dVLO}
[PWM driver output block]						
Output saturation voltage	V_{SAT}	—	1.0	2.0	V	Io = 75 mA
Output current when DWM is off	V_{OFF}	—	—	20	uA	V_{PWMOUT} = 30 V, V_{PWMCTL} = 0 V
[Switching regulator control pin]						
Off voltage input range	V_{PWMOFF}	0	—	1.0	V	
On voltage input range	V_{PWMON}	2.0	—	VREF	V	
[CD (short protection detection) signal output pin]						
SCD low output voltage	V_{SCDL}	0.0	—	1.0	V	V_{SCP} = 0 V
SCD high output voltage	V_{SCDH}	2.0	—	VREF	V	V_{SCP} = 2 V

●**Reference Data** (Unless otherwise specified, Ta = 25°C, Vcc = 13.5 V, V_{LDOVCC} = 5 V, V_{REF} = 3.0 V, V_{REG} = 5.0 V)

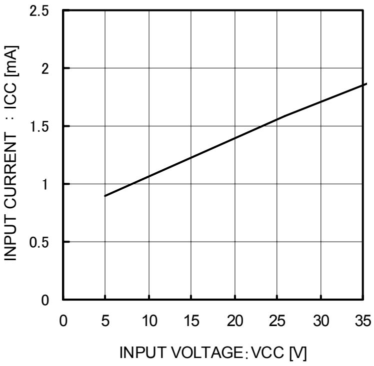


Fig.1 VCC Total Supply Current (BD9401FM)

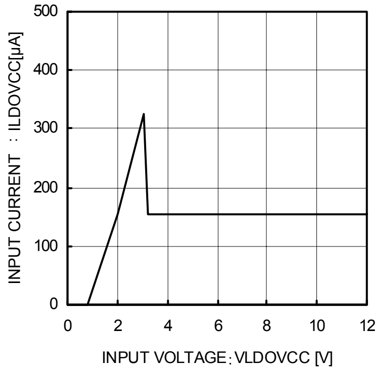


Fig.2 VLDOVcc Total Supply Current (BD9401FM)

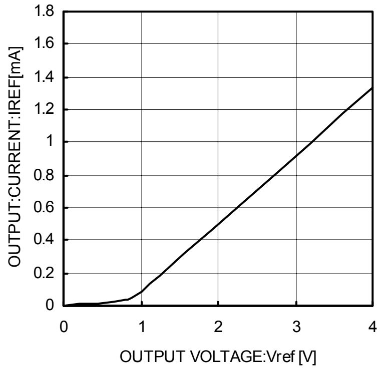


Fig.3 VREF Total Supply Current (BD9401FM)

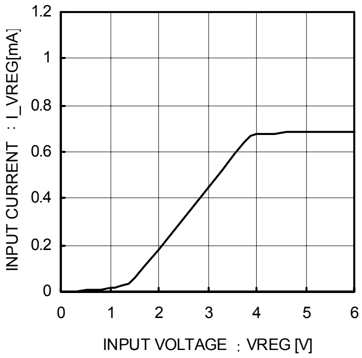


Fig.4 VREG Total Supply Current (BD9401FM)

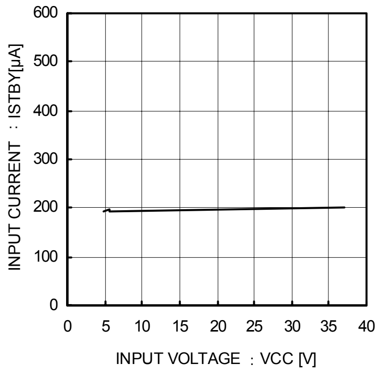


Fig.5 Total Supply Current When CTL Is Off (BD9401FM)

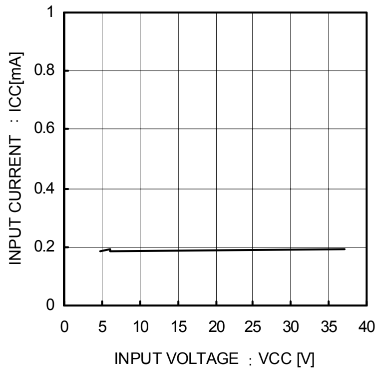


Fig.6 VCC Total Supply Current (BD9403FV)

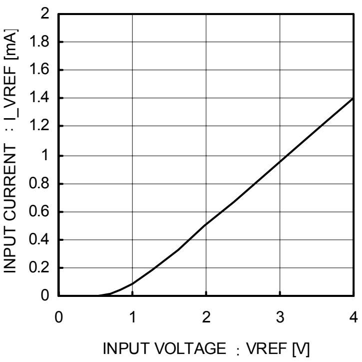


Fig.7 VREF Total Supply Current (BD9403FV)

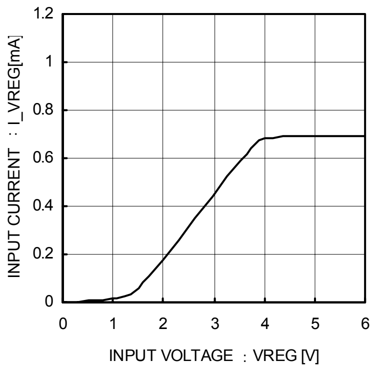


Fig.8 VREG Total Supply Current (BD9403FV)

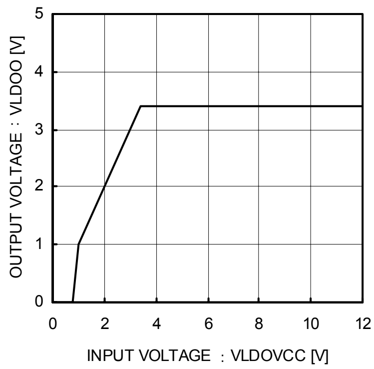


Fig.9 LDO Input Stability (1) (Io = 0 mA)

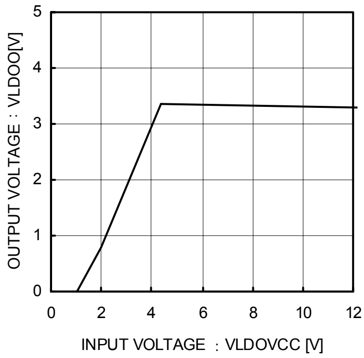


Fig.10 LDO Input Stability (2) (When V_{OUT} setting = 3.3 V; Io = 200 mA)

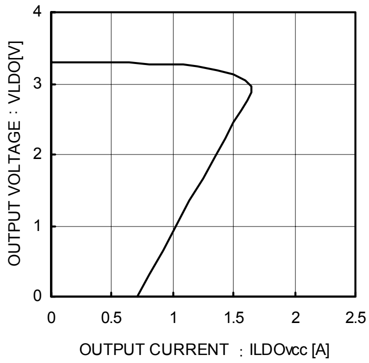


Fig.11 LDO Load Stability (When V_{OUT} setting = 3.3 V)

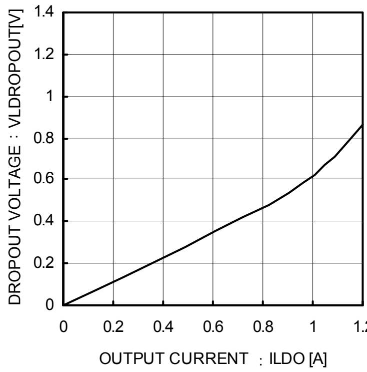


Fig.12 LDO I/O Voltage Differential

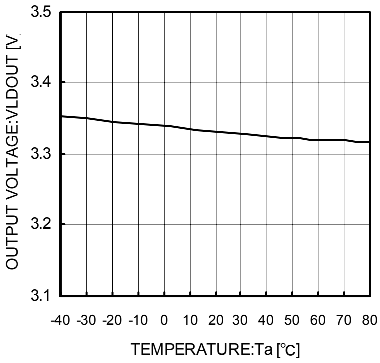


Fig.13 LDO Output Voltage vs Temperature

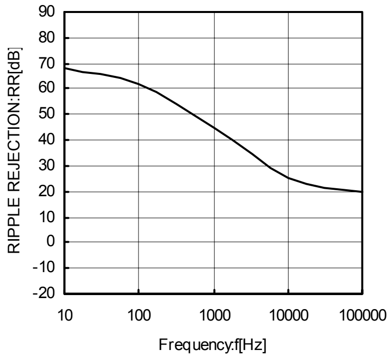


Fig.14 LDO Ripple Rejection

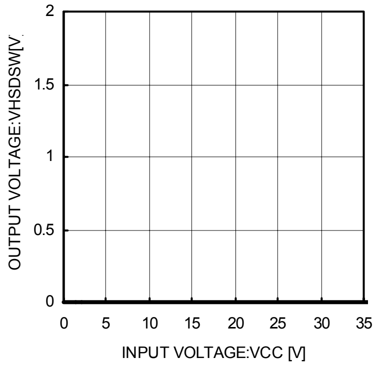


Fig.15 High-Side Switch Output When Off

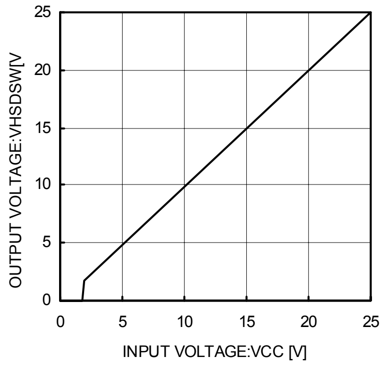


Fig.16 High-Side Switch I/O (Output Load: ∞)

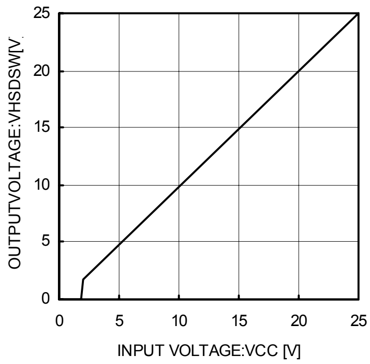


Fig.17 High-Side Switch I/O (Output Load: 50 Ω)

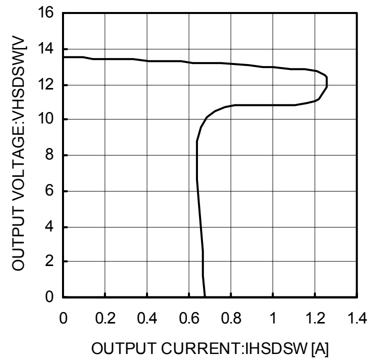


Fig.18 High-Side Switch Load Current

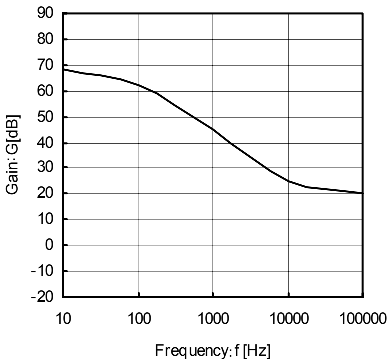


Fig.19 ERRAMP Frequency

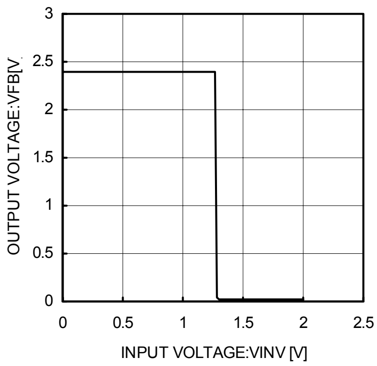


Fig.20 Error Amp I/O (VINV vs VFB)

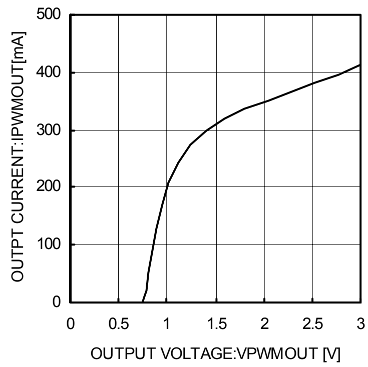


Fig.21 PWM Output Current

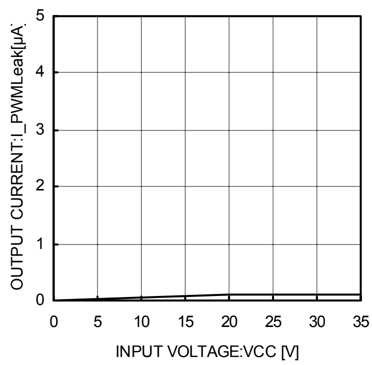


Fig.22 Leak When PWM Output Is Off

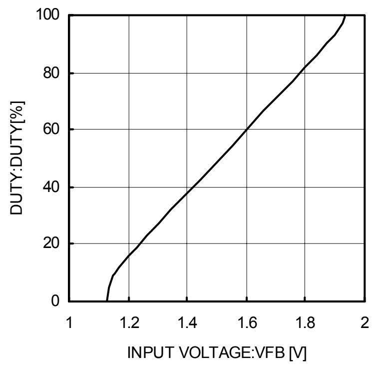


Fig.23 PWM Output FB vs Duty

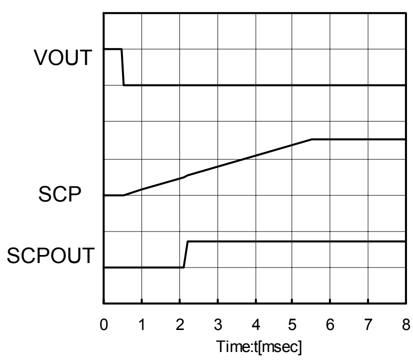


Fig.24 Short Protection Timer

●**Block Diagram** (BD9401FM)

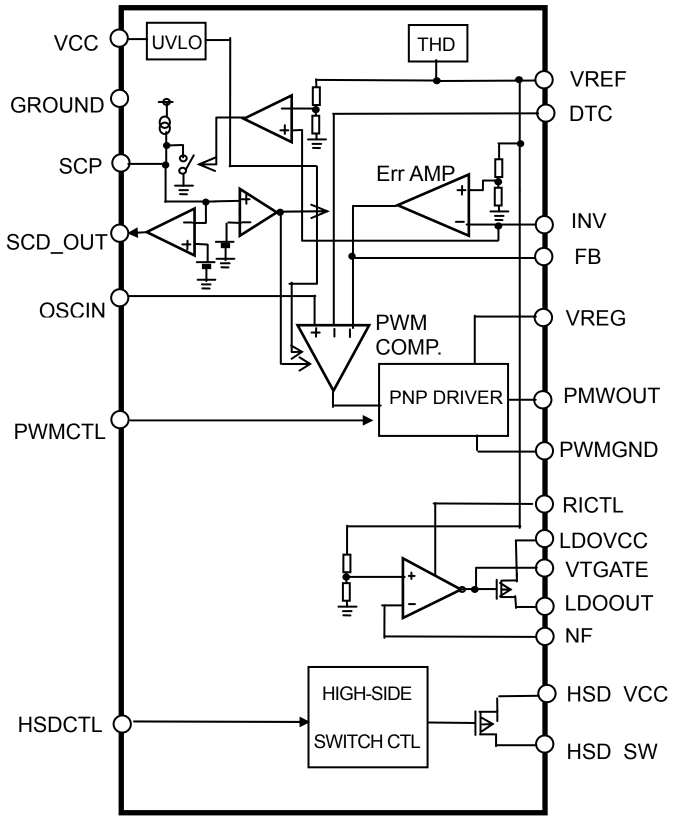


Fig.25 BD9401FM Block Diagram

●**Pin function descriptions** (BD9401FM)

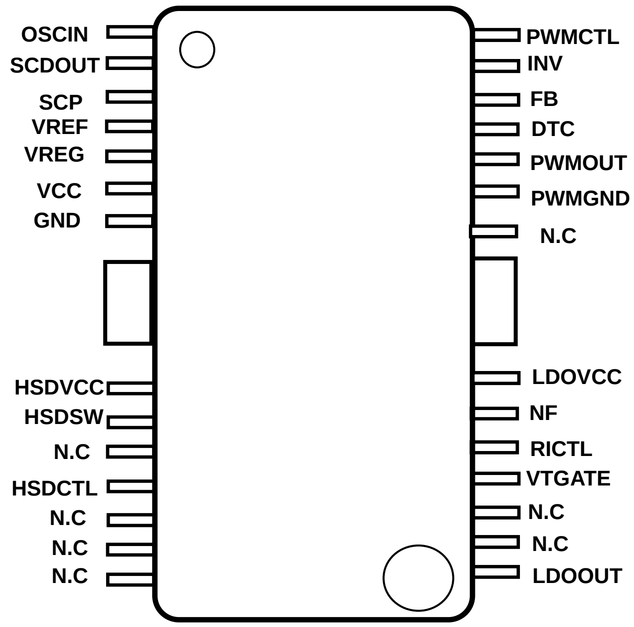


Fig.26 BD9401FM Pin Function Descriptions

●**Pin Descriptions** (BD9401FM)

Pin No.	Pin name	Function
1	OSCIN	Triangular waveform input pin
2	SCDOUT	Output short detection signal output pin (to BD9400BFP)
3	SCP	Output short detection delay time setting capacitor connection pin
4	VREF	Reference input VREF (3.0 V) input pin
5	VREG	Reference input VREF (5.0 V) input pin
6	VCC	Power supply input pin
7	GND	Ground pin
8	HSDVCC	High-side switch power supply input pin
9	HSDSW	High-side switch output pin
10	N.C.	NC pin
11	HSDCTL	High-side switch On/off control pin
12	N.C.	NC pin
13	N.C.	NC pin
14	N.C.	NC pin
15	LDOOUT	LDO regulator output pin
16	N.C.	NC pin
17	N.C.	NC pin
18	VTGATE	LDO regulator output PMOS gate pin
19	RICTL	LDO regulator overcurrent protection adjustment resistance connection pin (connect to GND when not using)
20	NF	LDO regulator output voltage setting resistance connection pin (reset input)
21	LDOVCC	LDO regulator power supply input pin
22	N.C.	NC pin
23	PWMGND	PWM ground
24	PWMOUT	PWM output pin
25	DTC	Dead time control pin
26	FB	Error amp output pin
27	INV	Error amp inverted input pin
28	PWMCTL	DC/DC control On/off switching pin
FIN	FIN	Heat dissipation fin; connect to ground.

●**Block Diagram** (BD9403FV)

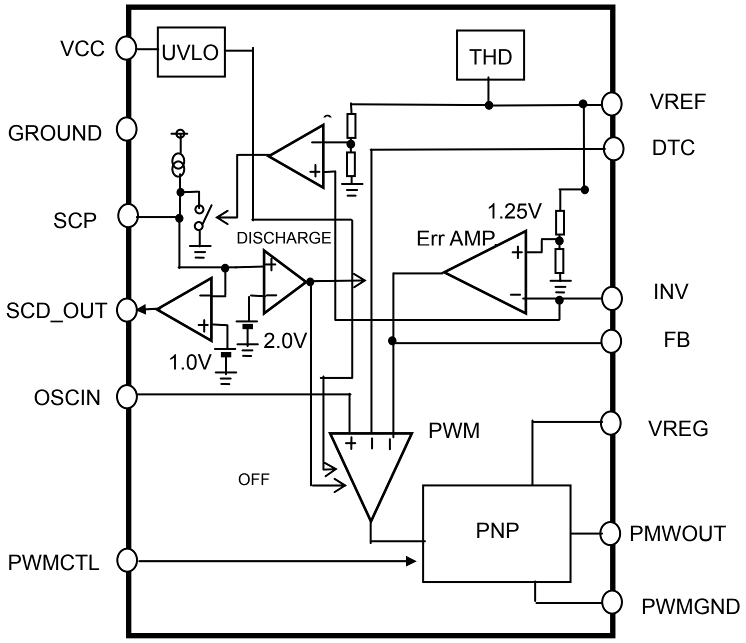


Fig.27 BD9403FV Block Diagram

●**Pin assignment diagram** (BD9403FV)

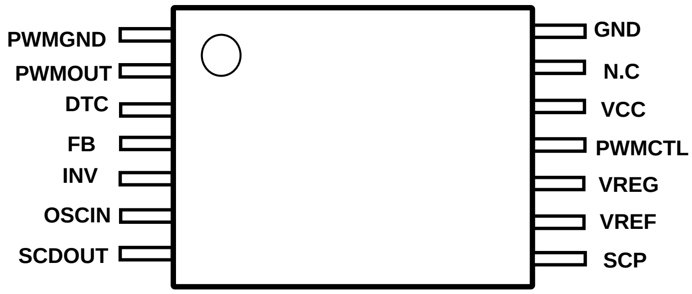


Fig.28 BD9403FV Pin Assignment Diagram

●**Pin function descriptions** (BD9403FV)

Pin No.	Pin name	Function
1	PWMGND	PWM ground
2	PWMOUT	PMW output pin
3	DTC	Dead time control pin
4	FB	Error amp output pin
5	INV	Error amp inverted input pin
6	OSCIN	Triangular waveform input pin
7	SCDOUT	Output short detection signal output pin (to BD9400BFP)
8	SCP	Output short detection delay time setting capacitor connection pin
9	VREF	Reference input VREF (3.0 V) input pin
10	VREG	Reference input VREF (5.0 V) input pin
11	PWMCTL	DC/DC control　On/off switching pin
12	VCC	Power supply input pin
13	N.C	NC pin
14	GND	Ground pin

●Application example

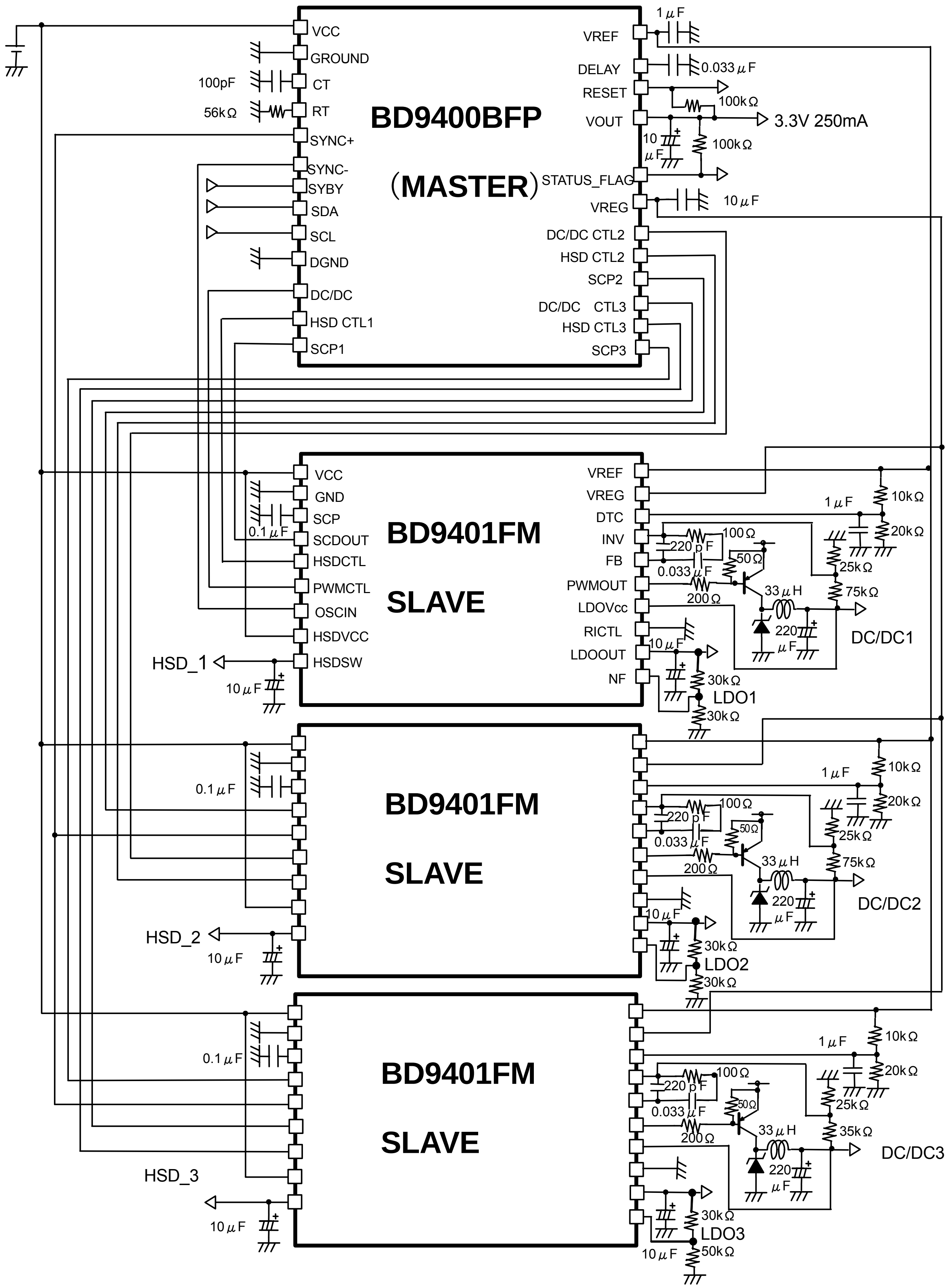


Fig.29 Application Example

●Block operation descriptions

•LDO block

The LDO block consists of an output-stage PMOS 1 A LDO with variable output voltage.
The feedback voltage pin carries 1.25 V at a precision of ± 2%. The input LDO voltage range is 3 V to 11 V. This range is independent of Vcc and assumes the connection of DC/DC output.

•High-side switch block

The high-side switch block consists of a high-side switch with a current capacity of 500 mA.
The HSD CTL pin provides on/off control.
The block incorporates a built-in overcurrent protection circuit.

•Error amp block

The error amp block connects the output feedback voltage to the INV pin. The reference voltage is connected internally to the inverted input pin. The switching duty is controlled with output feedback to control the output voltage. Phase compensation can be performed by connecting a capacitor or resistor between the INV and FB pins.

•PNM comparator

The triangular waveform from the BD9400BFP is input to the OSCIN pin. This triangular waveform and the FB voltage are used to output a switching pulse to create the duty. A capacitor can be connected to the DTC pin to set the Soft-start.

•PNP driver

The duty output by the PWM comparator drives the output NPN open collector. The PNP base current can be set by connecting a resistor to the PWM output.

•SCP block

The SCP block detects DC/DC converter output shorts and latches all output off after the set delay time elapses. The circuit is cleared by setting DC/DC CTL from low to high. Detection is performed using the INV pin, and the timer starts when the pin reaches 0.9 V. BD9401FM/BD9403FV short detection consists of 2 mode settings, with the short detection signal being output to SCD-OUT after 1/2 the timer latch delay time. The timer time can be set with the capacitor connected to the SCP pin.

•UVLO block

The IC incorporates a built-in UVLO (undervoltage lockout) circuit to prevent J output malfunctions, during periods of low Vcc input. When Vcc falls to 5.7 V or lower, this circuit operates and turns off PWM output. When Vcc rises above the 5.7 V hysteresis voltage (0.70 mA TYP), output is reset.

●**Timing chart** (DC/DC controller)

1) At startup

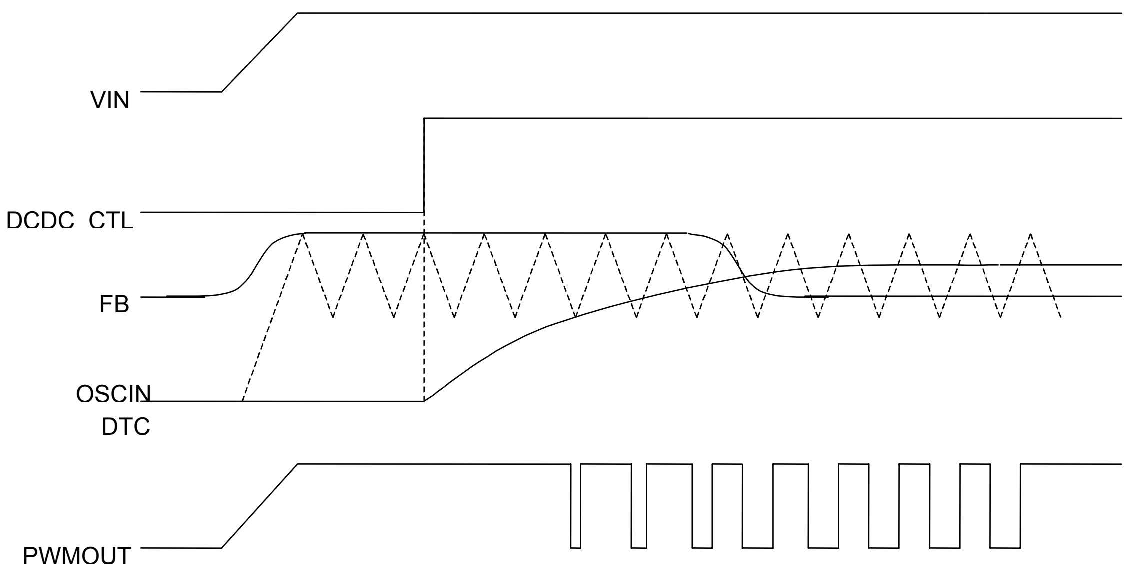


Fig.30 Timing Chart At Startup Time

2) During short protection

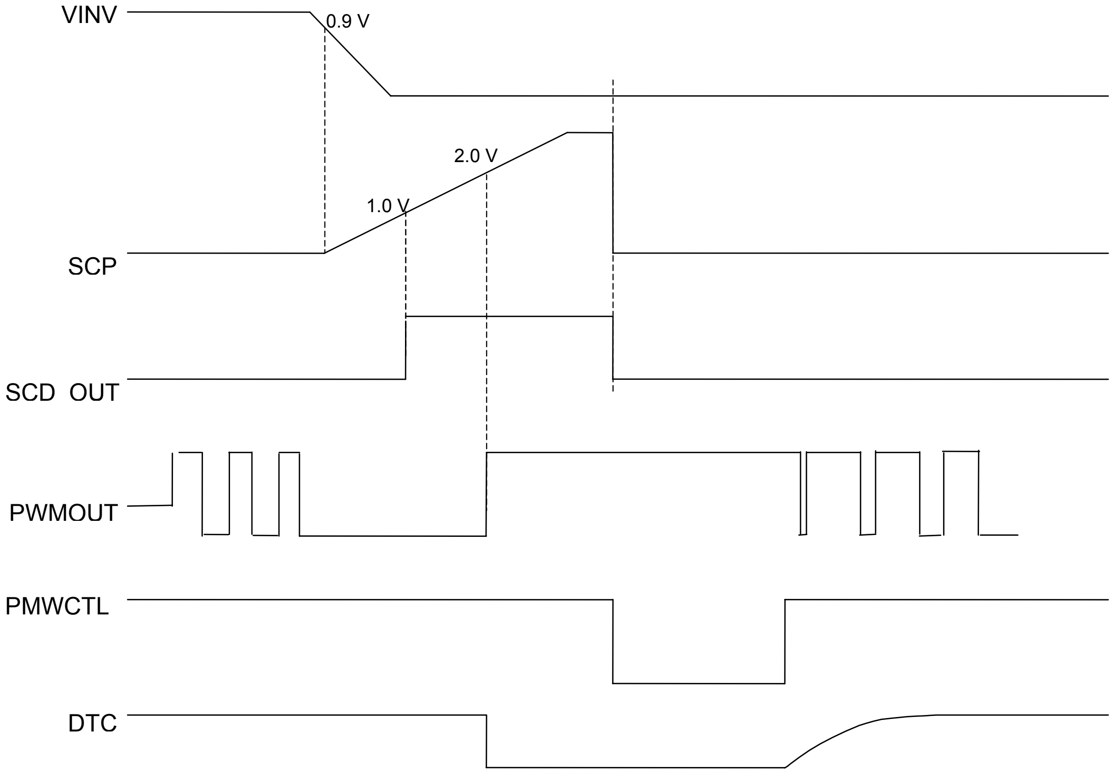
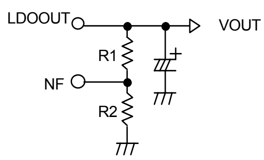
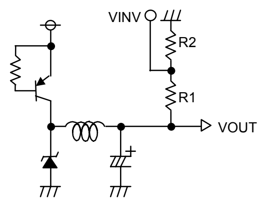
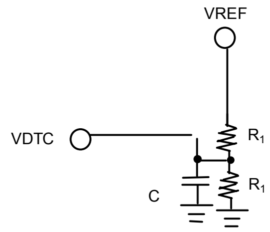
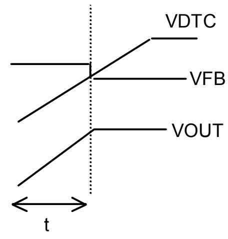
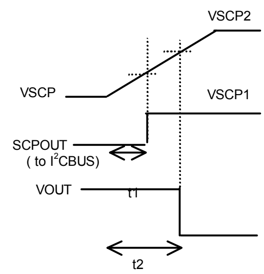


Fig.31 Timing Chart During Short Protection

●Selecting application components

Block name	Setting procedure	Calculation example	
LDO output voltage	$V_{OUT} = ((R1 + R2)/R2) \times V_{NF}$ $(V_{NF} = 1.25\ V)$ Use a ceramic capacitor with a capacitance of 1 μF or higher for the output capacitor. An electrolytic capacitor may also be used. Use a capacitance value of 1,000 μF or lower.	VOUT = 1.8 V $(R_1 + R_2)/R2 = \frac{V_{OUT}}{V_{NF}} = 1.439\ V$ $R_1 = 0.439 \times R_2$ $R_2 = 20\ k\Omega$ $R_1 = 8.70\ k\Omega$	
DC/DC output voltage	$V_{OUT} = ((R1 + R2)/R2) \times V_{INV}$ $(V_{INV} = 1.25\ V)$	$V_{OUT} = 3.3\ V$ $(R_1 + R_2)/R_2 = \frac{V_{OUT}}{V_{INV}} = 2.64\ V$ $R_1 = 1.64 \times R_2$ $R_2 = 10\ k\Omega$ $R_1 = 16.4\ k\Omega$	

●Selecting application components

Block name	Setting procedure	Calculation example	
MAX DUTY (DTC)	$V_{DTC} = (R_2/(R_1 + R_2)) \times V_{REF}$ Max DUTY = $(V_{DTC} - V_{DD})/(V_{D100} - V_{DO}) \times 100$ [%] (V_{REF} = 3.0 V, V_{D0} = 1.0 V, V_{D100} = 2.0 V) (typ.)	R_2 = 20 kΩ, R_1 = 10 kΩ V_{OTL} = 2.0 V Max DUTY = (1.0/1.1) × 100 = 90.9%	
Soft start (DTC)	V_{FB} = $(V_{OUT}/V_{IN}) \times (V_{D100} - V_{DD}) + V_{DO}$ $V_{DTC} = V_{REF} \times (1 - \exp(-\frac{t}{CR}))$ $V_{FB} = V_{DTC}$ $t = -C \times R \times \text{IN}(1 - V_{FB}/V_{REF})$ (V_{REF} = 3.0 V, V_{D100} = 2.1 V, V_{D0} = 1.0 V)	C = 10 μF1 R_1 = 10 kΩ V_{OUT} = 3.3 V, Vcc= 13.5 V t = 55 ms	
Short protection circuit (SLP)	$T_1 = (C_{SCP} \times V_{SCP1})$ /ISCP (I_{SCP} = 2.5 μA, V_{SCP1} = 1 V, V_{SCP2} = 2 V)	t_1 = 50 ms t_2 = 100 ms C_{CSCP} = 0.125 μF	

●Setting phase compensation

1. Application stability conditions

The following conditions are required in order to ensure the stability of the negative feedback circuit.

Because DC/DC converter applications use a switching frequency, the overall gain (BW) should be set to 1/10th the switching frequency or lower. The target application characteristics can be summarized as follows:

- Phase lag should not exceed 150° at gain 1 (0 dB). (A minimum phase margin of 30°)
- BW (frequency with gain of 0 dB) should not exceed 1/10th the switching frequency.

Because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies for quick response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting 2 phase advances).
Because the GMB is determined by the phase compensation capacitor, attached between the error amp output and INV input, capacitance must be increased in order to lower the GBW.

(1) Standard integrator (low-pass filter)

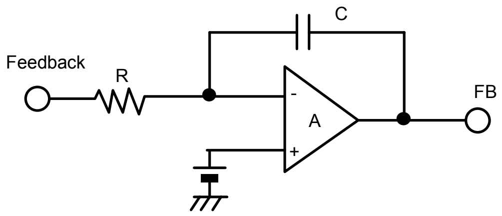
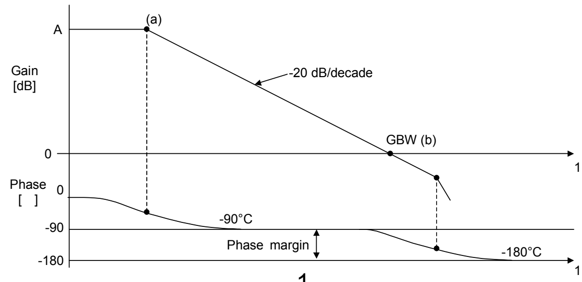


Fig. 32

(2) Integrator's open loop characteristics



At point (a), fa = $\frac{1}{2\pi RCA}$ (Hz)

Fig. 33

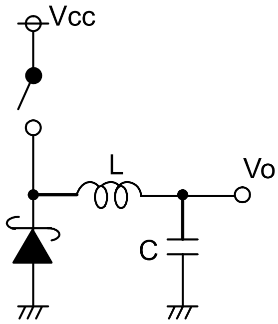
At point (b), fbGWB = $\frac{1}{2\pi RC}$ (Hz)

The error amp performs phase compensation of types (1) and (2), making it act as a low-pass filter.
For DC/DC converter applications, R refers to feedback resistors connected in parallel.

2. When the output capacitor is an electrolytic capacitor or other capacitor with a large ESR

When the output capacitor's ESR is large (> 1 Ω), phase compensation is reasonably simple. Because LC resonant circuits always exist in the output of DC/DC converter applications, the phase lag for those circuits is -180°. However, when an ESR component is present, a +90° phase advance occurs, reducing the phase lag to -90°. This is an extremely effective way of keeping the phase lag to within 150°C. However, it has the disadvantage of increasing the ripple component of the output voltage.

(1) LC resonant circuit



Resonance point and phase lag of -180° at

$$fr = \frac{1}{2\pi\sqrt{LC}} \quad [Hz]$$

Fig. 34

(2) With ESR

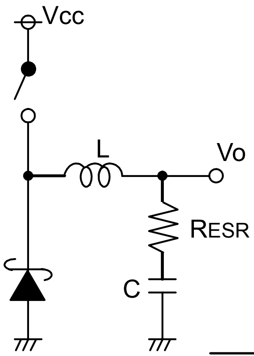


Fig. 35

Resonance point at fr = $\frac{1}{2\pi\sqrt{LC}}$ (Hz)

Phase advance at Fesr = $\frac{1}{2\pi\sqrt{R_{ESR}\ C}}$ (Hz)

Phase lag = -90°

One phase advance should be inserted due to variations in phase characteristics caused by ESR. This phase advance can be accomplished by either of the following methods:

(3) Insert C1 into the feedback resistors

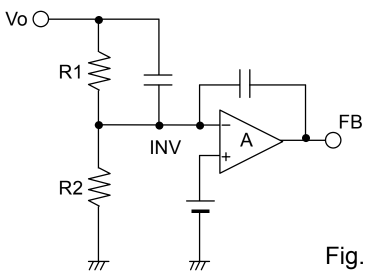


Fig. 36

(4) Insert R3 into the integrator

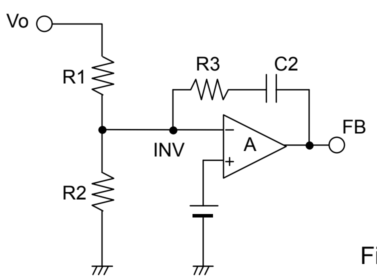


Fig. 37

Phase advance fz = $\frac{1}{2\,\pi\pi C1R}$ (Hz)

Phase advance fz = $\frac{1}{2\,\pi\pi C2R}$ (Hz)

To cancel LC resonance, set the phase advance frequency to the LC resonant frequency. This setting has been obtained in a simple fashion and does not reflect a rigorous calculation, so adjustment may be required for the actual implementation. These characteristics vary with board layout, load conditions, and other factors. They should be confirmed in the actual implementation during the mass production design process.

●**I/O Equivalent circuits**

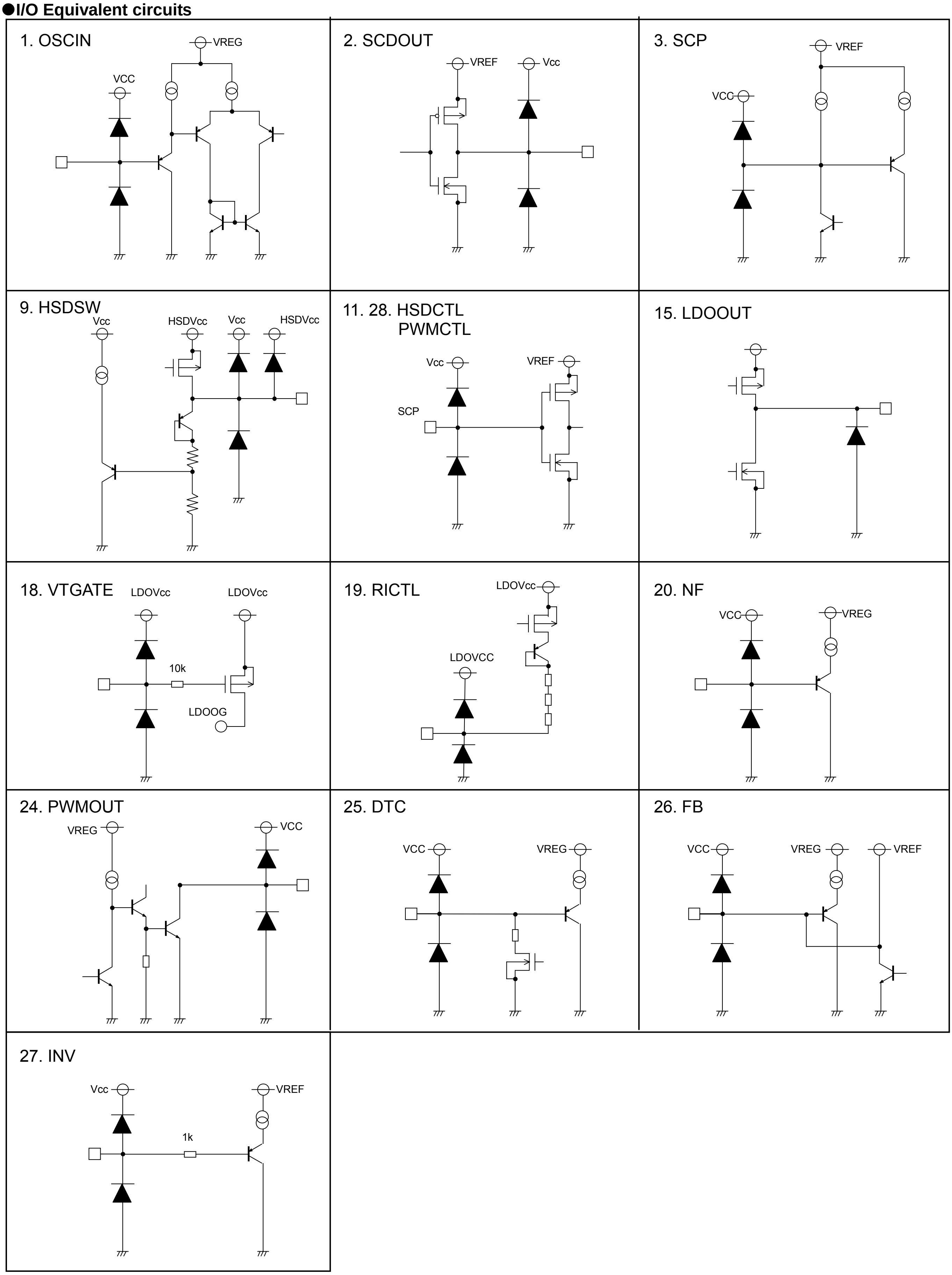


Fig.38 I/O Equivalent Circuits

●Operation Notes

1. Absolute maximum ratings

   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

2. GND potential

   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

3. Thermal design

   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.

4. Short circuit between terminals and erroneous mounting

   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

5. Operation in strong electromagnetic field

   Using the ICs in a strong electromagnetic field can cause operation malfunction.

6. Testing on application boards

   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

7. Regarding input pin of the IC (Fig. 40)

   This monolithic IC contains P^+ isolation and P substrate layers between adjacent elements to keep them isolated. P–N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

   When GND > Pin A and GND > Pin B, the P–N junction operates as a parasitic diode.

   When Pin B > GND > Pin A, the P–N junction operates as a parasitic transistor.

   Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

8. Ground wiring patterns

   The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

9. Thermal Shutdown Circuit (TSD)

   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

10. Over current protection circuit

    The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

11. When the Vcc pin is opposite in voltage to each pin in the application, the internal circuit or element may be damaged. For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. Use the output pin capacity with a maximum capacitance of 1000 μF. It is recommended to insert a diode in order to prevent back current flow in series with VCC or bypass diodes between VCC and each pin.

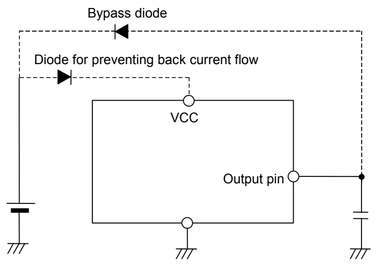


Fig. 39 Bypass diode

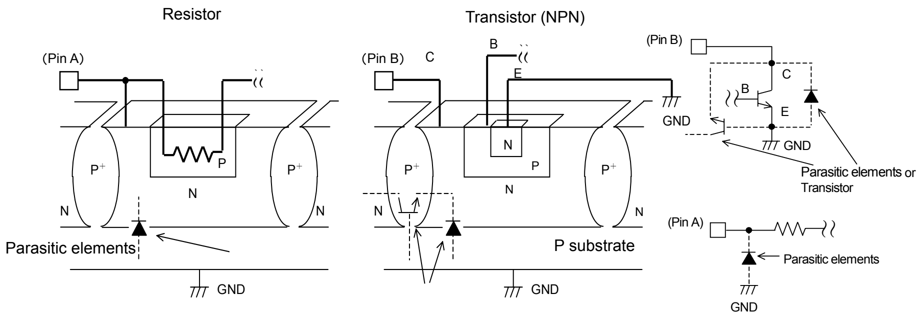
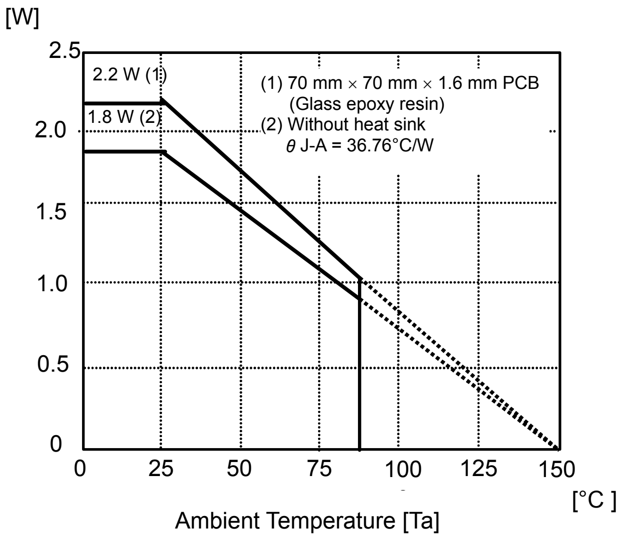
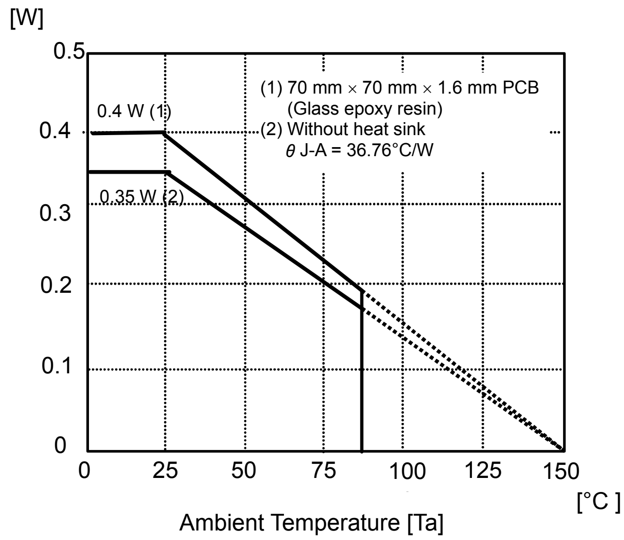


Fig. 40 Example of Simple Bipolar IC Architecture





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B	D		9	4	0	1		F	M	–	E	2

ROHM model name

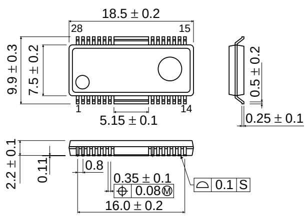
Part number

Packaging
FM: HSOP-M28
(BD9401FN)
FV: SSOP-B14
(BD9403FV)

Packaging specifications
E2: Emboss taping
(BD9403FV)
No: Tube container
(BD9401FM)

HSOP-M28

<Dimension>



(Unit:mm)

<Tape and Reel information>

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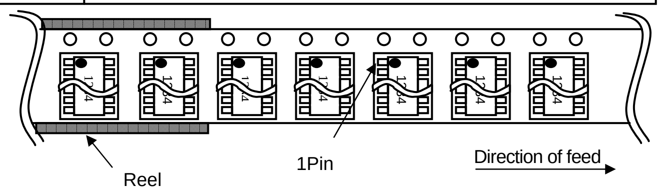
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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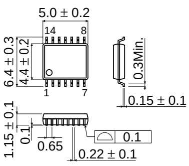

(Unit:mm)

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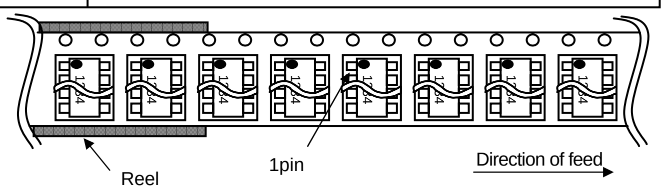

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