

N-Channel Power MOSFET

600V, 28A, 196mΩ

FEATURES

- Super-Junction technology
- High performance, small $R_{DS(on)} * Q_g$ figure of merit (FOM)
- High ruggedness performance
- 100% UIS & R_g tested
- High commutation performance
- ROHS Compliant
- Halogen-free according to IEC 61249-2-21

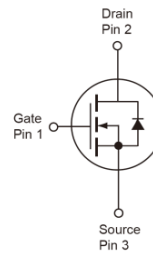
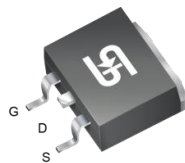
KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	196	mΩ
Q_g	39	nC

APPLICATIONS

- Power Supply
- AC/DC LED Lighting



TO-263-2L (D²PAK-2L)



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	28
		$T_C = 100^\circ\text{C}$	18
Pulsed Drain Current ^(Note 2)	I_{DM}	84	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	152	W
Single Pulse Avalanche Energy ^(Note 3)	E_{AS}	440	mJ
Single Pulse Avalanche Current ^(Note 3)	I_{AS}	4.2	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.82	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	40	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	$V_{GS(TH)}$	3	4.2	5	V
Gate Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10\text{V}, I_D = 9.5\text{A}$	$R_{DS(on)}$	--	182	196	m Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 300\text{V}, I_D = 20\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	39	--	nC
Gate-Source Charge		Q_{gs}	--	12	--	
Gate-Drain Charge		Q_{gd}	--	17	--	
Input Capacitance	$V_{DS} = 300\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	1566	--	pF
Output Capacitance		C_{oss}	--	46	--	
Reverse Transfer Capacitance		C_{rss}	--	11	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	2.3	4.6	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 300\text{V}, R_G = 10\Omega,$ $I_D = 10\text{A}, V_{GS} = 10\text{V},$	$t_{d(on)}$	--	32	--	ns
Turn-On Rise Time		t_r	--	31	--	
Turn-Off Delay Time		$t_{d(off)}$	--	55	--	
Turn-Off Fall Time		t_f	--	11	--	
Source-Drain Diode						
Body-Diode Continuous Forward Current		I_S	--	--	20	A
Body-Diode Pulsed Current		I_{SM}	--	--	60	A
Forward Voltage (Note 4)	$I_S = 20\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.5	V
Reverse Recovery Time	$I_S = 20\text{A}$ $di_f/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	420	--	ns
Reverse Recovery Charge		Q_{rr}	--	8.4	--	μC

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 50\text{mH}, I_{AS} = 4.2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega,$ Starting $T_J = 25^\circ\text{C}$
- Pulse test: $PW \leq 300\mu\text{s},$ duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

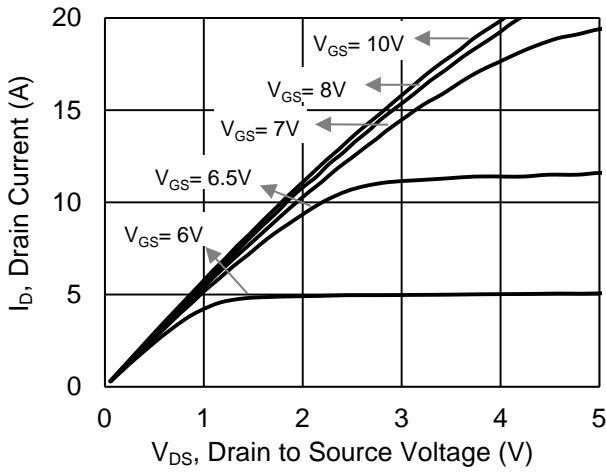
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM60NC196CM2 RNG	TO-263-2L (D ² PAK-2L)	800pcs / 13" Reel

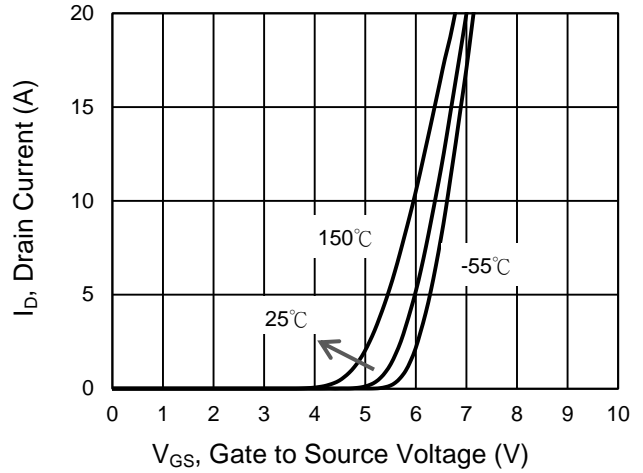
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

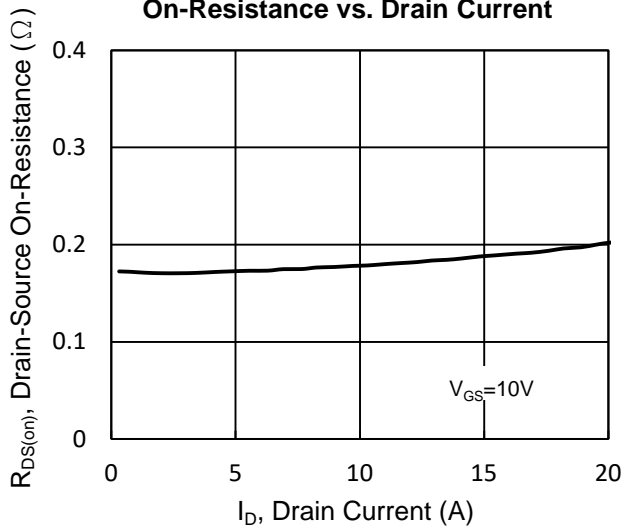
Output Characteristics



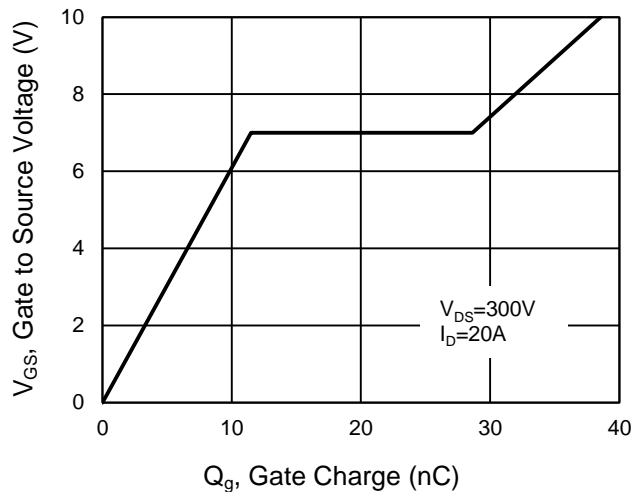
Transfer Characteristics



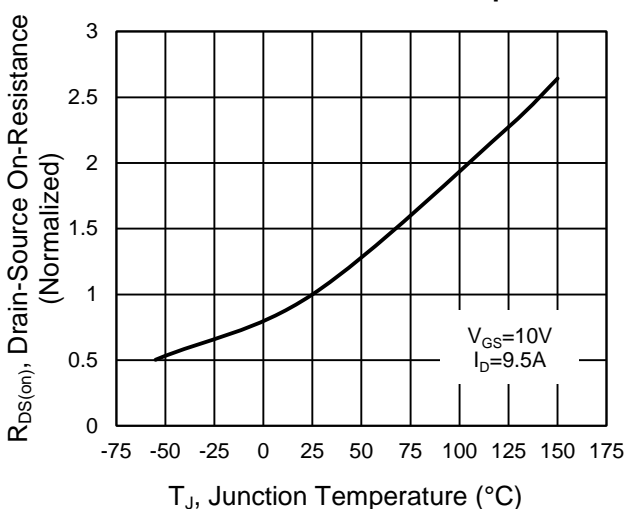
On-Resistance vs. Drain Current



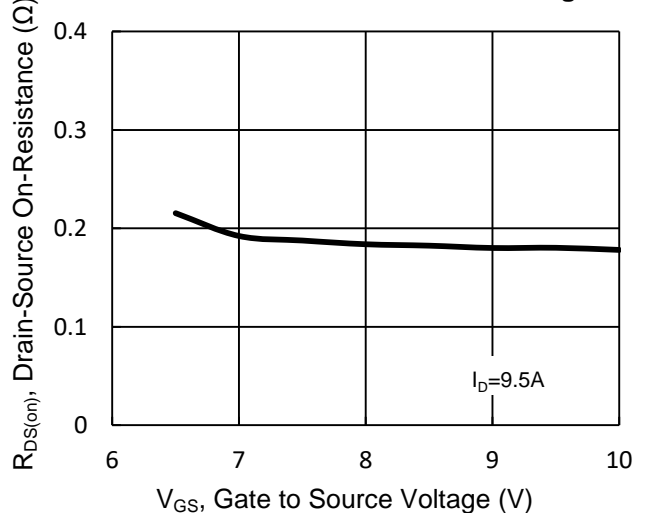
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



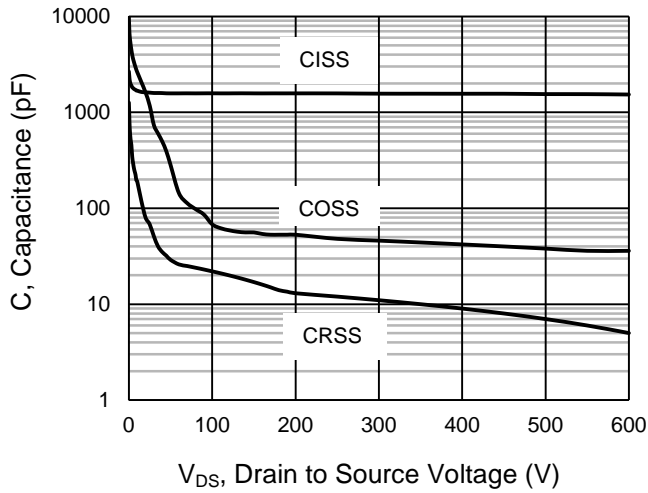
On-Resistance vs. Gate-Source Voltage



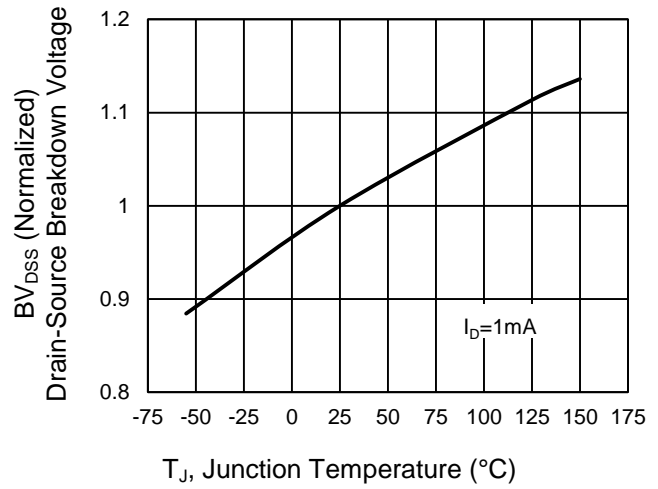
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

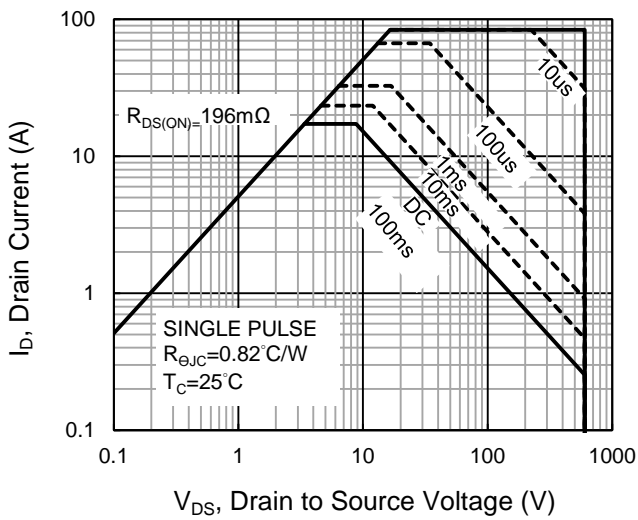
Capacitance vs. Drain-Source Voltage



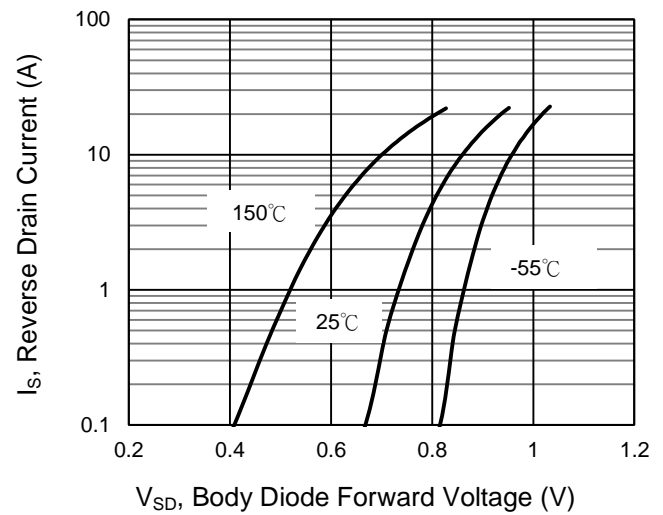
BV_{DSS} vs. Junction Temperature



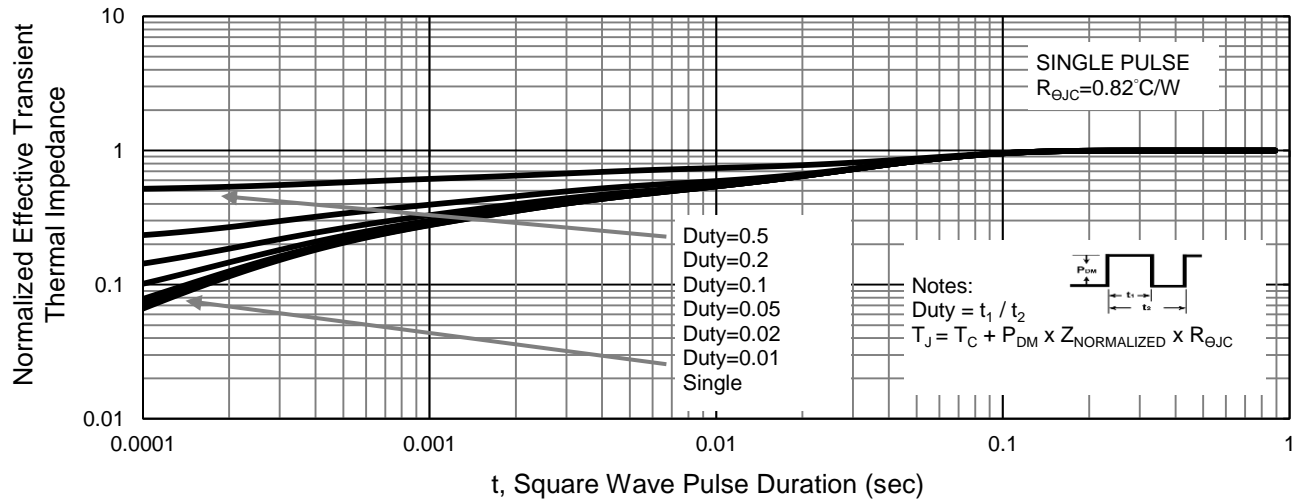
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

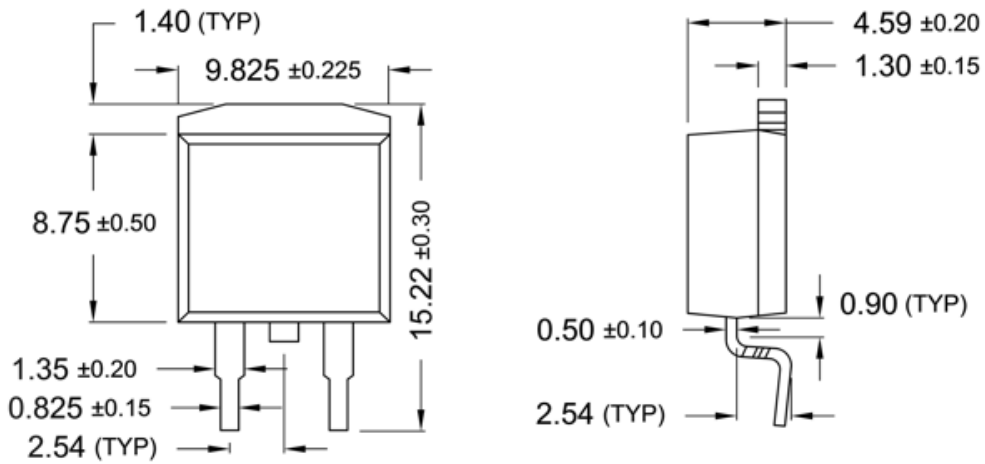


Normalized Thermal Transient Impedance, Junction-to-Case

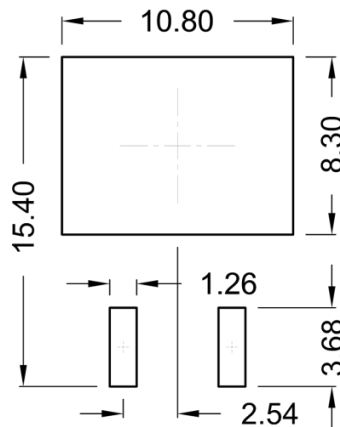


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-263



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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