AsahiKASEI
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AK7770EQ

Audio DSP with Multi-Channel Audio CODEC

GENERAL DESCRIPTION

The AK7770 is a digital signal processor with an integrated 4-channel audio ADC and a 6-channel audio DAC, as well as an S/PDIF transmitter. It utilizes an enhanced dual bit architecture that results in wide dynamic range for the ADC, and the advanced multi-bit architecture of the DAC enables wide dynamic range and low out-of-band noise. Two sample-rate converters are integrated, allowing for operation at 48kHz sampling rate with input rates of 32kHz, 44.1kHz, or 48kHz. Volume control, compression, EQ and sound processing are performed by the DSP. In addition, delay adjustment up to 70ms is possible for four output channels through the integrated delay RAM. The AK7770 is packaged in a space-saving 80-pin LQFP package.

FEATURES

■ **DSP**
- **Data Width: 24-bit (Data RAM F20.4 floating Point)**
- **Processing Speed: 13.5 ns (1536step/fs; fs = 48kHz)**
- **Multiplication: 20 x 16 → 36-bit Double precision arithmetic available**
- **Program RAM: 1536 x 36-bit**
- **Coefficient RAM: 1536 x 16-bit**
- **Offset RAM: 64 x 14-bit**
- **DRAM: 14kword (1word = F16.4 floating point)**
- **Sample Rate: fs = 48kHz**
- **Master / Slave operation**

■ **4:2 Selector with Input Pre-amp**

■ **4ch 24-bit ADC**
- **64-times oversampling**
- **Sample Rate: 48kHz**
- **S/(N+D): 84dB (fs = 48kHz)**
- **DR, S/N: 96dB (fs = 48kHz)**
- **Digital HPF for offset DC cancellation**
- **Channel independent Digital Volume control (+24/-103dB, 0.5dB step)**
- **Soft Mute**

■ **6ch 24-bit DAC**
- **128-times oversampling**
- **Sample Rate: 48kHz**
- **S/(N+D): 88dB (fs = 48kHz)**
- **DR, S/N: 100dB**
- **Channel independent Digital Volume control (+12/-115dB, 0.5dBstep)**
- **Soft Mute**
- **Digital de-emphasis**

- **Stereo Headphone Amplifier with Volume Control**
  - **DAC3 direct connection**
  - **S/(N+D): 73dB (fs=48kHz)**
  - **S/N: 86dB (fs=48kHz)**
  - **Analog volume control (+0/-50dB,1.0/2.0/4.0dB per step)**
  - **Output power: 22.5mW@16Ω**
  - **No click noise at power ON/OFF**
- **Headphone Detection Circuit (denounce circuit)**
- **High Tolerance to Clock Jitter**
- **Sample Rate Converter**
  - **Dual 2ch SRC**
  - **Input sample rate: 32kHz~48kHz**
  - **Output sample rate: 48kHz fixed**
- **DIT**
  - **S/PDIF, IEC958, AES/EBU, EIAJ CP1201**
  - **Output Selector (DIT or Through)**
  - **24 bit interface format**
  - **16 bit interface format**
- **CMOS Level Digital I/F (for 3.3V)**
- **Master Clock Input: 256fs (fs=48kHz)**
- **Master Clock Output: 128fs, 192fs, 256fs, 384fs**
- **Three Digital Audio Inputs**
- **I²C μP I/F**
- **Power Supply: +3.3V ±0.3V, +1.8V ±0.1V**
- **Temperature Range: -10°C~70°C**
- **Package: 80pin LQFP (0.5mm pitch)**

■ Block Diagram

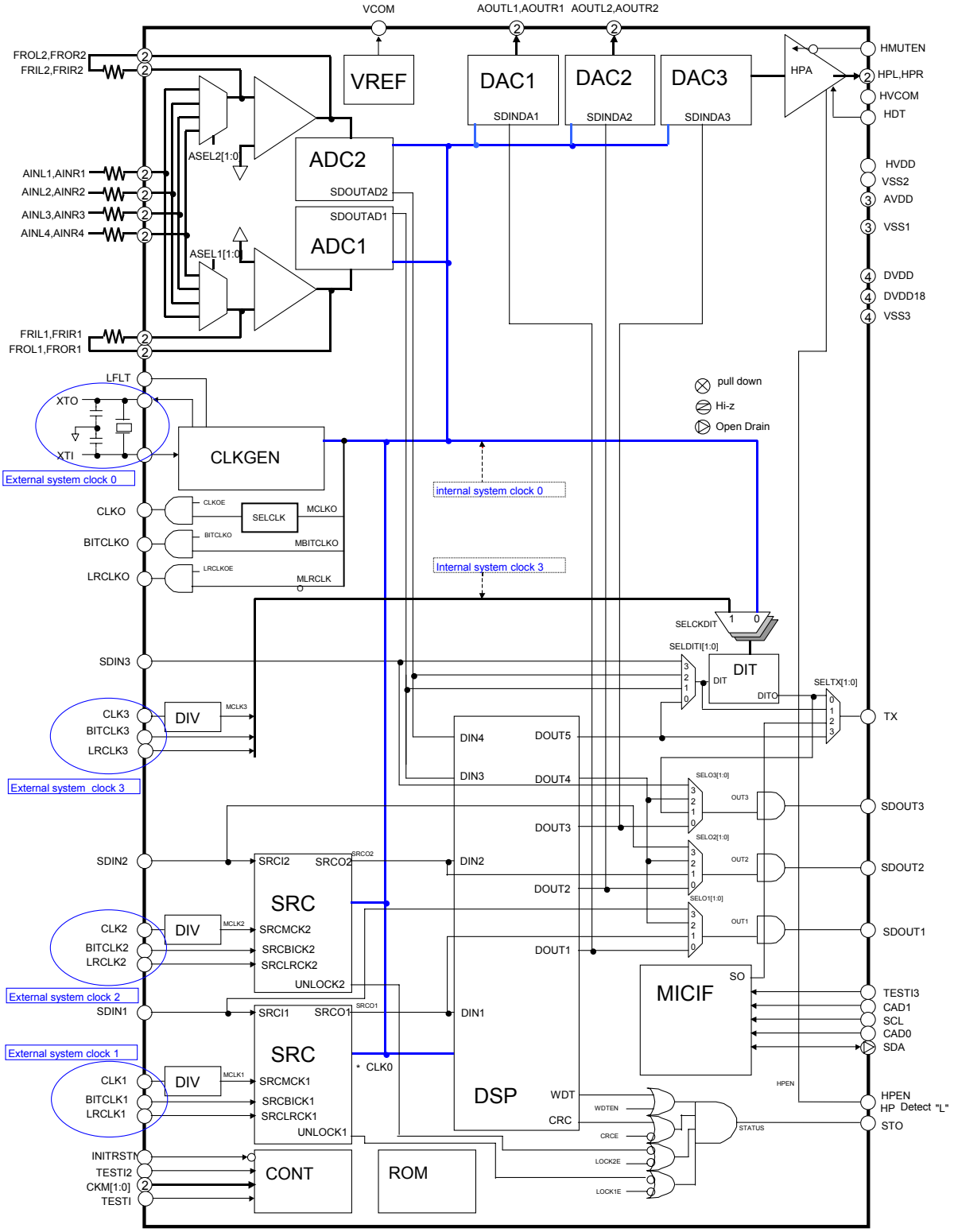


Figure 1. Block Diagram

Figure 1shows a simplified diagram of the AK7770, which is not the perfect same as the actual circuit diagram.

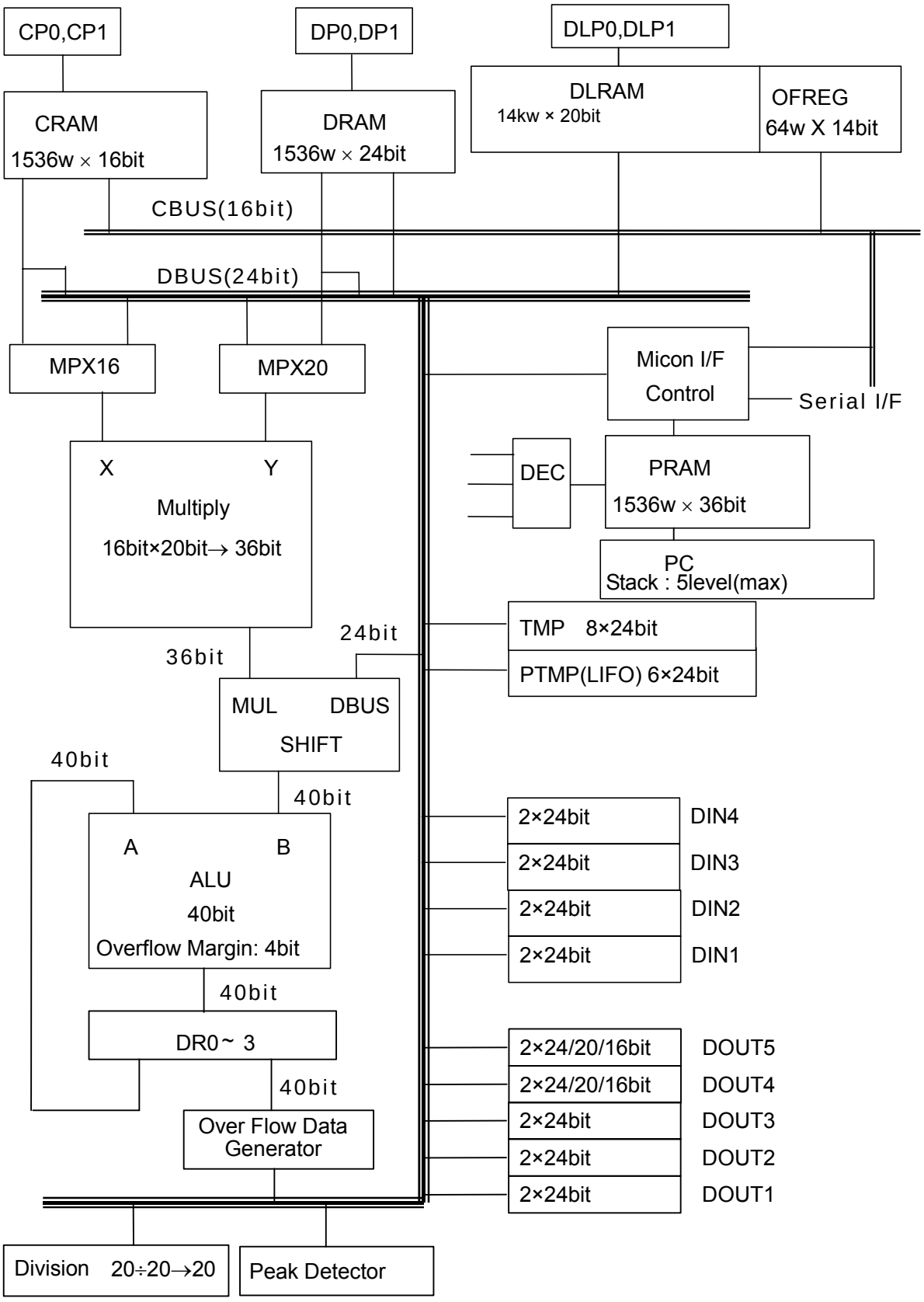
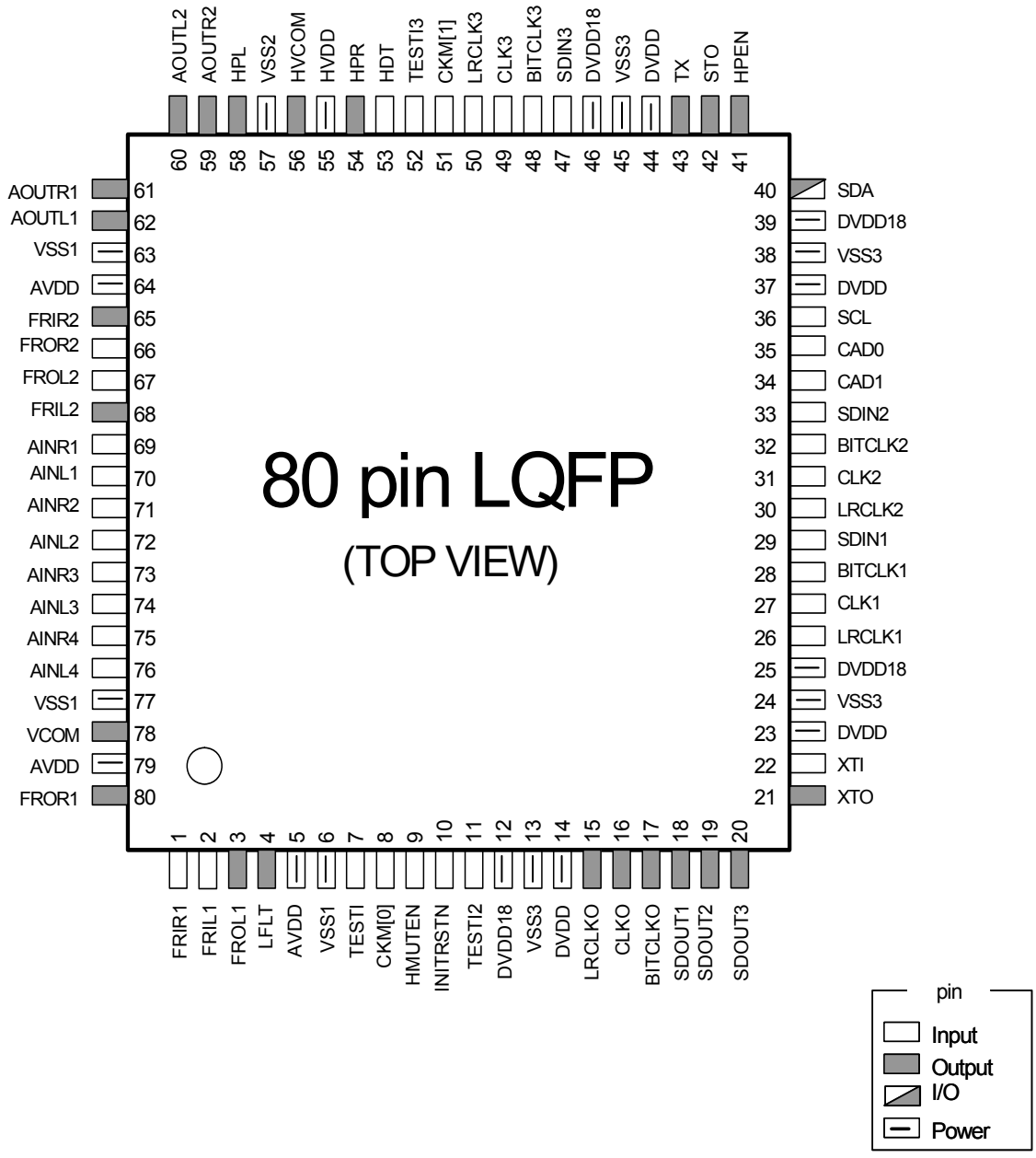


Figure 2. AK7770 DSP Block Diagram

■ Ordering Information

AK7770EQ	-10 ~ +70°C	80pin LQFP (0.5mm pitch)
AKD7770	Evaluation board	

■ Pin Assignment



PIN FUNCTION

No.	Pin name	I/O	Function	Classification
1	FRIR1	I	Rch Feedback Resistance Input Pin for ADC1	Analog
2	FRIL1	I	Lch Feedback Resistance Input Pin for ADC1	
3	FROL1	O	Lch Feedback Resistance Output Pin for ADC1 At initial reset, this pin goes Hi-Z.	
4	LFLT	O	Loop Filter Pin. Connect a 10nF cap to AVDD. The output is AVDD at initial reset	
5	AVDD	-	Analog Power Supply Pin 3.3V (typ)	Analog power supply
6	VSS1	-	Analog Ground Pin 0V (connected to silicon substrate)	
7	TESTI	I	Test Pin (Internal pull-down) Connect to GND.	Test
8	CKM [0]	I	Clock Mode Selection Pin Connect to GND.	Mode choice
9	HMUTEN	I	Headphone Amplifier Mute Pin	Headphones
10	INITRSTN	I	Reset Pin (for initialization) Use to initialize the AK7770.	Reset
11	TEST2	I	Test Pin Connect to GND.	Test
12	DVDD18	-	Digital Power Supply Pin 1.8V(typ)	Digital power supply
13	VSS3	-	Digital Ground Pin 0V	
14	DVDD	-	Digital Power Supply Pin 3.3V(typ)	
15	LRCLKO	O	Left/right Clock Output Pin The output in initial reset is “L”.	System clock
16	CLKO	O	Clock Output Pin The output in initial reset is “L”.	
17	BITCLKO	O	Bit Clock Output Pin The output in initial reset is “L”.	
18	SDOUT1	O	Serial Data Output 1 Pin The output in initial reset is “L”.	Serial data
19	SDOUT2	O	Serial Data Output 2 Pin The output in initial reset is “L”.	
20	SDOUT3	O	Serial Data Output 3 Pin The output in initial reset is “L”.	
21	XTO	O	Crystal Oscillator Output Pin Connect a crystal oscillator between the XTI pin and XTO pin. Leave open when using an external clock source. The output in initial reset is undetermined.	A system clock
22	XTI	I	Crystal Oscillator Input Pin Connect a crystal oscillator between the XTI pin and XTO pin. Input an external clock into the XTI pin when not using a crystal oscillator.	
23	DVDD	-	Digital Power Supply Pin 3.3V(typ)	Digital power supply
24	VSS3	-	Digital Ground Pin 0V	
25	DVDD18	-	Digital Power Supply Pin 1.8V(typ)	

No.	Pin name	I/O	Function	Classification
26	LRCLK1	I	Left/Right Clock Input 1 Pin	System clock
27	CLK1	I	Master Clock 1 Pin	
28	BITCLK1	I	Bit Clock 1 Pin	
29	SDIN1	I	Serial Data Input 1 Pin	Serial data
30	LRCLK2	I	Left/Right Clock Input 2 Pin	System clock
31	CLK2	I	Master Clock 2 Pin	
32	BITCLK2	I	Bit Clock 2 Pin	
33	SDIN2	I	Serial Data Input 2 Pin	
34	CAD1	I	I2C Bus Address Pin 1	I2C interface
35	CAD0	I	I2C Bus Address Pin 0	I2C interface
36	SCL	I	I2C Clock Pin	I2C interface
37	DVDD	-	Digital Power Supply Pin 3.3V(typ)	Digital power supply
38	VSS3	-	Digital Ground Pin 0V	
39	DVDD18	-	Digital Power Supply Pin 1.8V(typ)	
40	SDA	I/O	I^2C Bus Data Clock Pin SDA goes to “Hi-Z” during initial reset.	I2C interface
41	HPEN	O	Headphone Detect Output Pin Initial reset for headphone search is determined by the state of HDT	Headphones
42	STO	O	Status Output Pin When HDT = “H”, STO = “L” When HDT = “L”, STO = “H” The output in initial reset is “H”	Status
43	TX	O	S/PDIF transmitter Output Pin S/PDIF data is output when SELTX [1:0] bit= “00”. “L” during initial rest.	TX
44	DVDD	-	Digital Power Supply Pin 3.3V(typ)	Digital power supply
45	VSS3	-	Digital Ground Pin 0V	
46	DVDD18	-	Digital Power Supply Pin 1.8V(typ)	
47	SDIN3	I	Serial Data Input 3 Pin	Serial data
48	BITCLK3	I	Bit Clock 3 Pin	System clock
49	CLK3	I	Master Clock 3 Pin	
50	LRCLK3	I	Left/Right Clock 3 Pin	
51	CKM [1]	I	Clock Mode Selection Pin Connect to GND.	Mode selection
52	TESTI3	I	Test Pin This pin must be connected to DVDD.	Test

No.	Pin name	I/O	Function	Classification
53	HDT	I	Headphone Detection Pin	Headphones
54	HPR	O	Headphone Rch Output Pin Output is VSS2 at initial reset	Headphones
55	HVDD	-	Headphone Power Supply Pin 3.3V(typ)	Analog power supply
56	HVCOM	O	Headphone Common Voltage Output Pin Connect a of 1μF cap to VSS2. Do not use for an outside circuits. Output at initial reset is VSS2	Headphones
57	VSS2	-	Headphone Ground Pin 0V	Analog power supply
58	HPL	O	Headphone Lch Output Pin Output is VSS2 at initial reset	Headphone output
59	AOUTR2	O	DAC2 Rch Output Pin Output at initial reset is VSS1	Analog output
60	AOUTL2	O	DAC2 Lch Output Pin Output at initial reset is VSS1	
61	AOUTR1	O	DAC1 Rch Output Pin Output at initial reset is VSS1	
62	AOUTL1	O	DAC1 Lch Output Pin Output at initial reset is VSS1	
63	VSS1	-	Analog Ground Pin 0V (connected to silicon substrate)	Analog power supply
64	AVDD	-	Analog Power Supply Pin 3.3V (typ)	Analog power supply
65	FROR2	O	ADC2 Rch Feedback Resistance Output Pin The output at initial reset is Hi-Z	Analog output
66	FRIR2	I	ADC2 Rch Feedback Resistance Input Pin	Analog input
67	FRIL2	I	ADC2 Lch Feedback Resistance Input Pin	Analog input
68	FROL2	O	ADC2 Lch Feedback Resistance Input Pin The output at initial reset is Hi-Z.	Analog output
69	AINR1	I	ADC Rch Single-ended Input 1 Pin	Analog input
70	AINL1	I	ADC Lch Single-ended Input 1 Pin	
71	AINR2	I	ADC Rch Single-ended Input 2 Pin	
72	AINL2	I	ADC Lch Single-ended Input 2 Pin	
73	AINR3	I	ADC Rch Single-ended Input 3 Pin	
74	AINL3	I	ADC Lch Single-ended Input 3 Pin	
75	AINR4	I	ADC Rch Single-ended Input 4 Pin	
76	AINL4	I	ADC Lch Single-ended Input 4 Pin	
77	VSS1	-	Analog Power Supply Pin 0.0V	Analog power supply
78	VCOM	O	Analog Common Voltage Output Pin Output at initial reset is VSS1. Connect capacitors of 0.1uF and 2.2uF between this pin and VSS1. No external circuits should be connected to this pin.	Analog output
79	AVDD	-	Analog Power Supply Pin 3.3V (typ)	Analog power supply
80	FROR1	O	Rch Feedback Resistance Output Pin for ADC1 The output in initial reset is Hi-Z	Analog output

Note 1. Do not leave digital input pins floating.
Note 2. When analog input pins (AINL1-4 pins, AINR1-4) are not used, leave them open.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	FRIR1-2, FRIL1-2, FROL1-2, FROR1-2, XTO, AOUTL1-2, AOUTR1-2, AINL1-4, AINR1-4	These pins should be open.
Digital	LRCLKO,CLKO, BITCLKO, SDOUT1-3, HPEN, HPR, HPL	These pins should be open.
	TESTI2, CLK1-3, BITCLK1-3, LRCLK1-3 SDIN1-3, HDT	These pins should be connected to VSS3.
	HMUTEN	This pin should be connected to DVDD.

ABSOLUTE MAXIMUM RATINGS

(VSS1 = VSS2 = VSS3=0V: Note 3)

Parameter	Symbol	min	max	Units
Power supply voltage				
Analog	AVDD	-0.3	4.3	V
Analog	HVDD	-0.3	4.3	V
Digital	DVDD	-0.3	4.3	V
Digital	DVDD18	-0.3	2.5	V
Input current (except power supply pins)	IIN	-	±10	mA
Analog input voltage AINL1~AINL4, AINR1~AINR4 FRIL1, FRIL2, FRIR1, FRIL2	VINA	-0.3	AVDD+0.3	V
Digital input voltage	VIND	-0.3	DVDD+0.3	V
Ambient operating temperature	Ta	-10	70	°C
Storage temperature	Tstg	-65	150	°C

Note 3. All voltages referred to ground. Connect VSS1, VSS2, VSS3 to the same ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OERATING CONDITIONS

(VSS1 = VSS2 = VSS3=0V: Note 3)

Parameter		Symbol	min	typ	max	Units
Supply voltage	Analog	AVDD	3.0	3.3	3.6	V
	Analog	HVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	Digital	DVDD18	1.7	1.8	1.9	V
	Difference	HVDD-AVDD	-0.3	0	+0.3	V
	Difference	HVDD-DVDD	-0.3	0	+0.3	V
	Difference	AVDD-DVDD	-0.3	0	+0.3	V

Note 4. The power supply sequence for AVDD HVDD, DVDD, DVDD18 is not critical but all power supplies must be On before start operating the AK7770.

Note 5. Do not turn off the power supply of the AK7770 with the power supply of the surrounding device turned on. DVDD must not exceed the pull-up of SDA and SCL of I^2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

*AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

■ ADC1/2

(Ta=25 °C; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=0V; Signal frequency = 1kHz; Measurement bandwidth =20Hz~20kHz , fs=48kHz fs; SRC reset; unless otherwise specified)

Parameter		min	typ	max	Units
Pre-AMP	Feedback Resistance	10		30	kΩ
	S/(N+D) (Note 6)		99		dB
	S/N (A-weighted) (Note 6)		105		dB
	Load Capacitance			20	pF
Pre-AMP + ADC1 ADC2	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dBFS)	74	84		dB
	Dynamic range fs = 48kHz (A-weighted) (Note 7, Note 8)	88	96		dB
	S/N fs = 48kHz (A-weighted) (Note 7)	85	96		dB
	Interchannel Isolation((f=1kHz) (Note 9)	85	100		dB
ADC1 ADC2	**DC Accuracy**				
	Gain mis-match between channels		0.1	0.3	dB
	Analog input				
	Input voltage	2.05	2.2	2.35	Vp-p

Note 6. Value measured with an input resistance of 47kΩ and a feedback resistance of 16kΩ with a 2Vrms input voltage.
Note 7. The value measured through the pre-amp and ADC with an input resistance of 47kΩ and a feedback resistance of 16kΩ with a 2Vrms input voltage.
Note 8. S/(N+D) with an input signal of -60dBFS
Note 9. Isolation between AINL1-4, AINR1-4 with a -1dBFS input signal.
Note 10. When the SRC on DIT operate asynchronously, the performance may be degraded.

■ DAC1/2

(Ta= 25°C; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=0V;
Signal frequency = 1kHz; Measurement bandwidth =20Hz~20kHz, fs=48kHz fs; SRC reset; unless otherwise specified)

Parameter		min	typ	max	Units
DAC1 DAC2	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (0 dBFS)	78	88		dB
	Dynamic range (A-weighted) (Note 11)	92	100		dB
	S/N (A-weighted)	92	100		dB
	Interchannel Isolation (f=1kHz) (Note 12)	90	100		dB
	DC Accuracy				
	Gain mis-match between channels		0.2	0.5	dB
	Analog output				
	Output voltage (Note 13)	2.02	2.18	2.34	Vp-p
	Load resistance	5			kΩ
	Load capacitance			30	pF

Note 11. S/(N+D) with a -60dBFS input signal
Note 12. Isolation between Lch-Rch between each DAC
Note 13. Full scale output voltage

■ DAC3 + HP Amp

(Ta=25°C; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=0V;
Signal frequency = 1kHz; Measurement bandwidth =20Hz~20kHz , fs=48kHz fs; SRC reset; fs=48kHzs)

Parameter		min	typ	max	Units
Analog Volume Control Characteristics OPGA):					
Gain	Maximum (OPGA[4:0] bits= "1FH")	-	+0	-	dB
	Minimum (OPGA[4:0] bits= "01H")	-	-50	-	dB
Step size	+0dB ~ -16dB	0.1	1	-	dB
	-16dB ~ -38dB	0.1	2	-	dB
	-38dB ~ -50dB	-	4	-	dB
Headphone-Amp Characteristics: DAC → HPL/HPR pins, RL=16Ω					
Output Voltage		1.53	1.7	1.87	Vpp
S/(N+D)	(–3dBFS)	63	73	-	dB
S/N	(A-weighted)	80	86	-	dB
Inter channel Isolation		60	80	-	dB
Inter channel Gain Mismatch		-	0.1	0.5	dB
Load Resistance	(RL, Figure 3)	16	-	-	Ω
Load Capacitance	(C1, Figure 3)	-	-	30	pF
Load Capacitance	(C2, Figure 3)	-	-	300	pF

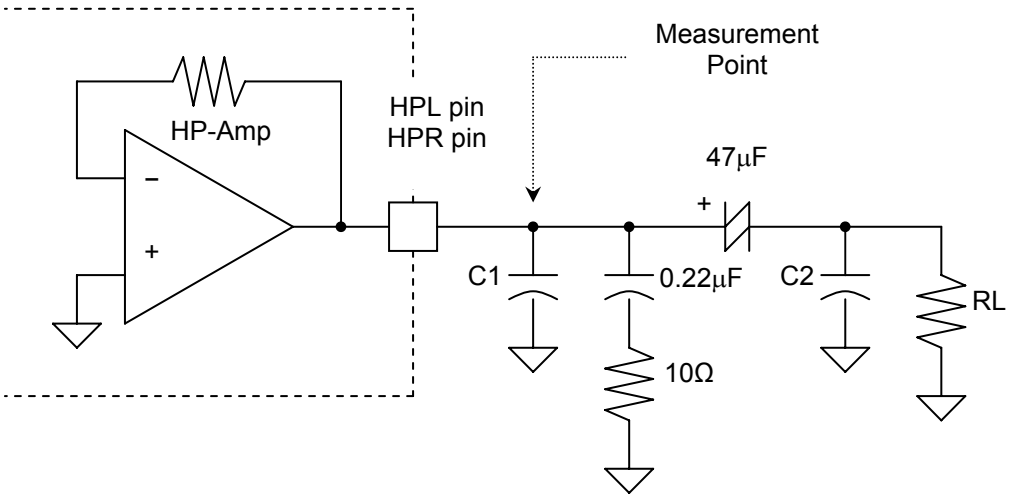


Figure 3. Headphone amplifier output circuit

■ SRC (SRC1, SRC2)

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.3V; DVDD18=1.8V; VSS1=VSS2=VSS3=0V;
Input signal frequency = 1kHz; measurement bandwidth = 20Hz to FSO/2, fs=48kHz)

Parameter	Symbol	min	typ	max	Units
Resolution				24	Bits
Input Sample Rate	FSI	32		48	kHz
Output Sample Rate	FSO	-	48	-	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=48kHz/44.1kHz			-112		dB
FSO/FSI=48kHz/32kHz			-112		dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=48kHz/44.1kHz			113		dB
FSO/FSI=48kHz/32kHz			113		dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)					
FSO/FSI=48kHz/32kHz			115		dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.98		1.5	-

DC CHARACTERISTICS

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, VSS1 = VSS2 = VSS3=0V)

Parameter	Symbol	min	typ	max	Units
High level input voltage (Note 14)	VIH	80%DVDD			V
Low level input voltage (Note 14)	VIL			20%DVDD	V
SCL, SDA high level input voltage	VIH	70%DVDD			V
SCL, SDA low level input voltage	VIL			30%DVDD	V
HDT high level input voltage	VIH	85%HVDD			V
HDT low level input voltage	VIL			45%HVDD	V
High level output voltage Iout=-100µA	VOH	DVDD-0.5			V
Low level output voltage Iout=100µA (Note 15)	VOL			0.5	V
SDA low level output voltage Iout=3mA	VOL			0.4	V
Input leakage current (Note 16)	Iin			±10	µA
Input leakage current pull-down pin (Note 17)	Iid		22		µA
Input leakage current XTI pin	Iix		26		µA

Note 14. SCL, SDA and HDT pins are not included.
Note 15. The SDA pin is not included
Note 16. Pull-down pins and the XTI pin are not included.
Note 17. Pull-down pins (Typ 150k) and TESTI

[Description rule]
Regarding the input/output levels in the text, the low level will be represented as “L”, and the high level as “H”.
In principle, “0” and “1” will be used to represent the bus (serial/parallel) such as registers.
##h means hexadecimal code. (#=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

POWER CONSUMPTION

(Ta=25°C; AVDD=HVDD=DVDD=3.0~3.6V(typ=3.3V, max=3.6V); DVDD18=1.7~1.9V(typ=1.8V, max=1.9V); VSS1= VSS2 = VSS3=0V)

Parameter	min	typ	max	Units
Power Supply				
Power supply electric current				
Normal Operation				
AVDD		75	-	mA
HVDD		6	-	mA
DVDD		5	-	mA
DVDD18 (Note 18)		58	85	mA
AVDD+HVDD+DVDD			120	mA
Reset (INITRSTN pin = "L" reference data)				
AVDD+HVDD+DVDD+DVDD18 (Note 19)		2	-	mA

Note 18. DVDD18 value varies with use frequency and DSP program contents.

Note 19. This is a reference value when using a crystal oscillator.
Since most of the supply current at the initial reset state is in the oscillator section, the value may vary slightly according to the crystal type and the external circuit. This is a "reference data" only.

DIGITAL FILTER CHARACTERISTICS

■ ADC1/2

(Ta=-10°C ~70°C; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V; fs=48kHz; Note 20)

Parameter	Symbol	min	typ	max	Units
PassBand (±0.1dB) (Note 21)	PB	0		18.9	kHz
(-0.2dB)			20.0		kHz
(-3.0dB)			23.0		kHz
Stopband	SB	28			kHz
Passband Ripple (Note 21)	PR			±0.04	dB
Stop band attenuation (Note 22, Note 23)	SA	68			dB
Group Delay deviation	ΔGD			0	μs
Group Delay (Ts=1/fs)	GD		16		Ts
Digital filter + analog filter					
Amplitude characteristic 20Hz~20.0kHz (Note 24)			±0.5		dB

Note 20. Frequency of each amplitude characteristic is in proportion to fs (sampling rate). The characteristic of the high pass filter is not included.

Note 21. The passband is from DC to 18.9kHz when fs=48kHz.

Note 22. Attenuation frequency is 48kHz to 3.044MHz when fs=48kHz.

Note 23. When fs = 48kHz, the analog modulator samples the input signal at 3.072MHz. There is no attenuation of an input signal in band (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3…) of integer times the sampling frequency of the digital filter.

Note 24. Value through Pre-Amp and ADC. External input resistance is 47kΩ, and feedback resistance is 16kΩ.

■ DAC1-3

(Ta=-10°C ~70°C; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V; fs=48kHz; DEM=OFF)

Parameter	Symbol	min	typ	max	Units
Passband (±0.05dB) (Note 25) (-6.0dB)	PB	0	 24	21.7	kHz kHz
Stopband (Note 25)	SB	26.2			kHz
Passband ripple	PR			±0.01	dB
Stopband Attenuation	SA	64			dB
Group delay (Ts=1/fs) (Note 26)	GD		24		Ts
Digital filter + analog filter					
Amplitude characteristic 20Hz~20.0kHz			±0.5		dB

Note 25. The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535 * fs (@ -0.05dB), and SB=0.5465 * fs, respectively.

Note 26. The digital filter's delay is calculated as the time from setting data into the input register until an analog signal is output.

■ SRC1/2

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V)

Parameter	Symbol	min	typ	max	Units
Passband -0.01dB (0.980≤FSO/FSI≤1.500)	PB	0		0.4583FSI	kHz
Stop Band (0.980≤FSO/FSI≤1.500)	SB	0.5417FSI			kHz
Passband ripple	PR			± 0.01	dB
Stop band attenuation	SA	102.2			dB
Group Delay (Ts=1/fs) (Note 27)	GD		56		Ts

Note 27. SRC delay time is calculated from the start of SRCLRCK just after data input to the start of LRCLKO just after data output, when there is no phase difference between SRCLRCK and LRCLKO.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V)

Parameter	Sysmbol	Min	typ	max	Units
XTI					
a) with a crystal oscillator	fXTI	-	12.288	-	MHz
b) with an external clock					
Duty cycle ratio		40	50	60	%
	fXTI	11.0		12.4	MHz
CLK1, CLK2 Frequency (Note 28)	fCK	2.0	12.288	50	MHz
Duty cycle ratio		40	50	60	%
Clock speed		256		1024	fs
LRCLK1, LRCLK2 Frequency (Note 29)	fs	8	48	48.4	kHz
BITCLK1, BITCLK2 Frequency					
High level width	tBCLKH	150			ns
Low level width	tBCLKL	150			ns
CLK3 Frequency (Note 28)	fCK	11.0	12.288	50	MHz
Duty cycle ratio		40	50	60	%
Clock speed		256		1024	fs
LRCLK3 Frequency (Note 29)	fs	43	48	48.4	kHz
BITCLK3 Frequency					
High level width	tBCLKH	150			ns
Low level width	tBCLKL	150			ns

Note 28. CLKn and LRCLKn must occur in the same period, but phase matching is not critical.
Note 29. The sample rate must match LRCLK.

■ Reset

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V)

Parameter	Symbol	Min	typ	max	Units
INITRSTN (Note 30)	tRST	600			ns

Note 30. Power supply must be up and a master clock must be present before initializing reset.

■ Audio System Interface

1. SDIN1~SDIN3, SDOUT1~SDOUT3

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1 = VSS2 = VSS3=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Units
Input					
Delay time from BITCLKn "↑"to LRCLK (Note 31)	tBLRD	20			ns
Delay time from LRCLKn to BITCLKn "↑" (Note 31)	tLRBD	20			ns
Serial data entry latch setup time	tBSIDS	80			ns
Serial data entry latch hold time	tBSIDH	80			ns
Output					
BITCLKO frequency	fBCLK		64		fs
BITCLKO duty cycle ratio			50		%
Delay time from BITCLKO "↓" to LRCLKO	tMBL	-20		40	ns
Delay time from LRCLKO to SDOUTn (Only MSB)	tLRD			80	ns
Delay time from BITCLKO to SDOUTn	tBSOD			80	ns
SDINn → SDOUTn (Note 32)					
Delay time from SDINn to SDOUTn	tIOD			50	ns

Note 31. BITCLKn "↑" must not occur at the same time as LRCKn edge

Note 32. SDIN1 → SDOUT1: control register setting SELO1[1:0]= "11", OUT1E=1
SDIN2 → SDOUT2: control register setting SELO2[1:0]= "11", OUT2E=1
SDIN3 → SDOUT3: control register setting SELO3[1:0]= "11", OUT3E=1

■ Microcontroller Interface (I2CBUS Interface)

(Ta=-10°C ~70°C; AVDD=HVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; VSS1= VSS2 = VSS3=0V)

Parameter	Symbol	min	typ	max	Unit
I^2C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppress By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 33. I2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

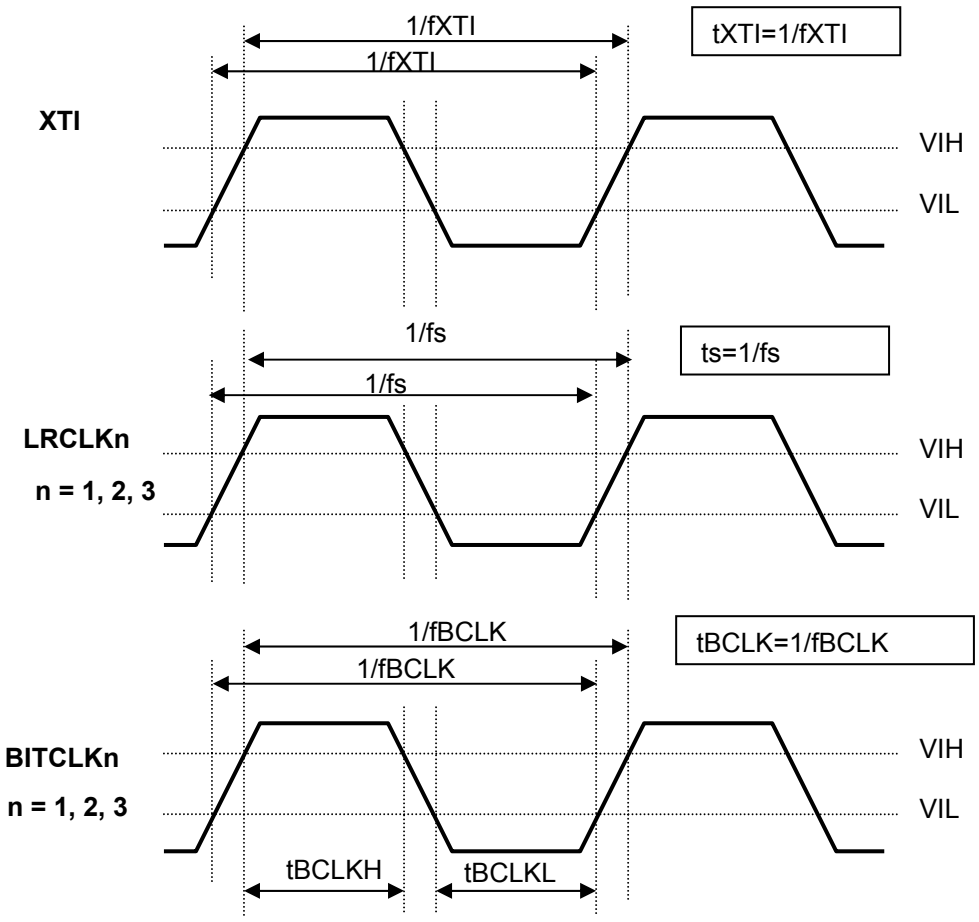


Figure 4. System Clock

INITRSTN

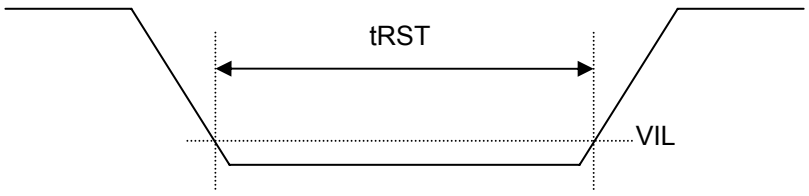


Figure 5. Reset

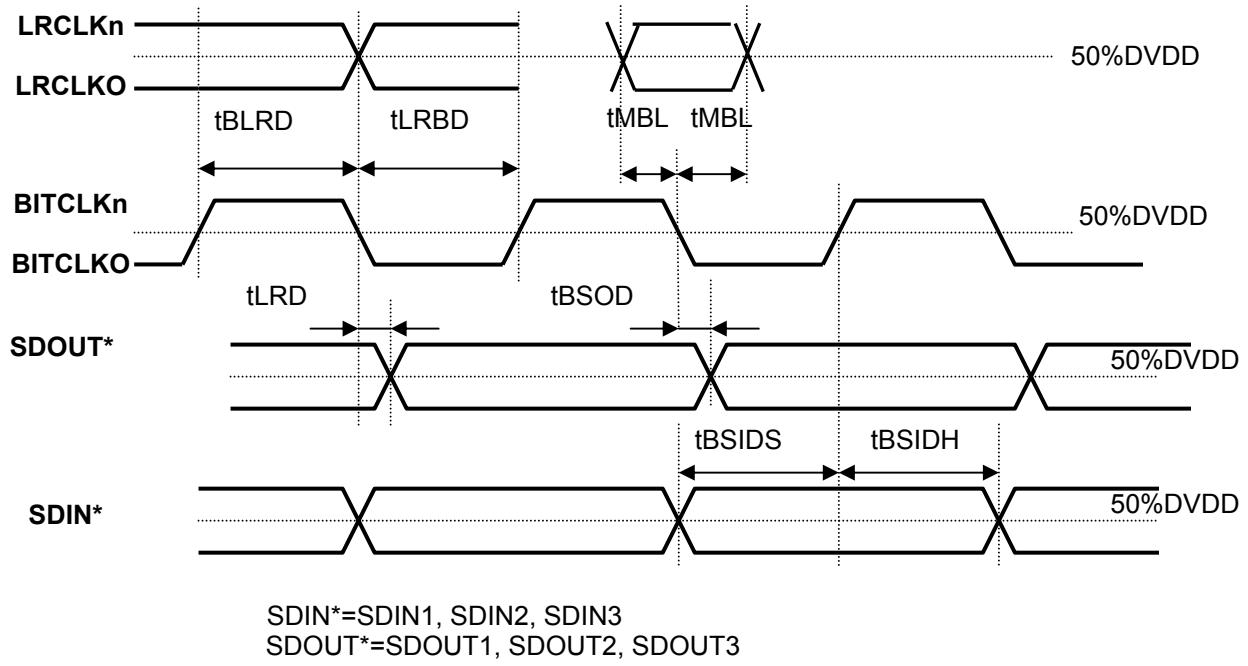


Figure 6. Audio System Interface

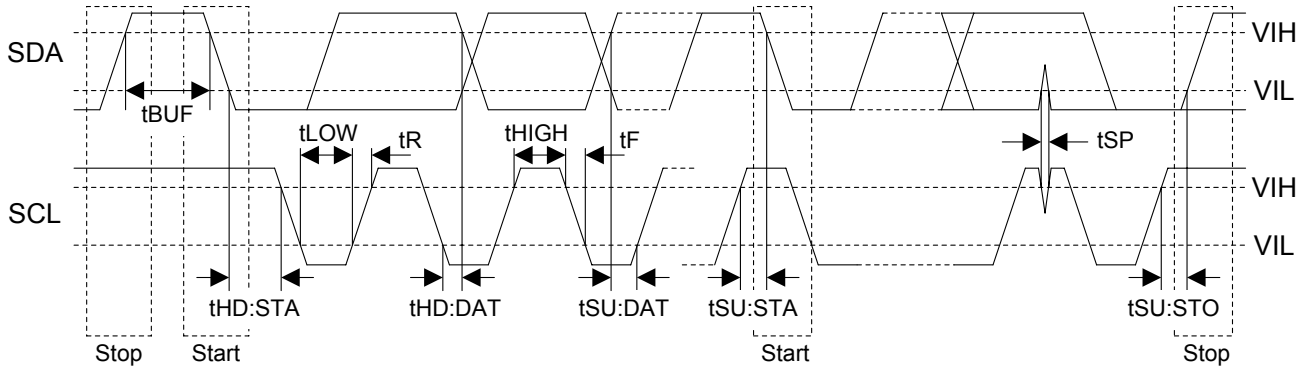
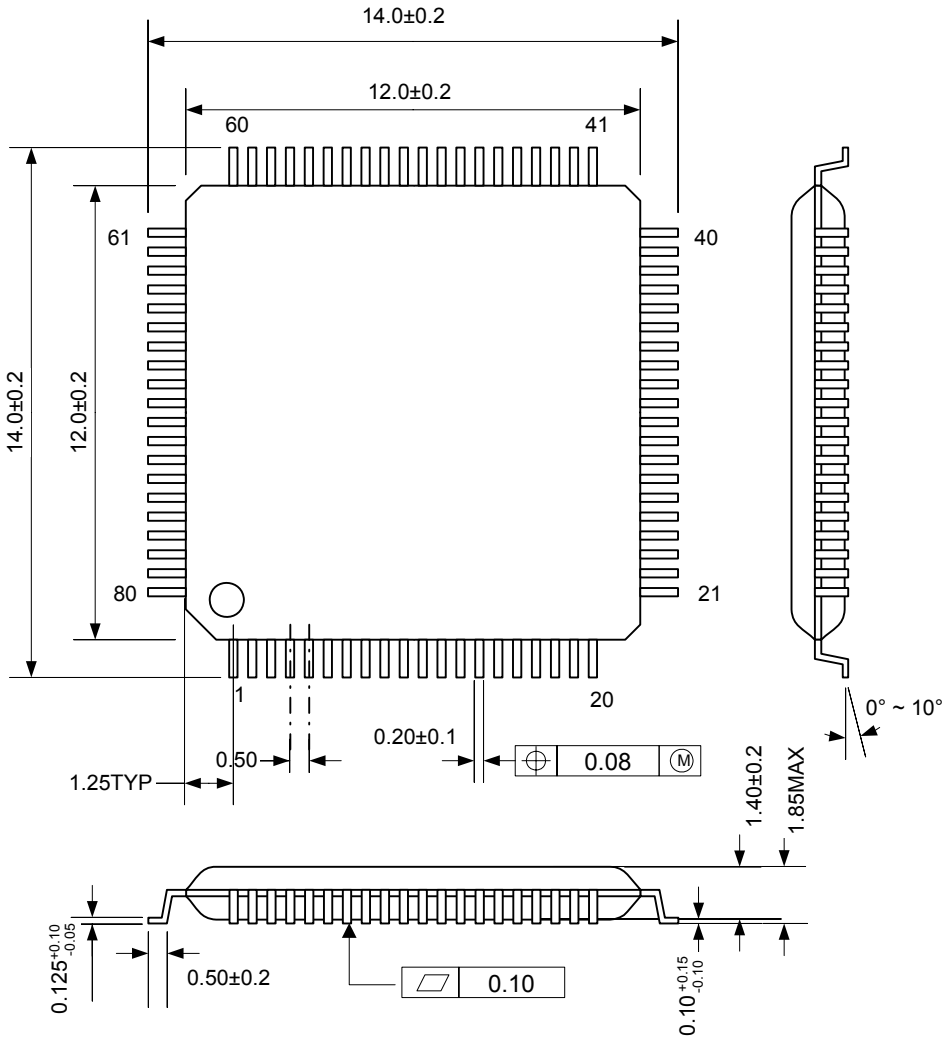


Figure 7. Microcontroller Interface (I^2C bus)

PACKAGE

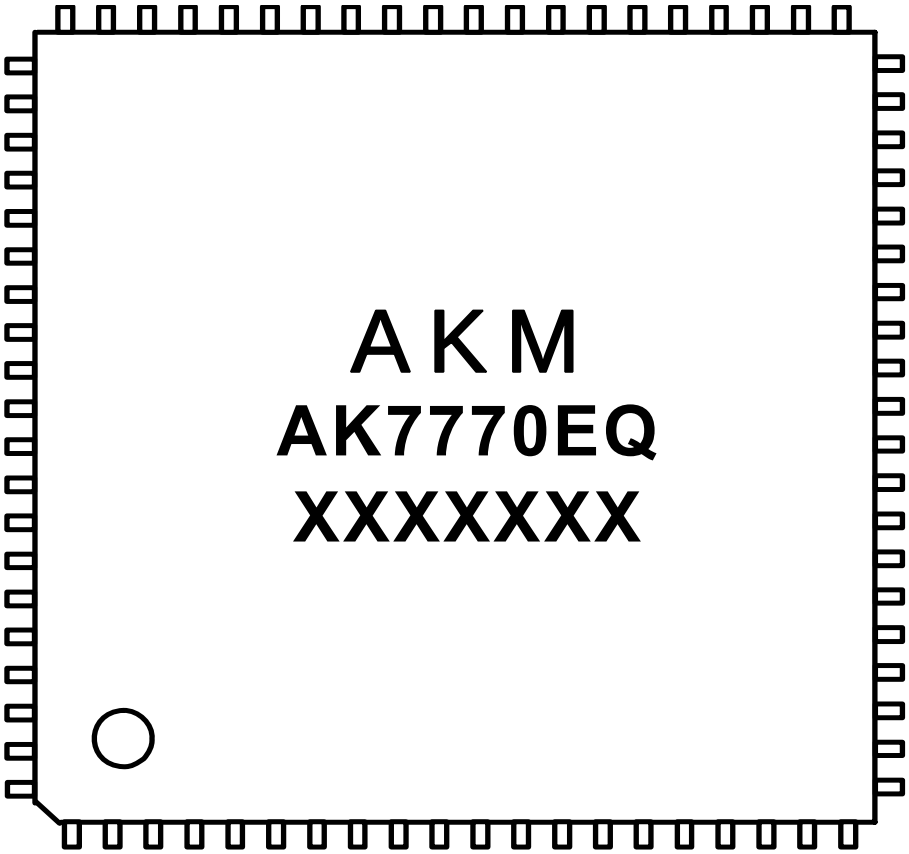
80-pin LQFP (Unit: mm)



■ Materials and lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering plate (Pb free)

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7digits)
3) Marking Code: AK7770EQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/01/08	00	First Edition		
08/06/24	01	Error Correct	15	SWITCHING CHARACTERISTICS ■System Clock CLK1, CLK2 Frequency; 11.0 → 2.0

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