Intel® Stratix® 10 Power Management User Guide

Updated for Intel® Quartus® Prime Design Suite: **21.1**

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UG-S10PWR

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Contents

1. Intel® Stratix® 10 Power Management Overview

The Intel® Stratix® 10 device family offers SmartVID standard power devices in all speed grades. Lower power fixed-voltage devices are also available in all speed grades except for the fastest speed grade.

Intel Stratix 10 devices also offer power gating feature to the digital signal processing (DSP) blocks and M20K memory blocks that are not in use for static power savings. You can implement this feature through the Intel Quartus® Prime software. This user guide describes power saving features of the Intel Stratix 10 device family, and also describes the power-up and power-down sequencing requirements for the Intel Stratix 10 devices.

Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- Intel Stratix 10 Device Datasheet

2. Intel Stratix 10 Power Management Architecture and Features

The following sections describe the power consumption, power reduction techniques, power sense line feature, power-on reset (POR) requirements, power-up and power-down sequencing requirements.

2.1. Power Consumption

The total power consumption of an Intel Stratix 10 device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating, excluding DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling.
- Standby power—the component of active power that is independent of signal activity or toggling. Standby power includes, but is not limited to, I/O and transceiver DC bias power.

2.1.1. Dynamic Power Equation

The following equation shows how to calculate dynamic power where P is power, C is the load capacitance, and V is the supply voltage level. The frequency refers to the clock frequency and data toggles once every clock cycle.

Figure 1. Dynamic Power Equation

$$P = \frac{1}{2} CV^2 \times frequency$$

The equation shows that power is design-dependent. Power is dependent on the operating frequency of your design, applied voltage, and load capacitance, which depends on design connectivity. Intel Stratix 10 devices minimize static and dynamic power using advanced process optimizations. These optimizations allow Intel Stratix 10 designs to meet specific performance requirements with the lowest possible power.

2.2. Power Reduction Techniques and Features

Intel Stratix 10 devices leverage on advanced 14-nm process technology, an enhanced core architecture, and various optimizations to reduce total power consumption. The power reduction techniques and features are listed below:

- SmartVID Standard Power Devices
- Power-Screened Devices
- Temperature Compensation
- DSP and M20K Power Gating
- Clock Gating
- Power Sense Line

2.2.1. SmartVID Standard Power Devices

The SmartVID feature compensates for process variation by narrowing the process distribution using voltage adaptation. This feature is supported in devices with the –V standard power option only. For the –V standard power option devices, you must connect the PWRMGT_SCL and PWRMGT_SDA pins in both the Power Management BUS (PMBus™) master and PMBus slave modes. An additional PWRMGT_ALERT pin is required when you configure the Intel Stratix 10 device in the PMBus slave mode. All connections required must be set up on the circuit board and in the Intel Quartus Prime software.

For more information about how to connect these pins on the circuit board, refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines*.

For instructions to set up the connection in the Intel Quartus Prime software, refer to the Specifying Parameters and Options on page 27.

Note: Intel Stratix 10 standard power devices (–1V, –2V, –3V power grade) are SmartVID devices. The core voltage supplies (V_{CC} and V_{CCP}) for each SmartVID device must be driven by a PMBus-compliant voltage regulator dedicated to the Intel Stratix 10 –V device that is connected to that Intel Stratix 10 device via PMBus. For Intel Stratix 10 standard power devices, use of a PMBus-compliant voltage regulator for each device is mandatory. Intel Stratix 10 devices will not configure or function correctly if the core voltage is driven by a non-PMBus compliant regulator with a fixed output voltage.

Intel programs the optimum voltage level required by each individual Intel Stratix 10 device into a fuse block during device manufacturing. The Secure Device Manager (SDM) Power Manager reads these values and can communicate them to an external power regulator or a system power controller through the PMBus interface.

The SmartVID feature allows a power regulator to provide the Intel Stratix 10 device with V_{CC} and V_{CCP} voltage levels that maintain the performance of the specific device speed grade. When the SmartVID feature is used:

1. Intel Stratix 10 devices are initially powered up to a nominal voltage level of 0.9V for both V_{CC} and V_{CCP}.
2. After the VID-fused value in the Intel Stratix 10 device is determined and propagated to the external voltage regulator, both the V_{CC} and V_{CCP} voltages are regulated based on the VID-fused value.

Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- Specifying Parameters and Options on page 27
- Intel Stratix 10 and Intel Agilex™ SmartVID Debug Checklist

2.2.1.1. SmartVID Feature Implementation in Intel Stratix 10 Devices

Devices supporting the SmartVID feature have a VID-fused value programmed into a fuse block during device manufacturing. The VID-fused value represents a voltage level in the range of 0.8V to 0.94V. Each device has its own specific VID-fused value.

The VID-fused value is sent to the external regulator or system power controller through the PMBus interface. Upon receiving the VID-fused value, an adjustable regulator tunes the V_{CC} and V_{CCP} voltage levels to the voltage specified by the VID-fused value.

Intel Stratix 10 devices perform the SmartVID setup in the early stage of the configuration process. The SmartVID process will continue to monitor the V_{CC} and V_{CCP} voltage rails in user mode. The Power Manager monitors the temperature and adjusts the voltage when required. For more information, refer to the Temperature Compensation section.

Table 1. SmartVID Regulator Requirements

Specification	Value
Voltage range	0.8 V – 0.94 V
Voltage step	10 mV
Ramp time	• Non-CvP—10 mV/10 ms to 10 mV/20 µs • Configuration via Protocol (CvP)—10 mV/60 µs to 10 mV/20 µs (1)

Table 2. Supported Voltage Output Format for Intel Stratix 10 Devices with the –V Power Option

Voltage Output Format	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
Linear mode	Yes	No
VID mode	No	No
Direct mode	Yes	Yes, with coefficient m=1, b=0, and R=0. Translated output voltage is in millivolts (mV).

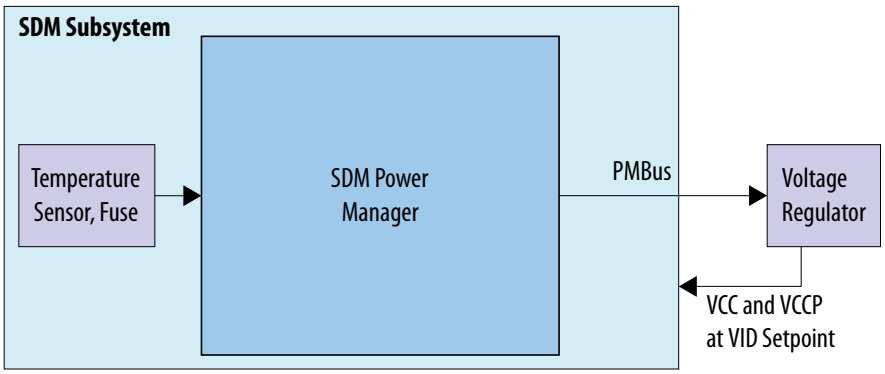
Related Information

- Temperature Compensation on page 14
- Recommended Operating Conditions
  Provides more information on the voltage range specifications.

(1) When the system is required to support the CvP functionality and meet the PCI Express* (PCIe*) link-up timing budget during the initial power up, the minimum ramp time is 10 mV/60 µs.

2.2.1.2. SDM Power Manager

Figure 2. SDM Power Manager Block Diagram



In Intel Stratix 10 devices, the SmartVID feature is managed by the SDM subsystem. The SDM subsystem is powered up after V_{CC} and V_{CCP} voltage levels are powered up to 0.9V. The SDM Power Manager reads the VID-fused value and communicates this value to the external voltage regulator through the PMBus interface.

The SDM Power Manager has the following stages:

- Initial stage
  - Sets the external voltage regulator to supply power to V_{CC} and V_{CCP} to the voltage level based on the VID-fused value and the device temperature.
  - Configures the FPGA and switches the FPGA to user mode.
- Monitor stage
  - Monitors temperature and updates the V_{CC} and V_{CCP}.

2.2.1.2.1. PMBus Master Mode

In the PMBus master mode, during the initial stage, the SDM Power Manager powers up the V_{CC} and V_{CCP} to the voltage level based on the VID-fused value and the device temperature before it starts to configure the FPGA. After entering the user mode (in the monitor stage), the SDM Power Manager monitors temperature changes and decides if the V_{CC} and V_{CCP} output voltage values need to be updated. If voltages require updating, the SDM Power Manager identifies the voltage value based on the fuse values and the current temperature and sends the desired voltage value to the voltage regulators through the PMBus (PWRMGT_SCL and PWRMGT_SDA).

Note: The PMBus mode only supports the 1.8-V I/O standard.

Figure 3. PMBus Master Mode

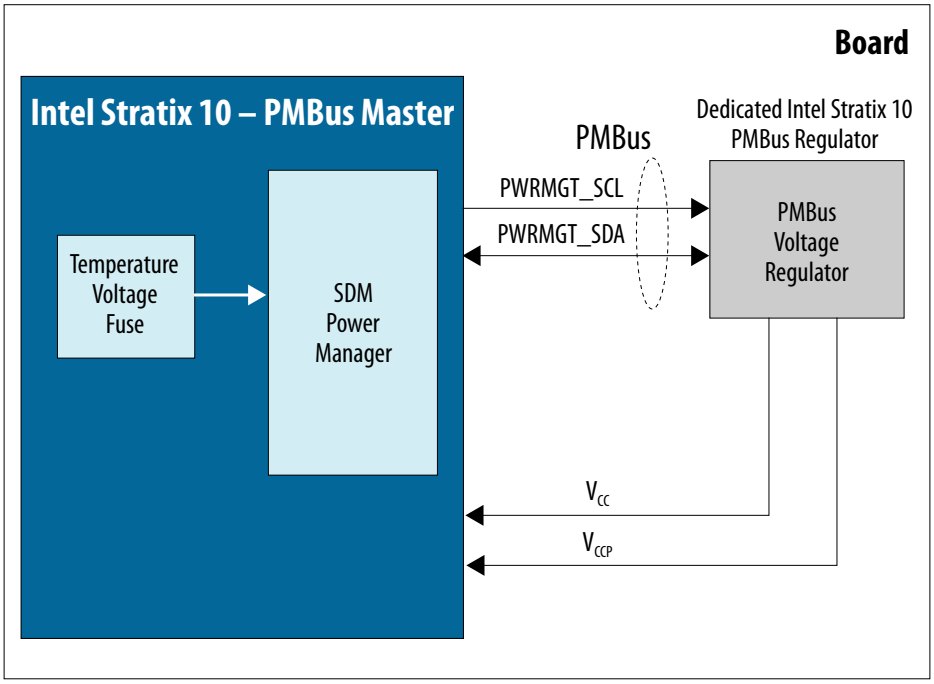


Table 3. Supported Commands for the PMBus Master Mode

Command Name	Command Code	PMBus Transaction Type	Number of Bytes
PAGE(2)	00h	Write byte	1
VOUT_MODE(3)	20h	Read byte	1
VOUT_COMMAND	21h	Write word	2
READ_VOUT	8Bh	Read word	2
MFR_ADC_CONTROL(4)	D8h	Write byte	1

Multi-Master Mode

The PMBus master mode supports the multi-master mode.

When multiple devices start to communicate at the same time, the device writing the most zeros to the bus or the slowest device wins the arbitration. The other devices immediately discontinue any operation on the bus. When there is an on-going bus communication, all devices must detect the communication and not interrupt it. The

(2) This is an optional command. This command is only applicable if you enable the PAGE command parameter. For more information, refer to the Power Management and VID Parameters section.

(3) This is an optional command. This command is only applicable if you select the Auto discovery in the voltage output format parameter. For more information, refer to the Power Management and VID Parameters section.

(4) This command is sent when you set the device type to LTM4677 only.

devices must wait for a stop condition to appear before starting communication to the bus. Once the stop condition is received on the bus, the next device that wins arbitration sends a start condition by pulling the PWRMGT_SDA low to re-initialize the bus communication.

In this mode, all master devices must be multi masters in a multi-master system. Single-master systems may not understand the arbitration and the busy detection mechanisms can cause unpredictable results.

Related Information

Power Management and VID Parameters on page 28

2.2.1.2.2. PMBus Slave Mode

Intel Stratix 10 devices can also be configured in the PMBus slave mode with an external power management controller acting as the PMBus master. When you configure the Intel Stratix 10 device in the PMBus slave mode, you must connect an additional PWRMGT_ALERT pin while connecting the existing PWRMGT_SCL and PWRMGT_SDA pins.

Note: The PMBus mode only supports the 1.8-V I/O standard.

The external PMBus master must poll the state of the PWRMGT_ALERT pin periodically, at an interval not longer than 100ms. When the PWRMGT_ALERT pin is asserted, the external master uses the Alert Response Address (ARA) flow to de-assert the ALERT signal and responds based on the STATUS_BYTE. The external master must also issue the VOUT_COMMAND every 200ms or less to check for a possible change in the target voltage due to temperature compensation.

Note: The same VOUT_COMMAND is used for reading the target voltage from the SDM or setting the voltage regulator to the new target voltage. When the Intel Stratix 10 device operates in the PMBus slave mode, the external master sends the VOUT_COMMAND to the SDM to get the target voltage required by the SDM. The external master then sends a VOUT_COMMAND to the voltage regulator to set its voltage.

Figure 4. PMBus Slave Mode

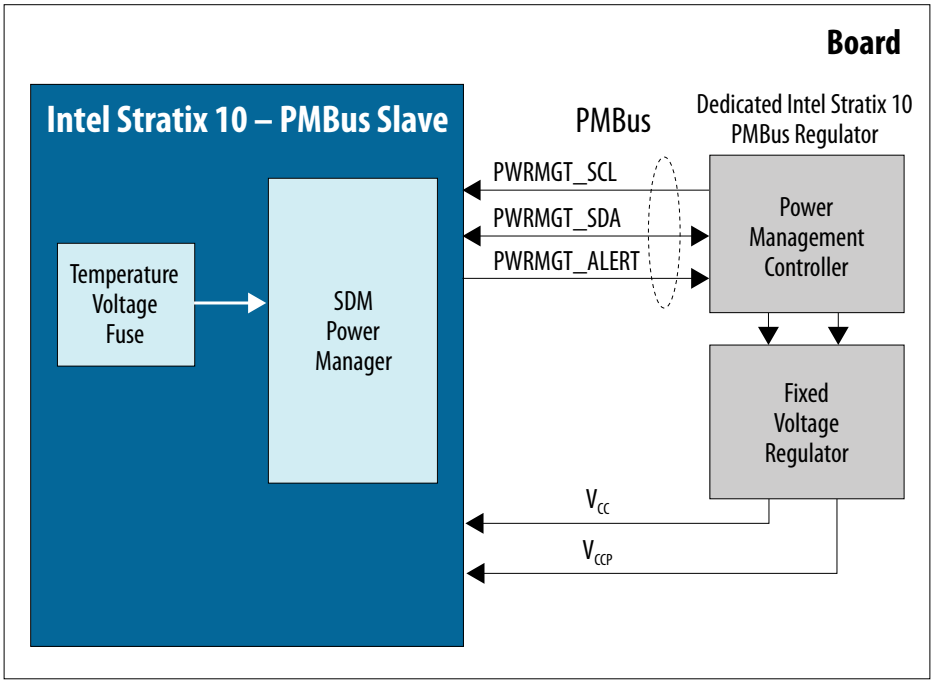
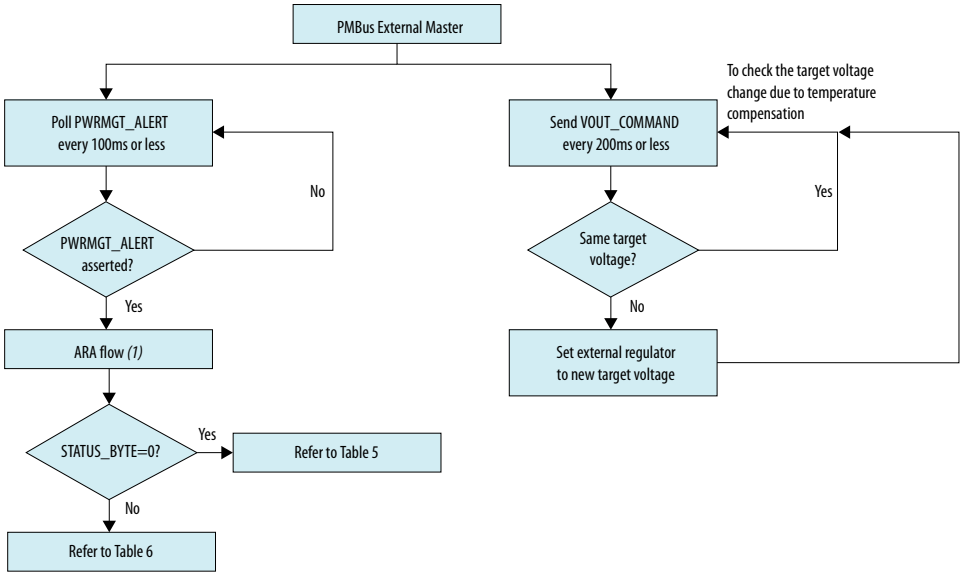


Table 4. Supported Commands for the PMBus Slave Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
CLEAR_FAULTS	03h	—	Send byte	0
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Read word	2
STATUS_BYTE	78h	00h	Read byte	1

Figure 5. External PMBus Master Software Flow



Note:

(1) When operating in the slave mode, the master and slave use the alert response address (ARA) flow to assert or de-assert the PWRMGT_ALERT signal.
The following are the details of the ARA flow:
(a) When operating in the slave mode, the slave device uses the ALERT signal to indicate the master device that an update is required.
(b) Upon reception of the ALERT signal, the external master device uses the ARA flow to determine which slave device has asserted the ALERT signal.
(c) The ARA flow is one-byte, broadcast read from the master device to the reserved SMBus Alert Response Address (0x0C).
(d) The slave device that has asserted the ALERT signal responds to this ARA flow with its address.
(e) The slave device de-asserts the ALERT signal after providing its address in step (4). The external master device uses the address provided to communicate with the correct slave device.

Table 5. Stage Flow for the External PMBus Master when the ALERT Signal is Asserted and STATUS_BYTE=0

Sequence	SDM	PMBus Master	Notes
1	Asserts the ALERT signal	—	—
2	—	Detects the ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the ALERT signal	—	The ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—
7	Returns STATUS_BYTE=0	—	Indicates the FPGA voltage requires an update.
8	—	Sends CLEAR_FAULTS	—
9	—	Sends VOUT_COMMAND	The VOUT_COMMAND must be received by the SDM within 200ms after the ALERT

continued...

Sequence	SDM	PMBus Master	Notes
			signal is asserted. Failure to meet this requirement will cause configuration error. (5)
10	Receives the VOUT_COMMAND, responds with the target voltage	—	Calculated based on the temperature, the VID fuse and the coefficient for the direct format (you need to specify this input).
11	—	Sets the voltage regulator to the target voltage in step size not greater than 10mV/ 10ms step	—

Table 6. Stage Flow for the External PMBus Master when the ALERT Signal is Asserted and STATUS_BYTE is not equal to 0

Sequence	SDM	PMBus Master	Notes
1	Asserts the ALERT signal	—	The SDM detects fault and asserts the ALERT signal. (6)
2	—	Detects the ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the ALERT signal	—	The ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—

continued...

(5) When there is an error triggered by the SDM because it did not receive the VOUT_COMMAND within the specified time, you must power cycle the device to recover from the error. If you do not power cycle the device to recover from the error, you will not be able to configure the device successfully.

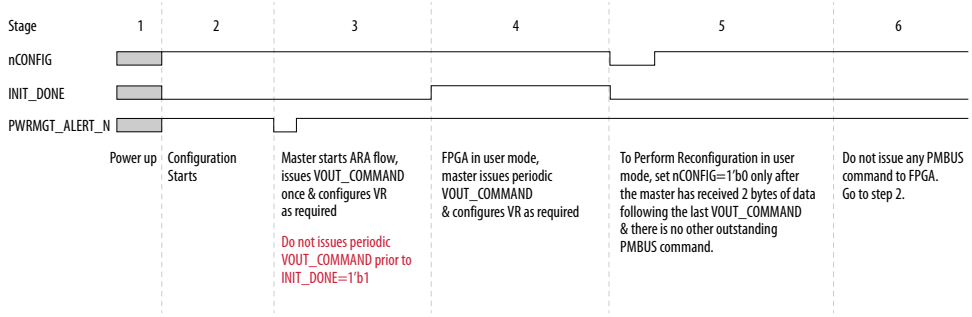
(6) The following faults can raise the ALERT signal:

- PMBUS_ERR_RD_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_WR_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_UNSUPPORTED_CMD (VOUT_COMMAND, VOUT_MODE, READ_STATUS, and CLEAR_FAULTS are the only supported commands in the PMBUS Slave Mode)
- PMBUS_ERR_READ_FLAG (Received duplicate command before being able to respond to the first command)
- PMBUS_ERR_INVALID_DATA (Invalid or malformed PMBus/I2C message)

If any of the above errors are detected, the ALERT signal is raised and bit 1 of the status register is set.

Sequence	SDM	PMBus Master	Notes
7	Returns the STATUS_BYTE when not equal to 0	—	Indicates that other fault has occurred
8	—	Sends CLEAR_FAULTS	To reset the STATUS_BYTE.
9	—	Reads the STATUS_BYTE	To confirm that STATUS_BYTE=0
10	—	External master to handle the faults	—

Figure 6. Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram



The Intel Stratix 10 device in the PMBus slave mode will be sending the VOUT_COMMAND value in the direct format only. To read the actual voltage value, use the following equation to convert the VOUT_COMMAND value from the Intel Stratix 10 device.

Figure 7. Direct Format Equation

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right)$$

The equation shows how to convert the direct format value where:

- X, is the calculated, real value units in mV;
- m, is the slope coefficient, a 2-byte two's complement integer;
- Y, is the 2-byte two's complement integer received from the Intel Stratix 10 device;
- b, is the offset, a 2-byte two's complement integer;
- R, is the exponent, a 1-byte two's complement integer

The following example shows how an external power management controller retrieves values from the Intel Stratix 10 device. Coefficients used in the VOUT_COMMAND are as follows:

- m = 1
- b = 0
- R = 0

If the external power management controller retrieved a value of 0384h, it is equivalent to the following:

$X = (1/1) \times (0384h \times 10^{-0} - 0) = 900\ mV = 0.90\ V$

2.2.2. Power-Screened Devices

Intel Stratix 10 power-screened devices are available in –2L and –3X options. Power-screened devices offer lower static power than the SmartVID –V power option devices. The –2L and –3X power-screened devices run at a fixed-voltage supply and do not require using the PMBus regulator.

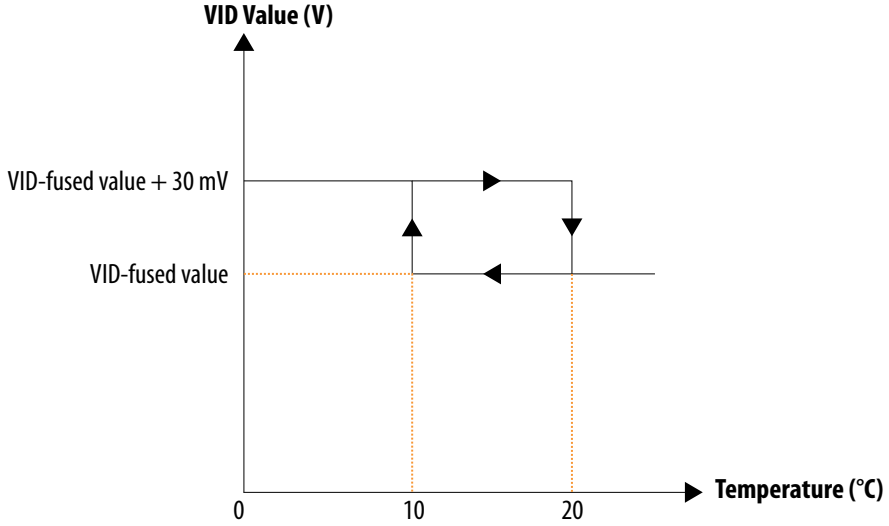
2.2.3. Temperature Compensation

Intel Stratix 10 devices are able to compensate for performance degradation at colder temperatures by raising the voltage. While raising the voltage does increase the dynamic power consumption, this is countered by lower leakage at cold temperatures, thus enabling total power consumption at cold temperatures to still be lower than at hot temperatures.

The SmartVID feature supports this dynamic voltage adjustment. The SDM Power Manager checks for temperature changes and updates the new VID value if the temperature crosses the threshold point.

Figure 8. Temperature Compensation for SmartVID for Intel Stratix 10 Devices—Preliminary

The SDM monitors the temperature, normally at every 100 ms, and adjusts the voltage by communicating with an external power management system. Adjustment is made by the SDM after the sensor detects the temperature setting is below 10 °C or above 20 °C.



The following shows the process when there is a change in the VID value:

- If the Intel Stratix 10 device operates as the PMBus master, the SDM sends the relevant commands to adjust the voltage of the external voltage regulator using the new VID value.
- If the Intel Stratix 10 device operates as the PMBus slave, the external power management controller gets the new VID value with the VOUT_COMMAND which is issued every 200 ms or less, and set the voltage regulator with the new VID value.

2.2.4. DSP and M20K Power Gating

Power gating of the DSP blocks and M20K memory blocks is enabled via the configuration RAM (CRAM) bits. Intel Stratix 10 devices support power gating for both DSP blocks and M20K memory blocks. By default, the Intel Quartus Prime software automatically configures unused DSP blocks and M20K memory blocks to be power gated.

2.2.5. Clock Gating

Clock gating can be used to reduce dynamic power consumption. When an application is idle, its clock can be gated temporarily and ungated based on wake-up events. This is done using user logic to enable or disable the global clock (GCLK) and sector clock (SCLK).

You can perform dynamic power reduction by gating the clock signals of any circuitry not used by the design in the Intel Stratix 10 devices.

Clock networks can be gated using one of the following methods:

Root Clock Gate

You can dynamically gate each clock network at the root level using the Clock Control Intel FPGA IP core.

Sector Clock Gate

You can dynamically gate each clock network at the clock sector level using the Clock Control Intel FPGA IP core.

I/O PLL Clock Gate

You can dynamically gate each output counter of the Intel Stratix 10 I/O PLL's using IOPLL reconfiguration.

Clock gating a large portion of your FPGA design could cause significant current change over a short time period when the gated circuitry is enabled or disabled. The maximum current step resulting from this clock gating should be sized such that it does not create noise exceeding the maximum allowed AC noise specification, as determined by the PDN decoupling design on your PCB. You can control the current step size by dividing a large gated area into smaller sub-regions and staging those regions to enter or exit power gating sequentially.

For more details, refer to the *Clock Gating* section in the *Intel Stratix 10 Clocking and PLL User Guide*.

2.2.6. Power Sense Line

Intel Stratix 10 devices support the power sense line feature. VCCLSENSE and GNDSENSE pins are differential remote sense pins used to monitor the V_{CC} power supply.

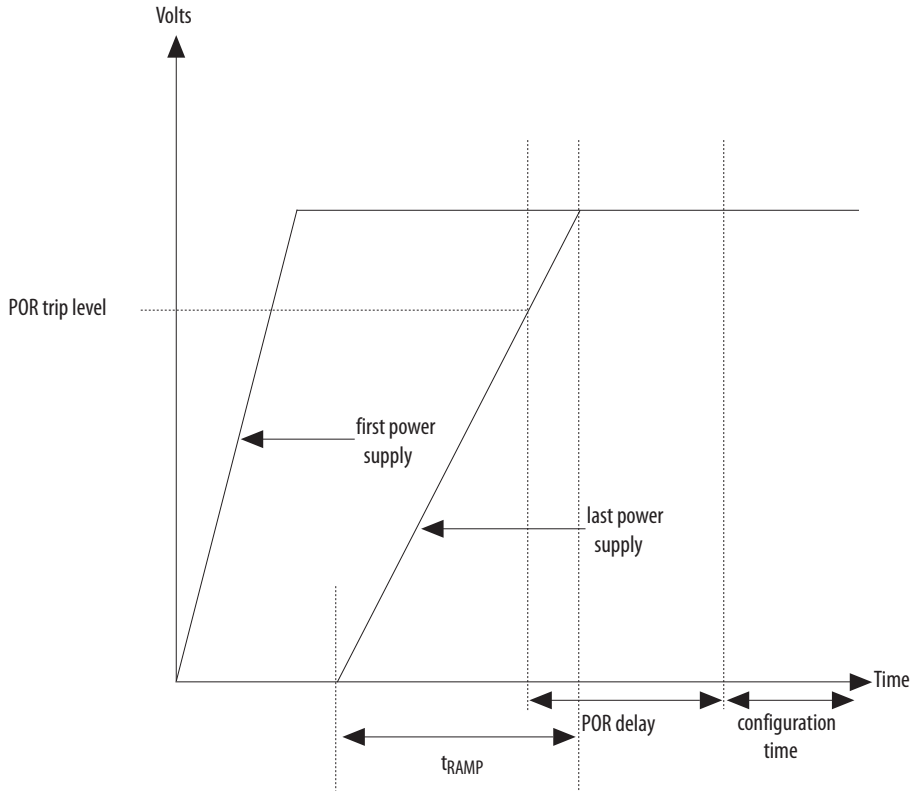
You must connect the VCCLSENSE and GNDSENSE pins to the remote sense inputs for all regulators that support the remote voltage sensing feature.

2.3. Power-On Reset Circuitry

The POR circuitry keeps the Intel Stratix 10 device in the reset state until the power supply outputs are within the recommended operating range.

A POR event occurs when you power up the Intel Stratix 10 device until all power supplies monitored by the POR circuitry reach the recommended operating range within the maximum power supply ramp time, t_{RAMP}. If t_{RAMP} is not met, the Intel Stratix 10 device I/O pins and programming registers remain tri-stated, which may cause device configuration to fail.

Figure 9. Relationship Between t_{RAMP} and POR Delay



The Intel Stratix 10 POR circuitry uses individual detection circuitry to monitor each of the configuration-related power supplies independently. The POR circuitry is gated by the outputs of all the individual detectors.

POR delay is the time from when the POR trips out to the final reset signal.

The Intel Stratix 10 device is held in the POR state until all power supplies have passed their trigger point. After power supplies have passed the trigger point, the SDM will wait for a configurable delay time and then start device configuration.

2.3.1. Power Supplies Monitored and Not Monitored by the POR Circuitry

Table 7. Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry

Power Supplies Monitored	Power Supplies Not Monitored
• V_{CC} • V_{CCERAM} • V_{CCPT} • V_{CCADC} • V_{CCIO_SDM} • V_{CCBAT} • V_{CCL_HPS} (7) • V_{CCFUSE_GXP} (8)	• V_{CCP} • V_{CCR_GXB} • V_{CCT_GXB} • V_{CCH_GXB} • V_{CCIO} • V_{CCIO_HPS} (7) • V_{CCA_PLL} • $V_{CCFUSEWR\_SDM}$ • $V_{CCPLLDIG\_SDM}$ • $V_{CCPLLDIG\_HPS}$ (7) • V_{CCPLL_HPS} (7) • V_{CCPLL_SDM} • V_{CCM_WORD} • V_{CCIO_UIB} • V_{CCRT_GXE} • $V_{CCRTPLL\_GXE}$ • V_{CCIO3V} • V_{CCH_GXE} • V_{CCCLK_GXE} • V_{CCRT_GXP} • V_{CCH_GXP} • V_{CCCLK_GXP} • V_{CCIO3D} (9) • V_{CCIO3C} (9)

Note: Intel recommends you to connect V_{CCBAT} to a 1.8V power supply if you do not use the design security feature in Intel Stratix 10 devices.

2.4. Power Sequencing Considerations for Intel Stratix 10 Devices

The Intel Stratix 10 devices require a specific power-up and power-down sequence. This section describes several power management options and discusses proper I/O management during device power-up and power-down. Design your power supply solution to properly control the complete power sequence.

(7) These are only supported by system-on-a-chip (SoC) FPGA.

(8) This power rail will not gate SDM power up, but it will gate FPGA configuration.

(9) Applies to the 1SG040 and 1SX040 devices only.

The requirements in this section must be followed to prevent unpredictable current draw to the FPGA device, which can potentially impact the I/O functionality. Intel Stratix 10 devices do not support 'Hot-Socketing' except under the conditions stated in the table below. The table below also shows what the unpowered pins can tolerate during power-up and power-down sequences.

The I/O pins are tri-stated with a weak pull-up during power up.

Table 8. Pin Tolerance—Power-Up/Power-Down

'√' is Applicable; '—' is Not Applicable.

Pin Type	Power-Up				Power-Down			
	Tristate	Drive to GND	Drive to VCCIO	Driven with < 1.0 Vp-p	Tristate	Drive to GND	Drive to VCCIO	Driven with < 1.0 Vp-p
3VIO banks	√	—	—	—	√	√	—	—
LVDS I/O banks	√	√	√(10)	—	√	√	√(10)	—
Differential Transceiver pins	√	√	—	√(11)	√	√	—	√(11)

Related Information

- LVDS I/O Pin Guidance for Unpowered FPGA
- Transceiver Pin Guidance for Unpowered FPGA

2.4.1. Power-Up Sequence Requirements for Intel Stratix 10 Devices

Note: To satisfy the power-up requirements, program the FPGA device immediately after the power-up sequence completes.

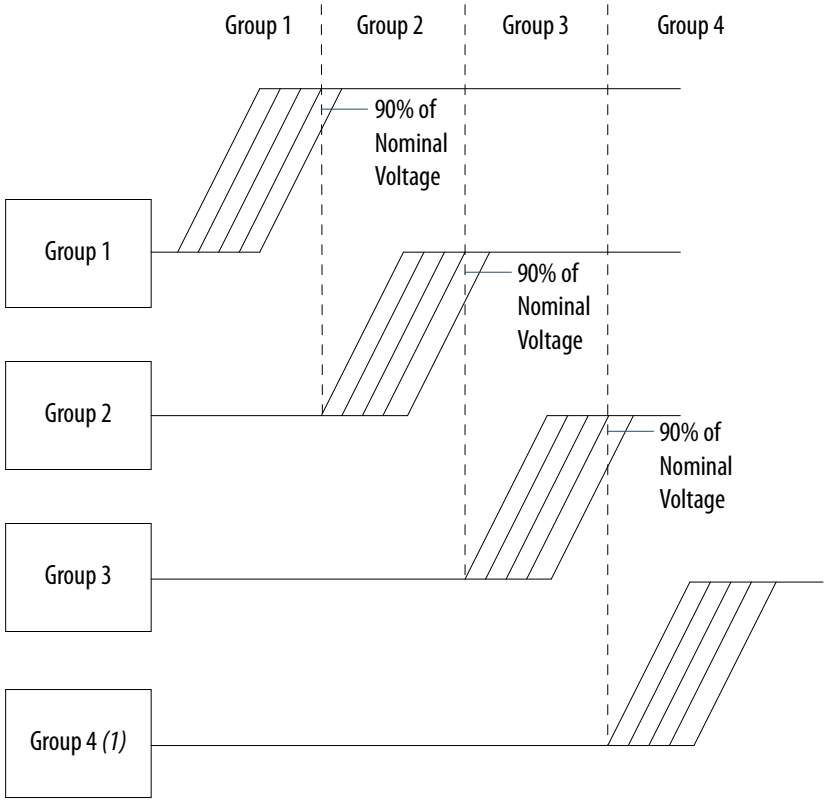
The power rails in Intel Stratix 10 devices are each divided into three groups. Refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines* and *AN692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix 10 Devices* for additional details.

The diagram below illustrates the voltage groups of the Intel Stratix 10 devices and their required power-up sequence.

(10) The maximum current allowed through any LVDS I/O bank pin when the device is unpowered or during power up/down conditions = 10 mA (refer to "LVDS I/O Pin Guidance for Unpowered FPGA Pins").

(11) This applies to Intel Stratix 10 L-Tile/H-Tile only (refer to "Transceiver Pin Guidance for Unpowered FPGA Transceiver Pins").

Figure 10. Power-Up Sequence for Intel Stratix 10 Devices



Note:
(1) Applies to the 1SG040 and 1SX040 devices only.

Note: VCCBAT is not in any of the groups below. VCCBAT does not have any sequence requirements. VCCBAT holds the contents of the security keys.

Table 9. Voltage Rails

Power Group	Intel Stratix 10 GX and SX (L-Tile and H-Tile)	Intel Stratix 10 MX (HBM, H-Tile, and E-Tile)	Intel Stratix 10 TX (H-Tile and E-Tile)	Intel Stratix 10 DX (E-Tile and P-Tile)
Group 1	V_{CC} V_{CCP} V_{CCERAM} V_{CCR_GXB} V_{CCT_GXB} V_{CCL_HPS} $V_{CCPLLDIG\_SDM}$ $V_{CCPLLDIG\_HPS}$	V_{CC} V_{CCP} V_{CCERAM} V_{CCR_GXB} V_{CCT_GXB} $V_{CCPLLDIG\_SDM}$ V_{CCRT_GXE} $V_{CCRTPLL\_GXE}$	V_{CC} V_{CCP} V_{CCERAM} V_{CCR_GXB} V_{CCT_GXB} V_{CCL_HPS} $V_{CCPLLDIG\_SDM}$ $V_{CCPLLDIG\_HPS}$ V_{CCRT_GXE}	V_{CC} V_{CCP} V_{CCERAM} V_{CCFUSE_GXP} (12) V_{CCRT_GXP} V_{CCL_HPS} $V_{CCPLLDIG\_SDM}$ $V_{CCPLLDIG\_HPS}$ V_{CCRT_GXE}

continued...

(12) You must always connect VCCFUSE_GXP to VCCERAM on your board.

Power Group	Intel Stratix 10 GX and SX (L-Tile and H-Tile)	Intel Stratix 10 MX (HBM, H-Tile, and E-Tile)	Intel Stratix 10 TX (H-Tile and E-Tile)	Intel Stratix 10 DX (E-Tile and P-Tile)
			$V_{CCRTPLL\_GXE}$	$V_{CCRTPLL\_GXE}$
Group 2	V_{CCPT} V_{CCH_GXB} V_{CCA_PLL} V_{CCPLL_HPS} V_{CCPLL_SDM} V_{CCADC}	V_{CCPT} V_{CCH_GXB} V_{CCA_PLL} V_{CCPLL_SDM} V_{CCADC} V_{CCM_WORD} (13) V_{CCH_GXE} V_{CCCLK_GXE}	V_{CCPT} V_{CCH_GXB} V_{CCA_PLL} V_{CCPLL_HPS} V_{CCPLL_SDM} V_{CCADC} V_{CCH_GXE} V_{CCCLK_GXE}	V_{CCPT} V_{CCA_PLL} V_{CCPLL_HPS} V_{CCPLL_SDM} V_{CCADC} V_{CCM_WORD} (13) V_{CCH_GXP} V_{CCCLK_GXP} V_{CCH_GXE} V_{CCCLK_GXE}
Group 3	V_{CCIO} (14) V_{CCIO3V} (14) V_{CCIO_SDM} (14) V_{CCIO_HPS} (14) $V_{CCFUSEWR\_SDM}$ V_{CCIO3D} (15)	V_{CCIO} V_{CCIO3V} V_{CCIO_SDM} V_{CCIO_UIB} (13) $V_{CCFUSEWR\_SDM}$	V_{CCIO} V_{CCIO3V} V_{CCIO_SDM} V_{CCIO_HPS} $V_{CCFUSEWR\_SDM}$	V_{CCIO} V_{CCIO_SDM} V_{CCIO_HPS} V_{CCIO_UIB} (13) $V_{CCFUSEWR\_SDM}$
Group 4	V_{CCIO3C} (15)	—	—	—

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up.

The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3 power rails can start ramping up.

The power rails within Group 3 can ramp up in any order after the last power rail in Group 2 ramps up to a minimum threshold of 90% of their full value.

Group 4 power rails can ramp up after the last power rail in Group 3 ramps up to a minimum threshold of 90% of their full value.

Note: E-tile devices must maintain the voltage rail groupings for the power-up sequencing as listed in the table above. V_{CCCLK_GXE} must be powered up before V_{CCIO_SDM}.

Note: For 1SG040 and 1SX040 devices, VCCIO_3D must be powered up before VCCIO_3C.

Note: Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.

(13) Applies to Intel Stratix 10 MX and DX devices only.

(14) For Intel Stratix 10 GX and SX devices, these power rails can be combined and shared using the same voltage regulator as the Group 2 power rail V_{CCPT} if all their voltages are 1.8V.

(15) Applies to the 1SG040 and 1SX040 devices only.

All power rails must ramp up monotonically. The power-up sequence should meet either the standard or the fast POR delay time. The POR delay time depends on the POR delay setting you use. For the POR specifications of the Intel Stratix 10 devices, refer to the POR Specifications section in the *Intel Stratix 10 Device Datasheet* .

For configuration via protocol (CvP), the total t_{RAMP} must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. Select a fast POR delay setting to allow sufficient time for the PCI Express (PCIe) link initialization and configuration. For more details about power supply ramp up for the CvP mode, refer to the *Intel Stratix 10 Configuration via Protocol (CvP) Implementation User Guide*.

Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- AN692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
- POR Specifications
- Intel Stratix 10 Configuration via Protocol (CvP) Implementation User Guide

2.4.2. Power-Down Sequence Recommendations and Requirements for Intel Stratix 10 Devices

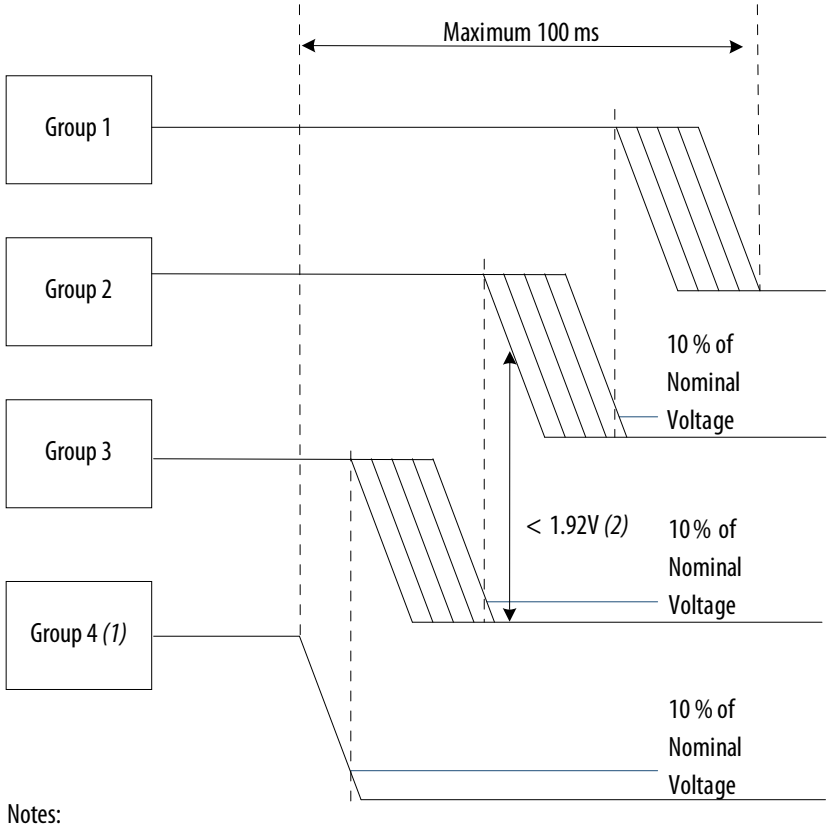
Intel's FPGAs need to follow certain requirements during a power-down sequence. The power-down sequence can be a controlled power-down event via an on/off switch or an uncontrolled event as with a power supply collapse. In either case, you must follow a specific power-down sequence. Below are four power-down sequence specifications. They are either Recommended (one), Required (two), or Relaxed (one). To comply with Intel's FPGA Power-Down requirements, the Recommended option is best.

Note: If you cannot follow the Recommended specification, you must follow the Required specification.

Recommended Power-Down Ramp Specification

This is the best option to minimize power supply currents.

Figure 11. Recommended Power-Down Ramp Specification



Notes:
(1) Applies to the 1SG040 and 1SX040 devices only.
(2) Only applicable for the 1.8V voltage rails in Group 2.

- Power down all power rails fully within 100 ms.
- Power down power supplies within the same Group in any order.
- Before Group 3 supplies power down, power down all Group 4 supplies within 10% of GND.
- Before Group 2 supplies power down, power down all Group 3 supplies within 10% of GND.
- Before Group 1 supplies power down, power down all Group 2 supplies within 10% of GND.
- The maximum voltage differential between any Group 3 supply and any Group 2 supply is 1.92 V, and only applicable for the 1.8V voltage rails in Group 2.

For Intel Stratix 10 GX and SX devices, you can combine and ramp down Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as the Group 2 power rails.

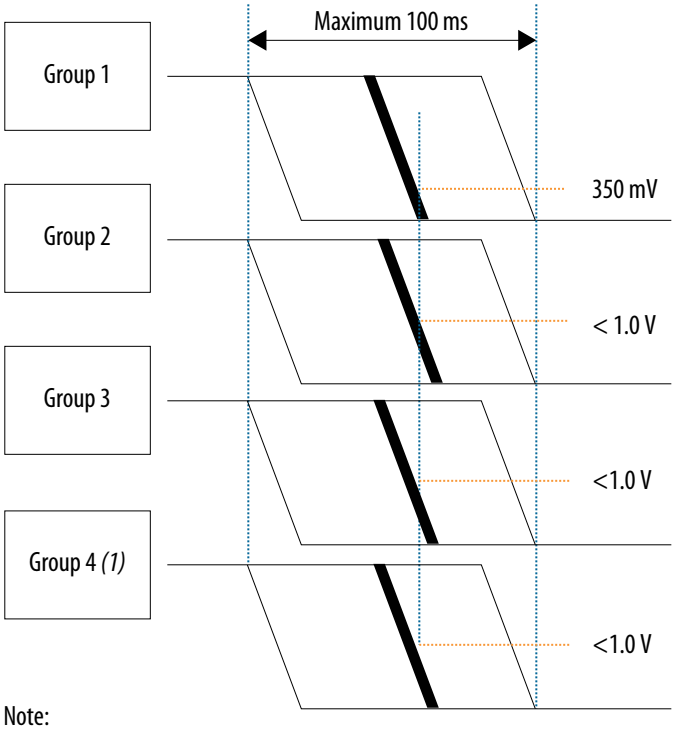
- Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.
- Ensure that the newly combined power rails do not violate any power-down sequencing specification due to device (third party) leakage; maintain the Required Voltage Differential Specification.

During the power-up/down sequence, the device output pins are tri-stated. To ensure long term reliability of the device, Intel recommends that you do not drive the input pins during this time.

Required Power-Down Ramp Specification

In cases where power supply is collapsing or if the recommended specification cannot be met, the following PDS sequence is required.

Figure 12. Required Power-Down Ramp Specification



Note:
(1) Applies to the 1SG040 and 1SX040 devices only.

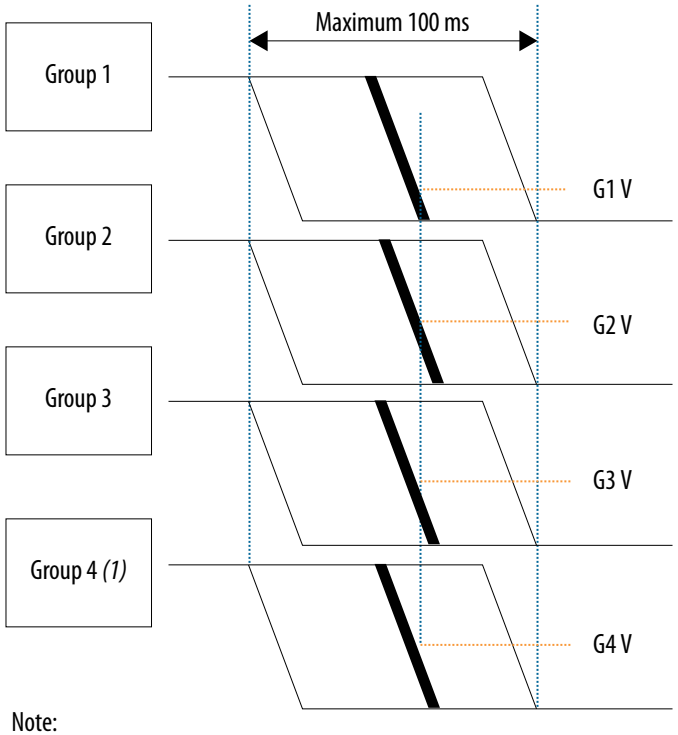
- Power down all power rails fully within 100 ms.
- As soon as possible, disable all power supplies.
  - Tri-state Group 1 supplies, and do not drive them actively to GND.
  - If possible, drive or terminate Group 2, Group 3, and Group 4 supplies to GND.
- Ensure no alternative sourcing of any power supply exists during the power-down sequence; reduce all supplies monotonically and with a consistent RC typical decay.
- By the time any Group 1 supply goes under 0.35 V, all Group 2, Group 3, and Group 4 supplies must be under 1.0 V.

Required Voltage Differential Specification

To not excessively overstress device transistors during power-down, there is an additional voltage requirement between any two power supplies between different power groups during power-down:

$\Delta V < \Delta V_{nom} + 500$ mV

Figure 13. Required Voltage Differential Specification



Note:
(1) Applies to the 1SG040 and 1SX040 devices only.

- Power down all power rails fully within 100 ms.
- For example, if Group 1 Voltage = 0.9 V, Group 2 Voltage = 1.8 V, and Group 3 Voltage = 3.0 V, then:

$G3V_{nom}$ = 3.0 V $G2V_{nom}$ = 1.8 V	$G2V_{nom}$ = 1.8 V $G1V_{nom}$ = 0.9 V	$G3V_{nom}$ = 3.0 V $G1V_{nom}$ = 0.9 V
$(G3V - G2V)_{nom}$ = 1.2 V	$(G2V - G1V)_{nom}$ = 0.9 V	$(G3V - G1V)_{nom}$ = 2.1 V
(G3V – G2V) <= 1.2 V + .5 V	(G2V – G1V) <= 0.9 V + .5 V	(G3V – G1V) <= 2.1 V + .5 V
(G3V – G2V) <= 1.7 V	(G2V – G1V) <= 1.4 V	(G3V – G1V) <= 2.6 V

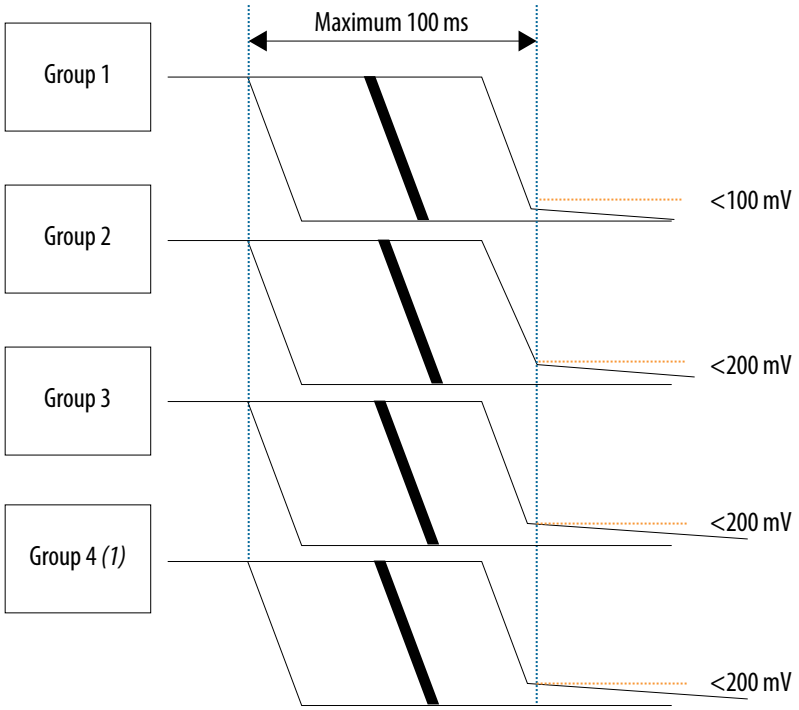
- To meet this voltage differential requirement, ramp down all power supplies as soon as possible according to the Required Power-Down Ramp Specification.

Note: Not following the required power sequence can result in unpredictable device operation and internal high current paths.

Relaxed Power-Down Duration Specification

For supplies being powered down with no active termination, voltage reduction to GND slows down as supply approaches 0 V. In this case, the 100 ms power requirement is relaxed - measure it when supply reaches near GND.

Figure 14. Relaxed Power-Down Duration Specification



Note:
(1) Applies to the 1SG040 and 1SX040 devices only.

- Ensure all Group 1 supplies reach < 100 mV within 100 ms.
- Ensure all Group 2, Group 3, and Group 4 supplies reach < 200 mV within 100 ms.

Related Information

AN692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

2.5. Power Supply Design

The power supply requirements for Intel Stratix 10 devices will vary depending on the static and dynamic power for each specific use case.

Intel Stratix 10 devices have multiple input voltage rails that require regulated power supplies for their operation. Multiple input rail requirements may be grouped according to system considerations such as voltage requirements, noise sensitivity, and sequencing. The *Intel Stratix 10 Device Family Pin Connection Guidelines* provides more detailed recommendations about which input rails may be grouped. The Intel FPGA Power and Thermal Calculator (PTC) for Intel Stratix 10 devices also provides

input rail power requirements and specific device recommendations based on each specific Intel Stratix 10 use case. Individual input rail voltage, current requirements, and input rail groupings are summarized on the “Report” tab.

Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- Intel FPGA Power and Thermal Calculator User Guide
- Intel FPGA Power and Thermal Calculator Standalone
  Provides standalone Intel FPGA Power and Thermal Calculator tool

3. Intel Stratix 10 Power Management and VID Interface Implementation Guide

The Intel Stratix 10 SDM Power Management Firmware manages the SmartVID configuration and enables the FPGA to power up before you can access the FPGA core.

3.1. Intel Stratix 10 Power Management and VID Interface Getting Started

The Intel Stratix 10 Power Management and VID interface is installed as part of the Intel Quartus Prime software.

3.1.1. Specifying Parameters and Options

Follow these steps to specify the **Power Management and VID** parameters and options.

1. Create an Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Assignments** menu, click **Device**.
3. On the **Device** dialog box, click **Device and Pin Options**.
4. On the **Device and Pin Options** dialog box, click **Configuration**.
5. On the **Configuration** page, specify the **VID Operation mode**. There are two modes available—PMBus Master and PMBus Slave.
6. Both the PMBus Master and PMBus Slave modes require the PWMGT_SDA and PWMGT_SCL pins. For the PMBus Slave mode, additional PWRMGT_ALERT pin is required. To configure these pins, on the **Configuration** page, click **Configuration Pin Options**. For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*.
7. On the **Configuration Pin** dialog box, assign the appropriate SDM_IO pin to the power management pins. Click **OK**.
8. On the **Device and Pin Options** dialog box, click **Power Management and VID** to specify the device settings if your device is in the PMBus Master mode. Click **OK**. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

This completes the SmartVID setup for the Intel Stratix 10 device.

3.1.1.1. Configuration Pin Parameters

You can configure the following power management pins using the GUI parameters.

Table 10. Configuration Pin Parameters

Parameters	Value	Description
Use PWRMGT_SCL output	SDM_IO0 SDM_IO14	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO14 pin for this parameter.
Use PWRMGT_SDA output	SDM_IO11 SDM_IO12 SDM_IO16	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO11 pin for this parameter.
Use PWRMGT_ALERT output	SDM_IO0 SDM_IO9 SDM_IO12	This is a required PMBus interface for the power management that is used only in the PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO12 pin for this parameter. This parameter is an active-low signal.

Related Information

- SDM Pin Mapping
  Provides more information on the configuration functions for each SDM pin.
- Secure Device Manager (SDM) Pins
  Provides more information on the pin description and connection guidelines for each SDM pin.

3.1.1.2. Power Management and VID Parameters

You can use the GUI parameters to configure the Power Management and VID interface if the VID operation is in the PMBus Master mode.

Table 11. Power Management and VID Parameters

Parameters	Value	Description
Bus speed mode(16)	100 KHz 400 KHz	Bus speed mode of PMBus interface when operating in the PMBus Master mode.
Slave device type(16)	LTM4677 Other	Supported device types. Intel recommends you to use one of the slave device type listed in the drop-down menu that has been tested with the Intel FPGA tools. If you are not using one of the slave device type listed in the drop-down menu, select **Other** option. When you select **Other**

continued...

(16) This parameter is used for the PMBus Master mode.

Parameters	Value	Description
		option, refer to Table: *SmartVID Regulator Requirements*, Table: *Supported Voltage Output Format for Intel Stratix 10 Devices with the –V Power Option*, and Table: *Supported Commands for the PMBus Master Mode* for the voltage regulator requirements details.
Device address in PMBus Slave mode(17)	7-bit hexadecimal value	Device address in the PMBus Slave mode.
Slave device_0 address(16)	7-bit hexadecimal value	External power regulator address. This parameter must be non-zero when you are using the PMBus Master mode.
Slave device_1 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_2 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_3 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_4 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_5 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_6 address(16)	7-bit hexadecimal value	External power regulator address.
Slave device_7 address(16)	7-bit hexadecimal value	External power regulator address.
Voltage output format(16)	Auto discovery Direct format Linear format	The voltage output format when the operation mode is PMBus Master. If the voltage output format is the Auto discovery or Direct format, you must set the following parameters: • Direct format coefficient m • Direct format coefficient b • Direct format coefficient R If the voltage regulator is the Linear format, you must set the Linear format N parameter. (18) For all voltage output format, you must also select the correct "translated voltage output unit".
Direct format coefficient m(16)	Signed integer: -32768 to 32767	Direct format coefficient m of the slave device type when the operation mode is PMBus Master.
Direct format coefficient b(16)	Signed integer: -32768 to 32767	Direct format coefficient b of the slave device type when the operation mode is PMBus Master.
Direct format coefficient R(16)	Signed integer: -128 to 127	Direct format coefficient R of the slave device type when the operation mode is PMBus Master.
Linear format N(16)	–16 to 15	Output voltage command when the voltage output format is set to the Linear format.

continued...

(17) This parameter is used for the PMBus Slave mode.

(18) N is the exponent of a 5-bit two's compliment integer.

Parameters	Value	Description
Translated voltage value unit(16)	millivolts	Indicates the translated output voltage is in millivolts (mV) or volts (V).
	volts	
Enable PAGE command(16)	Enable	By enabling the PAGE command, the FPGA PMBus Master will use the PAGE command to set all the output channels (0xFF) on registered regulator modules to respond to VOUT_COMMAND. If only specified output channels on registered regulator modules must respond to VOUT_COMMAND, enter the corresponding page value (0x00 – 0xFF).
	Disable	

3.1.1.3. Intel Stratix 10 Power Management and VID Interface QSF Constraint Guide

You can specify the **Power Management and VID** parameters and options through QSF constraints command.

For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

Example 1. Specifying the Power Management and VID Parameters through QSF Constraints

```
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTM4677
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS41
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS42
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS43
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS44
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS45
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS46
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS47
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS48
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "AUTO DISCOVERY"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD xx
```

4. Intel Stratix 10 Power Management User Guide Archives

For the latest and previous versions of this user guide, refer to Intel Stratix 10 Power Management User Guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

5. Document Revision History for the Intel Stratix 10 Power Management User Guide

Document Version	Intel Quartus Prime Version	Changes
2022.08.26	21.1	Updated the *Multi-Master Mode* section.
2022.06.26	21.1	Updated Table: *Pin Tolerance—Power-Up/Power-Down*.
2022.05.27	21.1	Removed instances of Enpirion from *Power Supply Design* section and *Power Management and VID Parameters* table.
2022.04.04	21.1	• Updated the *Clock Gating* section. • Removed ISL82XX from the slave device type parameters Table: *Power Management and VID Parameters*.
2021.07.02	21.1	Updated Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*.
2021.03.30	21.1	• Added reference to the *Intel Stratix 10 and Intel Agilex™ SmartVID Debug Checklist*. • Added reference to the *Intel FPGA Power and Thermal Calculator Standalone* and *Intel FPGA Power and Thermal Calculator User Guide*. • Updated the Early Power Estimator (EPE) to Intel FPGA Power and Thermal Calculator (PTC). • Updated the *SDM Power Manager* section to remove the shutdown stage. • Updated Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*. • Updated Table: *Supported Voltage Output Format for Intel Stratix 10 Devices with the –V Power Option*. • Updated the description of the slave device type and voltage output format parameters in Table: *Power Management and VID Parameters*.
2020.10.16	20.3	• Updated the *Power-Up Sequence Requirements for Intel Stratix 10 Devices* section to include information for Group 4 power rails. • Updated the *Power-Down Sequence Recommendations and Requirements for Intel Stratix 10 Devices* section to include information for Group 4 power rails. • Updated the *Intel Stratix 10 Power Management and VID Interface QSF Constraint Guide* section. • Updated the SmartVID value and SmartVID programmed value terms to VID-fused value. • Added Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*. • Updated Figure: *Power-Up Sequence for Intel Stratix 10 Devices*. • Updated Figure: *Recommended Power-Down Ramp Specification*. • Updated Figure: *Required Power-Down Ramp Specification*. • Updated Figure: *Required Voltage Differential Specification*. • Updated Figure: *Relaxed Power-Down Duration Specification*.

continued...

Document Version	Intel Quartus Prime Version	Changes
		• Removed note (2) from Figure: *External PMBus Master Software Flow*. • Updated Table: *Configuration Pin Parameters* to include SDM_IO9 to the *Use PWRMGT_ALERT output* parameter. • Updated Table: *Power Management and VID Parameters* to include ED8401, EM21XX, and EM22XX to the *Slave device type* parameter and to update the description of the *Enable PAGE command* parameter.
2020.04.30	20.1	Added the *Supported Voltage Output Format for Intel Stratix 10 Devices with the –V Power Option* table.
2020.01.23	19.4	• Added V_{CCIO3D} power rail in Group 3 and V_{CCIO3C} power rail in Group 4 to the *Intel Stratix 10 GX and SX (L-Tile and H-Tile)* column of the *Voltage Rails* table. • Added V_{CCIO3D} and V_{CCIO3C} power supplies to the *Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry* table. • Updated the *PMBus Slave Mode* section. • Updated the *Power Sequencing Considerations for Intel Stratix 10 Devices* section. • Updated the description for the *Use PWRMGT_ALERT output* parameter in the *Configuration Pin Parameters* table.
2019.11.05	19.3	Updated the power rails in Table: *Voltage Rails*: • Removed V_{CCM_WORD} and V_{CCIO_UIB} from the Intel Stratix 10 GX and SX (L-Tile and H-Tile) column. • Added V_{CCRT_GXE}, $V_{CCRTPLL\_GXE}$, V_{CCCLK_GXE}, and V_{CCH_GXE} in the Intel Stratix 10 MX (HBM, H-Tile, and E-Tile) column. • Removed V_{CCL_HPS}, $V_{CCPLLDIG\_HPS}$, V_{CCPLL_HPS}, and V_{CCIO_HPS} from the Intel Stratix 10 MX (HBM, H-Tile, and E-Tile) column. • Removed V_{CCM_WORD} and V_{CCIO_UIB} from the Intel Stratix 10 TX (H-Tile and E-Tile) column.
2019.09.19	19.3	• Added support for Intel Stratix 10 DX variant in Table: *Voltage Rails*. • Added the following power rails to Table: *Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry*: — V_{CCFUSE_GXP} — V_{CCIO3V} — V_{CCH_GXE} — V_{CCCLK_GXE} — V_{CCRT_GXP} — V_{CCH_GXP} — V_{CCCLK_GXP}
2019.08.23	19.2	Updated the note for V_{CCBAT} in the *Power Supplies Monitored and Not Monitored by the POR Circuitry* section.
2019.07.01	19.2	• Added the *Multi-Master Mode* section. • Added ISL82XX device selection in the slave device type parameters in the *Power Management and VID Parameters* table. • Added the *Intel Stratix 10 Power Management and VID Interface QSF Constraint Guide* section. • Updated the *Temperature Compensation* section to include details on the SmartVID value change for the PMBus Master and PMBus Slave modes. • Updated the Vp-p value in the *Pin Tolerance—Power-Up/Power-Down* table. • Updated the power rails for Group 1, Group 2, and Group 3 in the *Voltage Rails* table.

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Document Version	Intel Quartus Prime Version	Changes
		• Updated the *Stage Flow for the External Power Management Controller in the PMBus Slave Mode* figure. • Updated description in step 6 of the *Specifying Parameters and Options* section. • Updated the description of the slave device type parameter in the *Power Management and VID Parameters* table.

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Document Version	Intel Quartus Prime Version	Changes
2018.09.26	18.1	• Updated the SmartVID details in the *Intel Stratix 10 Power Management Overview* section. • Added the power-screened devices feature in the *Power Reduction Techniques and Features* section. • Added the *Power-Screened Devices* section. • Updated the SmartVID regulator requirements in the *SmartVID Standard Power Devices* section. • Updated the *Power Sequencing Considerations for Intel Stratix 10 Devices* section. • Updated the *Power-Up Sequence Requirements for Intel Stratix 10 Devices* section to provide more information on the Group 2 and Group3 power rails sharing. • Updated the *PMBus Master Mode* and *PMBus Slave Mode* figures. • Removed support for the Pulse-Width Modulation (PWM) mode.
2018.05.07	18.0	• Added the `MFR_ADC_CONTROL` command to the *Supported Commands for the PMBus Master Mode* table. • Updated the *SmartVID* section to include information for the `PWRMGT_SCL` and `PWRMGT_SDA` pins. • Updated the *Stage Flow for the External Power Management Controller in the PMBus Slave Mode* figure. • Removed the *Monitor Stage for the External Power Management Controller in the PMBus Slave Mode* figure. • Updated the description of the direct format equation in the *PMBus Slave Mode* section. • Updated the *Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry* table: — Added the V_{CCRT_GXE} and $V_{CCRTPLL\_GXE}$ rails — Removed the V_{CC_SDM} rail • Editorial updates.
2018.02.28	17.1	• Added the Supported Commands for the PMBus Slave Mode table. • Added a note about the `PWRMGT_ALERT` pin for the PMBus Slave mode in the PMBus Mode section. • Added a note about the I/O standards supported in the PMBus mode in the PMBus Mode section. • Added recommendation to connect to the `PWRMGT_ALERT` when configuring in the PMBus slave mode in the PMBus Slave Mode section. • Added information on the multi-master mode in the PMBus Master Mode section. • Added the direct format equation for the PMBus Slave Mode section. • Added the Temperature Compensation for SmartVID for Intel Stratix 10 Devices figure. • Updated the SmartVID section to change the nominal voltage to 0.9V. • Updated the SmartVID Regulator Requirements table to update the values for the non-CvP and CvP ramp time. • Updated the guidelines for the Power Sense Line section. • Updated the Power Sequencing Considerations for Intel Stratix 10 Devices section. • Updated the value of slave device addresses in the Power Management and VID Parameters table. • Updated the steps in the Specifying Parameters and Options section. • Updated the SDM Power Manager section to include the initial/ shutdown and monitor stages. • Removed the Temperature Compensation for SmartVID for Intel Stratix 10 Devices table.

Date	Version	Changes
May 2017	2017.05.08	• Updated the PowerPlay Early Power Estimator (EPE) to Early Power Estimator. • Updated the Power Consumption section to include the standby power. • Updated the Power Reduction Techniques section. • Updated the SmartVID section to change the nominal voltage to 0.89V. • Updated the SmartVID Feature Implementation in Stratix 10 Devices section. • Updated the SDM Power Management section. • Updated the PMBus Mode section. • Updated the PWM Mode section. • Updated the Temperature Compensation section. • Updated the DSP and M20K Power Gating section. • Updated the Clock Gating section. • Updated the Power Sense Line section. • Updated the Power-On Reset Circuitry section. • Updated the Power-Up and Power-Down Sequences section. • Updated the Using the SmartVID Feature on V_{CC} and V_{CCP} Rails section. • Updated the Power Supply Design section. • Updated the Specifying Parameters and Options section. • Added the Temperature Compensation for SmartVID for Stratix 10 Devices table. • Updated the CvP's ramp time in the SmartVID Regulator Requirements table. • Updated the Power Supplies Monitored and Not Monitored by the Stratix 10 POR Circuitry table to include the HPS power supplies. • Updated the Power Groups Ramping Sequence table. • Updated the Configuration Pin Parameters table. • Updated the Power Management and VID Parameters table. • Updated the Configuration Pin Parameters table. • Updated the Power Management and VID Parameters table. • Updated the SDM Power Management Block Diagram figure. • Updated the PMBus Master Mode figure. • Updated the PMBus Slave Mode figure. • Updated the Power-Up and Power-Down Sequences Requirement for Stratix 10 Devices figure.
October 2016	2016.10.31	Initial release.